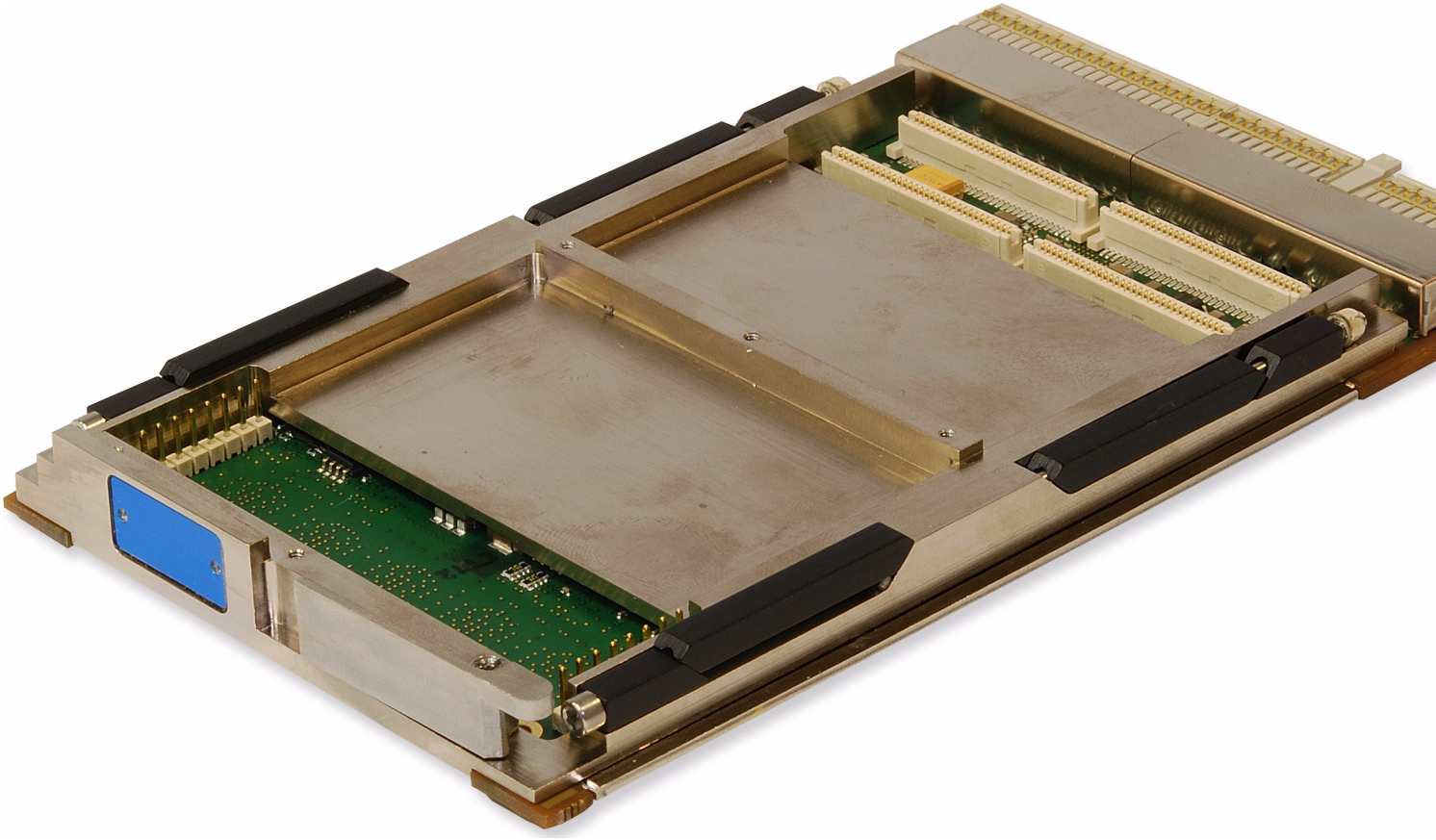
GE
Intelligent Platforms

# Hardware Reference Manual

## IMP3A 3U cPCI Single Board Computer

## Edition 2

Publication No. IMP3A-HRM/2



imagination at work

## Document History

| Edition | Date | Board Artwork Revision |
|---|---|---|
| First | May 2010 | Revision 1 |
| 2 | July 2011 | Revision 2 |
| | | |
| | | |

## Waste Electrical and Electronic Equipment (WEEE) Returns

GE Intelligent Platforms Limited is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE Intelligent Platforms Limited. will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

# Preface

This manual contains hardware information for the IMP3A board with PCB artwork revisions 2 and onwards. The information contained in this manual must be used in conjunction with the PowerPact3 Family Product Manual.

LINK

PowerPact3 Family Product Manual, publication number PP3-0HH.

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# 1 • Overview

The GE Intelligent Platforms IMP3A is a 3U CompactPCI Single Board Computer, using the Freescale P2020 Dual-Core Integrated Host Processor. The board offers up to 4 GBytes of DDR3 SDRAM, scalable NAND Flash memory, Gigabit Ethernet, serial, USB2 and SATA I/O options.

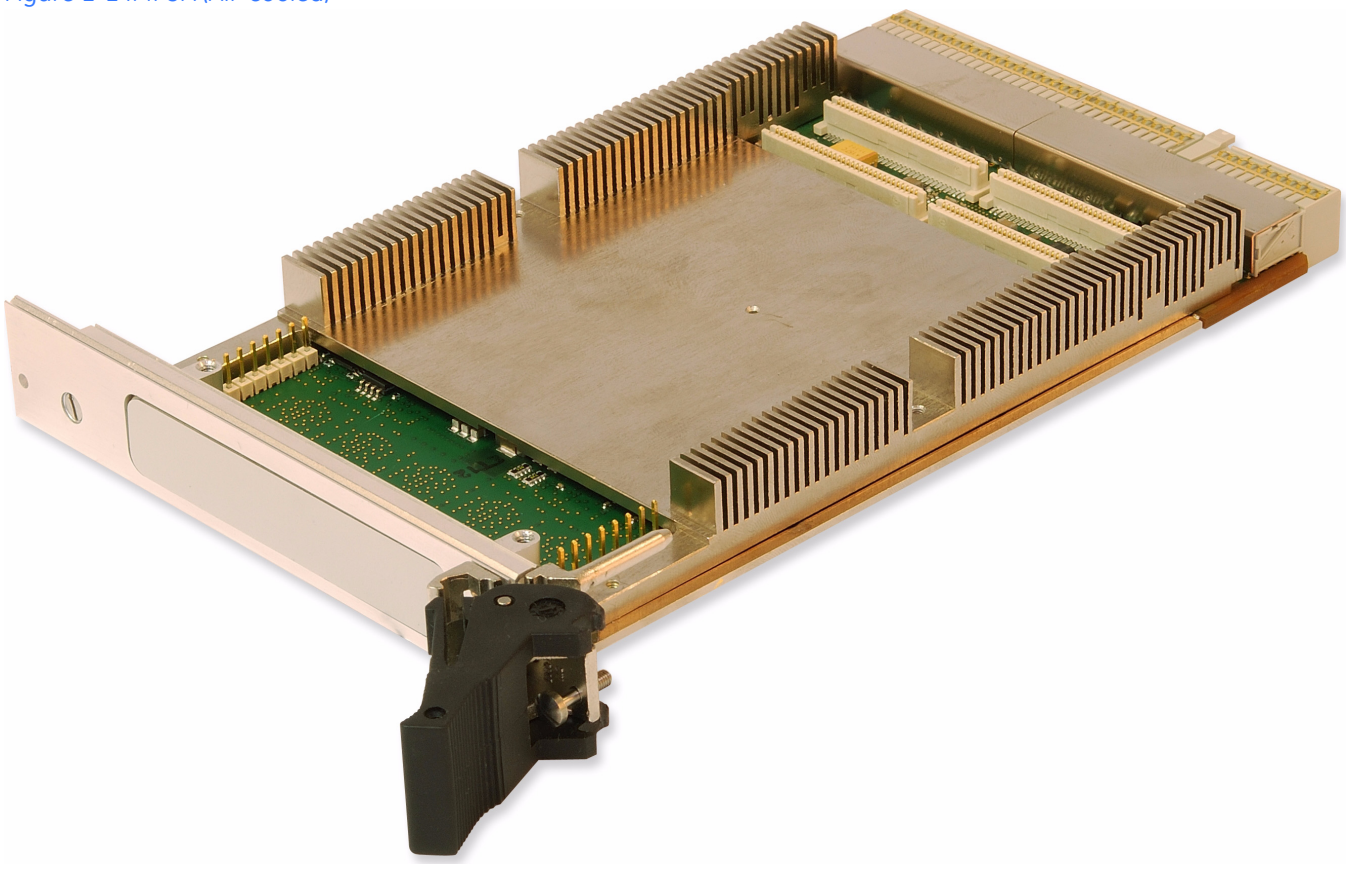
One 64-bit PMC site is provided, supporting PCI-X operation at up to 133 MHz, allowing for off-the shelf or custom mezzanines to be fitted to add further functionality to the board.

The IMP3A is the latest member of the PowerPact3 family, targeted at some of the most demanding applications in embedded computing. By preserving the same hardware interfaces as previous PowerPact3 family members, the IMP3A provides an ideal opportunity for state of the art technology insertion into both upgrade programs and new platforms alike.

## 1.1 Features

- Freescale P2020/P2010 Integrated Host Processor
- Up to 4 GBytes of DDR3 SDRAM
- PCI-X 133 MHz PMC site with up to 64 I/O lines routed (46 minimum)
- Up to two Gigabit Ethernet channels
- Single channel USB 2.0 option
- Up to two SATA 150 MBytes/second channels
- Solid State Drive (SSD) - currently 8 GByte but scalable as silicon becomes available
- Up to 16 bits of GPIO
- Real Time Clock
- Elapsed Time Indicator
- Ambient temperature sensors
- Five environmental build levels

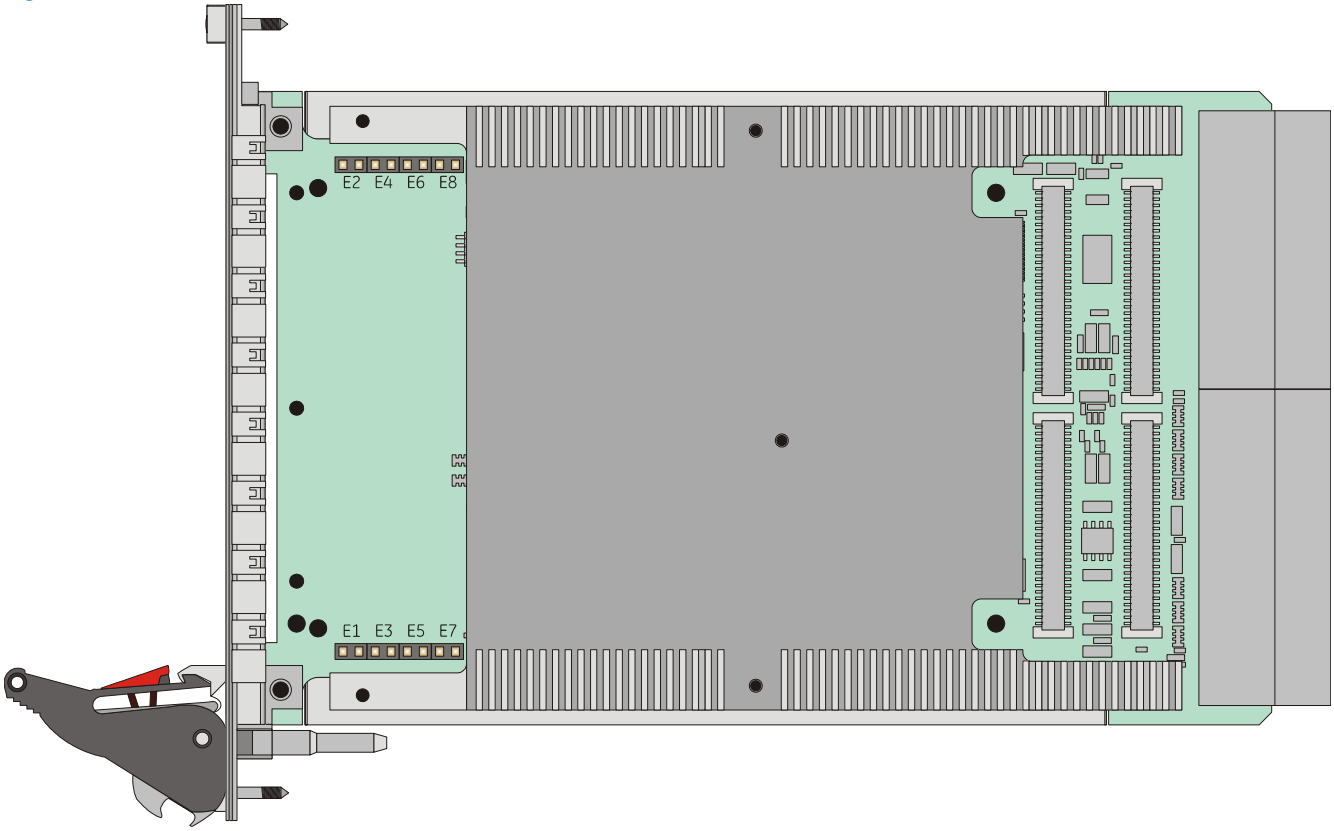
Figure 1-1 IMP3A (Air-cooled)



# 2 • Link Settings

This section describes the configuration of links on the IMP3A. The board is delivered with push-on jumpers, but for more rugged or military applications, link pins must be connected using wire-wraps.

Figure 2-1 Link Locations




## 2.1 Default Link Settings

The IMP3A is shipped from the factory with no links fitted. Before changing any of the link options, refer to the appropriate section(s) in the following pages.

TIP

If you are about to install your board and power-up for the first time, leaving your board in the default configuration will enable board operation to be proven before tackling any further configuration issues.

## 2.2 Link Overview

Some of the links on the IMP3A are connected to a PCA9560 EEPROM Switch device, which is accessible over the $I^2C$ bus and allows software to achieve the same function as fitting or removing a jumper on the appropriate link in a deployed system. Any hardware setting overrides the software setting. The following table shows these links, together with an overview of the functions of all the links.

Table 2-1 Link Overview

| Link | Function | Connected to PCA9560 |
|---|---|---|
| E1 | Core 0 boot area swap | Yes |
| E2 | JTAG Scanbridge output enable | No |
| E3 | Core 1 boot area swap | Yes |
| E4 | Flash protection unlock | Yes |
| E5 | Recovery | No |
| E6 | NVM write enable | Yes |
| E7 | PMC VIO voltage selection | No |
| E8 | SSD write enable | Yes |

## 2.3 Core 0 Boot Area Swap Links (E1 and E5)

The Boot Flash for Processing Core 0 is divided into four sections, allowing for three different boot images to be loaded into Flash. There is also a factory-programmed Recovery boot image. These links are used to select which image is used at boot time. The settings of these links are reflected in the FPGA Configuration Register 1 (Offset 0x0008).

Table 2-2 Core 0 Boot Area Selection

| E1 | E5 | Active Core 0 Boot Image |
|---|---|---|
| Out | Out | Main |
| In | Out | Alternate |
| Out | In | Recovery |
| In | In | Extended |

In normal operation, these links are not fitted, and the IMP3A boots from the Main boot image.

## 2.4 JTAG Scanbridge Output Enable Link (E2)

The IMP3A uses a JTAG Scanbridge device to connect all of the JTAG-compliant devices on the board. This link is provided to enable the Scanbridge on the backplane J1 connector during boundary scan. It should not normally be fitted in deployed systems. The settings of this link is reflected in the FPGA Configuration Register 1 (Offset 0x0008).

Table 2-3 JTAG Scanbridge Output Enable Link

| Setting | Meaning |
|---|---|
| Out | JTAG Scanbridge is disabled (outputs are high) |
| In | JTAG Scanbridge is enabled onto the backplane |

NOTE

If the BDM header on the Test Access Card is being used for access to the P2020 JTAG port, ensure that the Scanbridge device is disabled.

## 2.5 Core 1 Boot Area Swap Link (E3 and E5)

Processing Core 1 may boot either from the same Flash image as Processing Core 0 or from its own Boot Flash, which may hold up to three different boot images. These links are used to select which of the Core 1 boot images is used at boot time, if selected. The settings of these links are reflected in the FPGA Configuration Register 1 (Offset 0x0008).

Table 2-4 Core 1 Boot Area Selection

| E3 | E5 | Active Core 1 Boot Image |
|---|---|---|
| Out | Out | Main |
| In | Out | Alternate |
| Out | In | Reserved |
| In | In | Extended |

In normal operation, these links are not fitted, and the IMP3A boots from the Main boot image.

## 2.6 Flash Protection Unlock Link (E4)

Fitting this link makes the NOR Flash password visible to software via the FPGA Test Registers (offsets 0x0010 to 0x0016), and allows software modification of the Permanent Protection status of NOR Flash memory sectors. Not fitting the link hides the NOR Flash password and prevents changes to the Permanent Protection status, although writes to unprotected Flash sectors are allowed in this case. See the NOR Flash section for more details. The setting of this link is reflected in the FPGA Configuration Register 1 (Offset 0x0008).

Table 2-5 Flash Protection Unlock Link

| Setting | Meaning |
|---|---|
| Out | NOR Flash protection cannot be changed/NAND Flash is write protected |
| In | NOR Flash protection can be changed/NAND Flash is write enabled |

NOTE

This link function is mirrored by the FLASH_WE# pin on the J2 connector (pin B4) to allow protection to be controlled at the system level.

CAUTION

If the EEPROM DIP switch is used to "fit" the NVM Write Enable Link (E6), then it is not possible to hardware write-protect the Flash, since the state of link E4 can be changed in software by changing the EEPROM DIP switch. To apply full hardware protection to a board, link E6 must be removed and disabled in the EEPROM DIP switch

## 2.7 Recovery Link (E5)

In addition to selecting the Recovery boot image (when used in conjunction with link E1 and/or link E3), this link also prevents the loading of EEPROM configuration data by the P2020 and overrides software link settings. This is useful where the EEPROM data has become corrupted and needs to be reprogrammed. The setting of this link is reflected in the FPGA Configuration Register 1 (Offset 0x0008).

Table 2-6 Recovery Link

| Setting | Meaning |
|---|---|
| Out | P2020 can load configuration data from EEPROM (normal mode) |
| In | P2020 prevented from loading configuration data from EEPROM (recovery mode) |

## 2.8 NVM Write Enable Link (E6)

When fitted, this link enables writes to all Non-Volatile Memory, including Serial EEPROMs, NVRAM and $I^2C$ devices. Its setting is reflected in the FPGA Configuration Register 1 (Offset 0x0008).

Not fitting this link ensure that software cannot corrupt any of the non-volatile memory during operation.

Table 2-7 NVM Write Enable Link

| Setting | Meaning |
|---|---|
| Out | Non-Volatile Memory writes disabled |
| In | Non-Volatile Memory writes enabled |

NOTE

This link does not affect the write-protection status of the SSD. That is controlled by link E8.

## 2.9 PMC VIO Voltage Selection Link (E7)

This link selects the VIO signaling voltage for the PMC site. Its setting is reflected in the FPGA Device/Bus Register 1 (Offset 0x0004).

Table 2-8 PMC VIO Voltage Selection Link

| Setting | Meaning |
|---|---|
| Out | VIO is 3.3 V |
| In | VIO is 5 V |

A 0 Ω resistor option is provided to permanently set the site to 5V.

CAUTION

Ensure that the configuration of this link is correct for any PMC fitted before powering up.

CAUTION

Do not change the configuration of this link during normal operation.

## 2.10 SSD Write Enable Link (E8)

This link controls the write protection on the SSD device.

Table 2-9 SSD Write Enable Link

| Setting | Meaning |
|---|---|
| Out | SSD is write-protected |
| In | SSD is write-enabled |

CAUTION

If the EEPROM DIP switch is used to “fit” the NVM Write Enable Link (E6), then it is not possible to hardware write-protect the SSD, since the state of link E8 can be changed in software by changing the EEPROM DIP switch. To apply full hardware protection to a board, link E6 must be removed and disabled in the EEPROM DIP switch

## 2.11 PMC Installation

See the PowerPact3 Family Product Manual, and section 4 for connector pinout information.

LINK

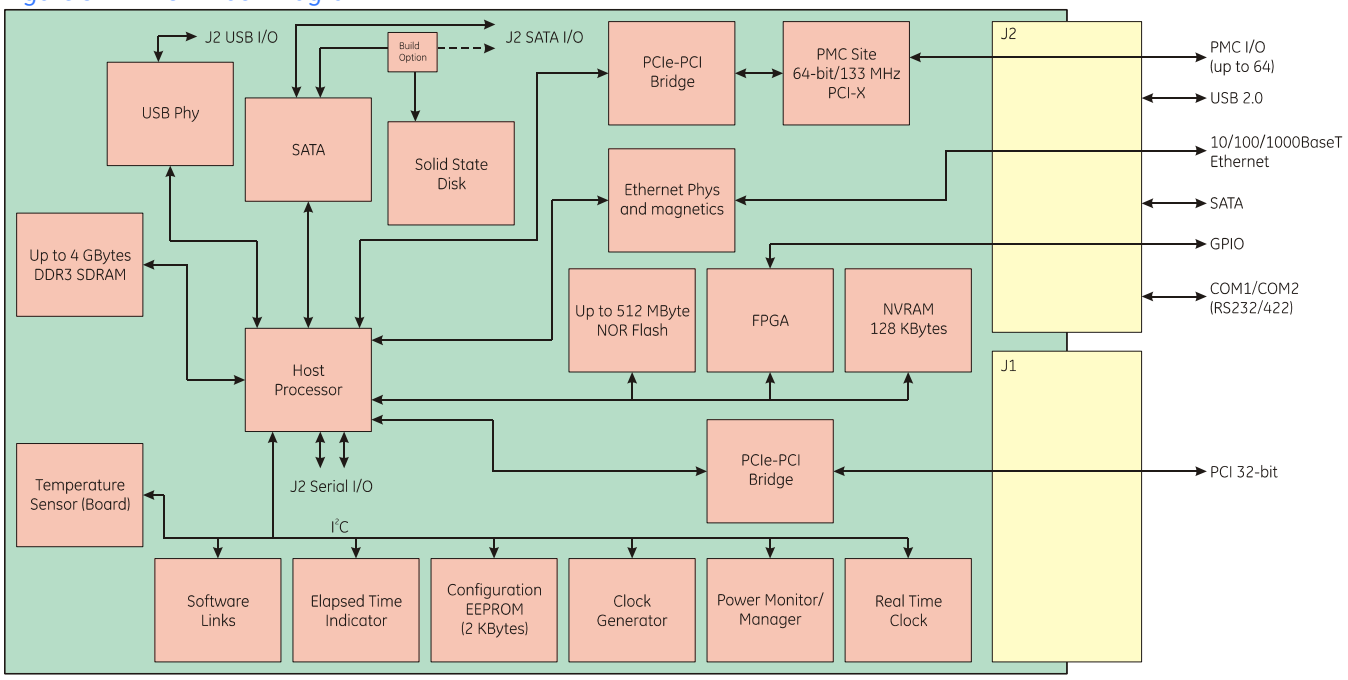
PowerPact3 Family Product Manual, publication number PP3-0HH.

CAUTION

Ensure that the configuration of the PMC VIO Voltage Selection Link (E7) is correct for any PMC fitted before powering up.

# 3 • Functional Description

Figure 3-1 IMP3A Block Diagram




## NOTE

Due to the increasingly short lifetimes of system components, the I/O devices used on the IMP3A are not guaranteed to remain fixed in the future.

Hardware should be accessed only through mechanisms provided by the Operating System's Board Support Package, and not directly by application software.

If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

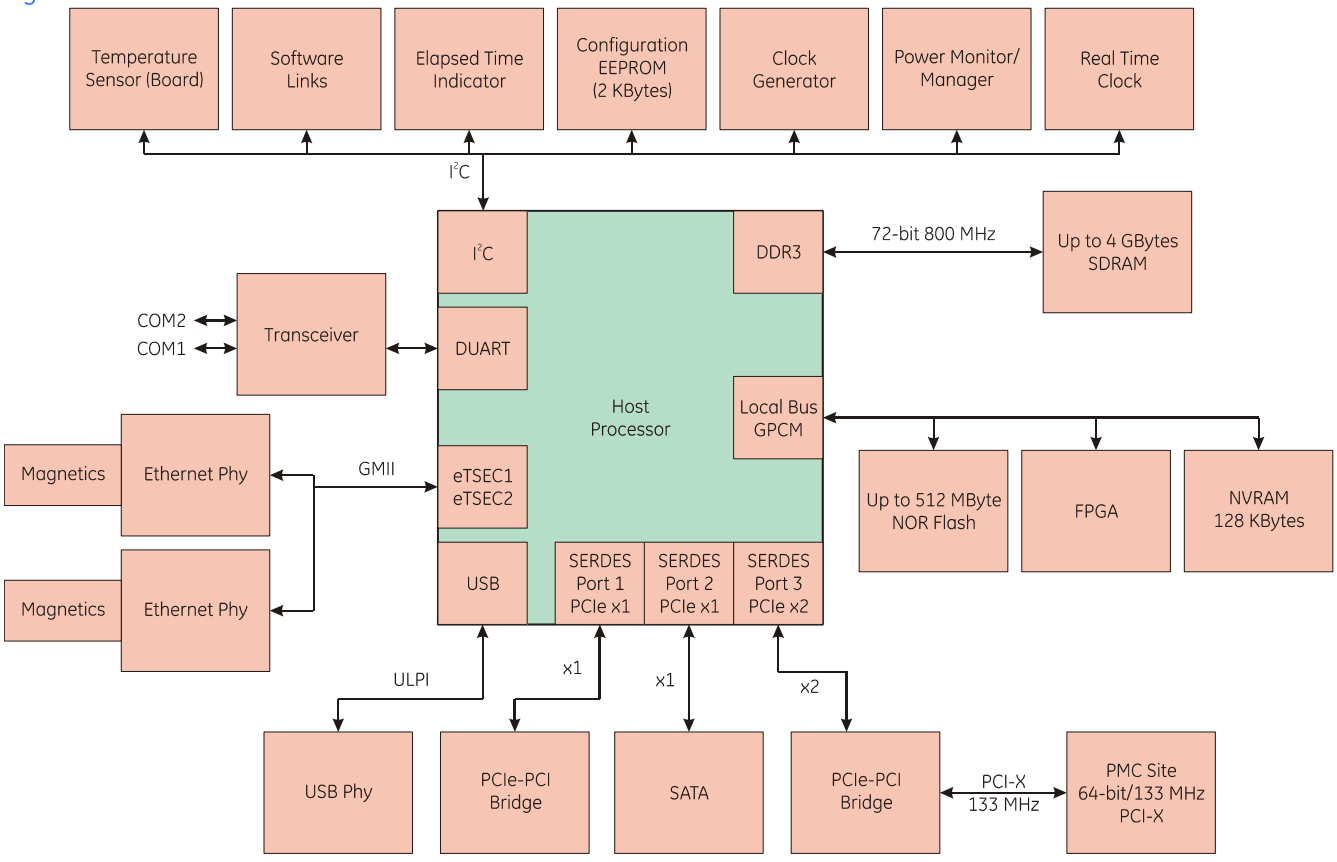
GEIP-supported Operating Systems guarantee compatibility at the application level through hardware independent mechanisms.

## 3.1 Integrated Host Processor

The IMP3A uses the Freescale P2020 processor, which provides the following features:

- Two e500v2 cores operating at frequencies up to 1.2 GHz
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KByte L1 instruction cache and 32 KByte L1 data cache per core
- Shared 512 KByte L2 Cache with ECC
- Two 10/100/1000 Mbps eTSECs
- Three PCIe interfaces, each capable of operating as an endpoint
- High-speed USB interface (USB 2.0)
- DDR3 memory controller with ECC
- Power Management controller
- Two 4-channel DMA controllers
- Two $I^2C$ controllers, DUART, timers
- Enhanced Local Bus Controller (eLBC)
- 16 GPIO lines
- Optional Security Engine

Figure 3-2 Host Processor Interfaces



### 3.1.1 Memory Map

The P2020 supports a fully programmable memory map, shared between each of the processing cores.

Software will set up memory windows; the hardware will not set up any memory windows unless required for the processor to boot.

### 3.1.2 EEPROM Configuration (Boot Sequencer)

An AT24C64A 8 KByte EEPROM is attached to $I^2C$ Bus 1. This is primarily intended as the P2020 boot-sequencer device, and may be used by the P2020 to load various configuration data before the processor cores start to run. It is also possible to use this EEPROM for general purpose storage should it be required by application software.

The EEPROM is write-protected by default to ensure its contents are not corrupted. It may be write-enabled by software only when the NVM Write Enable Link (E6) is fitted, and when the $I^2C$ Device Write Protection bit is cleared in the FPGA Control Register 1 (offset 0x000C). If the data becomes corrupted, the P2020 can be prevented from loading configuration data from the EEPROM by fitting the Recovery Link (E5).

### 3.1.3 Local Bus

The following devices are connected to the P2020 local bus:

- FPGA
- NOR Flash
- NVRAM

These are accessed via the P2020 enhanced Local Bus Controller (eLBC).

### 3.1.4 Local Bus Memory Map

All eight device chip selects for the local bus are made available, shared between the devices as defined in the following table. The minimum possible window size is 32 KBytes.

Table 3-1 Local Bus Chip-select Mapping

| Chip Select | eLBC Machine | Target | Device Width | Required Window Size |
|---|---|---|---|---|
| CS0 | GPCM | Boot Flash | 16-bit | 16 MBytes |
| CS1 | GPCM | User Flash (core 0) | 16-bit | 128 MBytes in Paged Mode, up to 1 GByte otherwise |
| CS2 | GPCM | User Flash (core 1) | 16-bit | 128 MBytes in Paged Mode, up to 512 MBytes otherwise |
| CS3 | GPCM | NVRAM | 8-bit | 128 KBytes |
| CS4 | GPCM | Control/Status registers, Interrupt Controller, Watchdogs | 16-bit | 32 KBytes |
| CS5 | GPCM | System Semaphore Register | 16-bit | 32 KBytes |

### 3.1.5 Processor Power Management

All power management features of the processing cores, such as the programmable power states (Doze, Nap and Sleep) and Dynamic Power Management within the P2020 are available to the software. No external hardware support is required.

### 3.1.6 PCI Express Power Management

The PCI Express links support several power management features, which are under software control and require no hardware support.

## 3.2 Memory

### 3.2.1 RAM

The IMP3A provides 1 GByte of DDR3 RAM with ECC as standard, and supports up to 4 Gbytes. The RAM is implemented by nine 8-bit DDR3 devices. The FPGA Device/Bus Register 1 (Offset 0x0004) shows the configuration of memory fitted.

### 3.2.2 NOR Flash

The following table shows the Flash options available for the IMP3A:

Table 3-2 Flash Options

| Flash Size (MBytes) | Banks | Organization | Comments |
|---|---|---|---|
| 256 | 2 | 2 x 1 Gbit | Standard configuration |
| 512 | 2 | 2 x 2 Gbit | Not yet available |

The Flash uses 16-bit wide Spansion S29GL family devices arranged in 128 KByte sectors, has an erase capacity of 100,000 cycles per sector and typical data retention of 20 years. Flash details are available to software via the FPGA Device/Bus Register 1 (offset 0x0004).

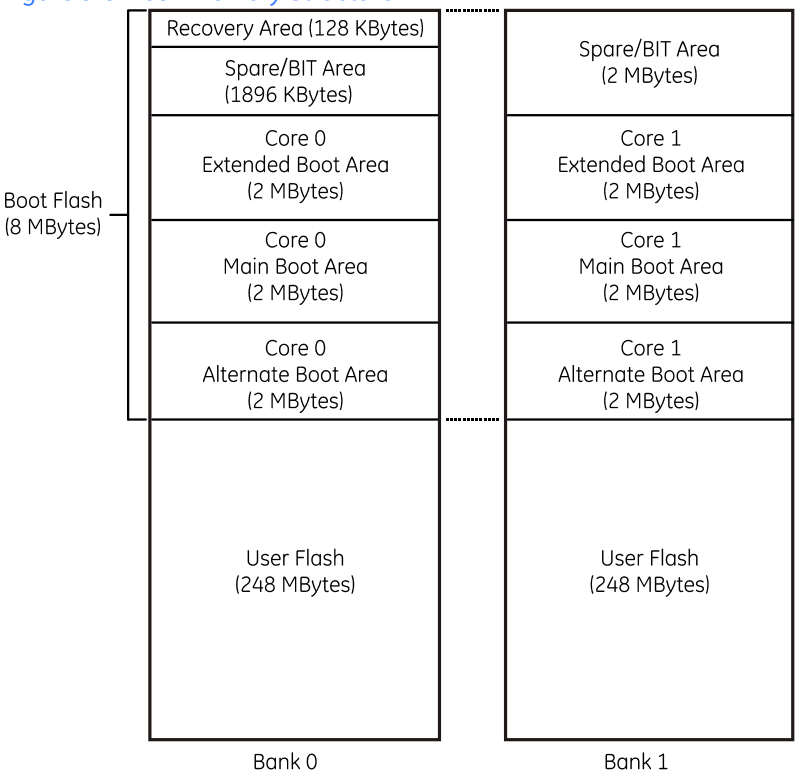
The Flash supports page-mode accesses, which allows the Flash array to be accessed in 128 MByte pages. Separate Flash control is provided for each processor core, to allow the IMP3A to operate in AMP mode.

**CAUTION**

Integrity of Flash data cannot be guaranteed if a hard reset occurs during a Flash write cycle.

The following figure shows the Flash memory structure. Bank 0 holds the Boot Flash for core 0 and Bank 1 holds the Boot Flash for core 1. The boot images may be selected using hardware links.

Figure 3-3 Flash Memory Structure



## Boot Flash

The top 8 MBytes of Flash memory on each of the Flash banks is used as Boot Flash, and holds initialization and operating system boot routines for one of the processing cores (the Bank 0 region for core 0; bank 1 for core 1). If a single-core device is used or a separate boot image for core 1 is not required (e.g. if an SMP operating system is used), the 8 MByte region in Bank 1 may be considered as part of the contiguous block of User Flash.

Each Boot Flash region contains four independent 2 MByte boot areas (Main, Alternate, Extended and Recovery). The active boot area for each processing core is selected using the appropriate links (E1 and E5 for Core 0; E3 and E5 for Core 1), as shown in the following table:

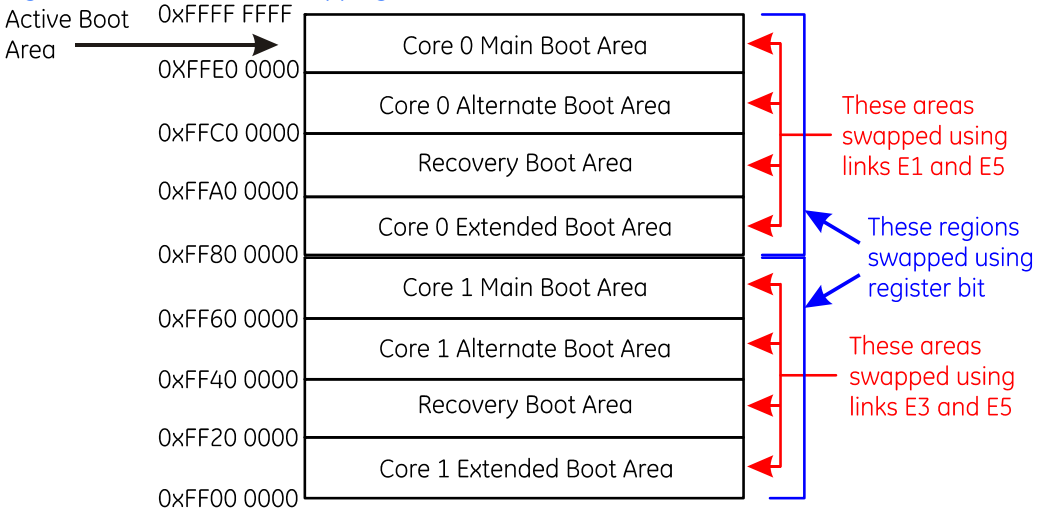
Table 3-3 Boot Image Selection

| E1/E3 | E5 | Boot Image |
|---|---|---|
| Out | Out | Main |
| In | Out | Alternate |
| Out | In | Recovery |
| In | In | Extended |

The Recovery (BANC) boot area contains a 128 KByte factory-programmed boot image, shared by both processing cores, allowing the Flash to be reprogrammed if other boot images become corrupted. This area is limited to a size of 128 KBytes as only one device's top sector is available (the top sectors of the other banks are not used in this way as this would break up the linear Flash array). The Recovery area is protected by hardware and is not writeable by the user. The remainder of this 2 MByte area can be used to store BIT results.

By default, the P2020's CPU address map provides a fixed 8 MByte window from 0xFF80 0000 to 0xFFFF FFFF, which is mapped to the eLBC to access Boot Flash. The default chip select mapping causes the eLBC to select Chip Select 0 (CS0), which is always used to access the Boot Flash. The boot areas are mapped into the 8 MByte window as shown in the following figure (default mapping shown).

Figure 3-4 Local Bus CS0 Mapping



When a core comes out of reset, it begins execution with the instruction at address 0xFFFF FFFC. Core 0 always boots from the Core 0 boot area, but Core 1 can boot from either area. If a separate boot image is required for Core 1, the Core 1 boot region can be made active by setting the Core 1 Boot Mode bit in the FPGA Flash Addressing Control Register (Offset 0x0050) before allowing core 1 to boot.

The other (inactive) boot region is mapped to the 8 MByte block below the standard boot window, providing the ability for software to access both boot regions.

The Boot Flash can also be accessed through CS1 or CS2 (see below).

### User Flash

Any Flash that is not used as Boot Flash is designated as User Flash and is intended to hold user application code or data.

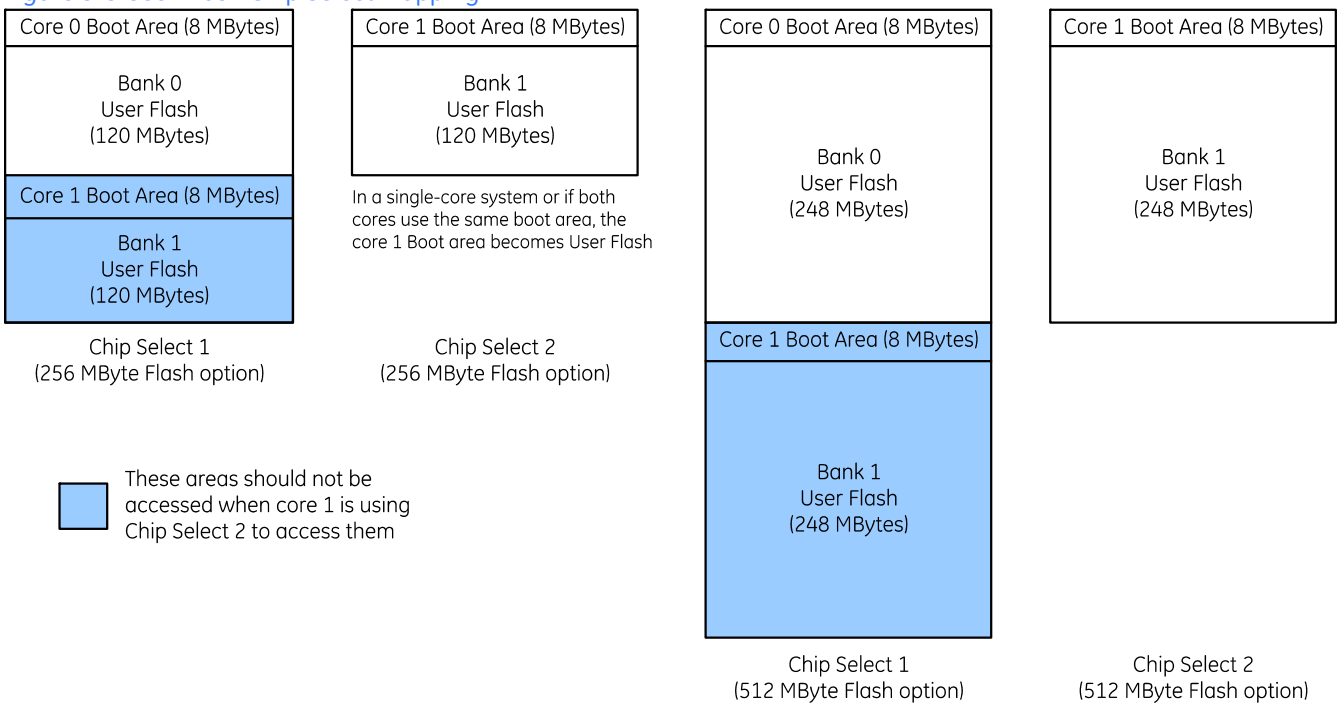
Two P2020 chip selects (CS1 and CS2) are used to access half of the linear Flash array each. CS1 is intended for use by processing core 0 and may be used to access the upper area of Flash; CS2 is intended for use by processing core 1 and may only access the lower area of Flash. This enables each processing core to access a specific Flash region independently of the other core, allowing the use of Flash file systems while running in AMP mode.

For use in a single core or SMP system, CS1 may actually access the entire Flash array as a single block. To ensure private access for core 1, when it is using CS2 to access Flash, core 0 should not use CS1 to access the same area.

CS1 and CS2 also allow access to the 8 MByte Boot Flash areas at the top of the User Flash area. The four boot images appear in their physical locations (as shown in Figure 3-3) unaffected by the state of the Flash Boot Image Select links.

The following figure shows how the User Flash is mapped for 256 MByte and 512 MByte build options:

Figure 3-5 User Flash Chip Select Mapping



Where less than the maximum amount of Flash is fitted, the top address bits are not connected to the devices, so the memory range appears to be mirrored to fill the entire space. This allows software to map space from the base address up or the top address down as required.

### MAC Address Mirror Mode

The Recovery Boot Area is accessible in User Flash, only in the top sector of Flash Bank 0 (accessed via Chip Select 1). This area also contains the board's serial number and MAC addresses, which may be required by processor core 1 (accessing Flash via Chip Select 2). There is a function to "mirror" the top sector of Flash Bank 0 to Flash Bank 1 to allow this to be visible to software. This mode is controlled by the FPGA Flash Addressing Control Register (Offset 0x0050) and is enabled by default. It may be disabled, as this feature is not desirable in a single core or SMP mode.

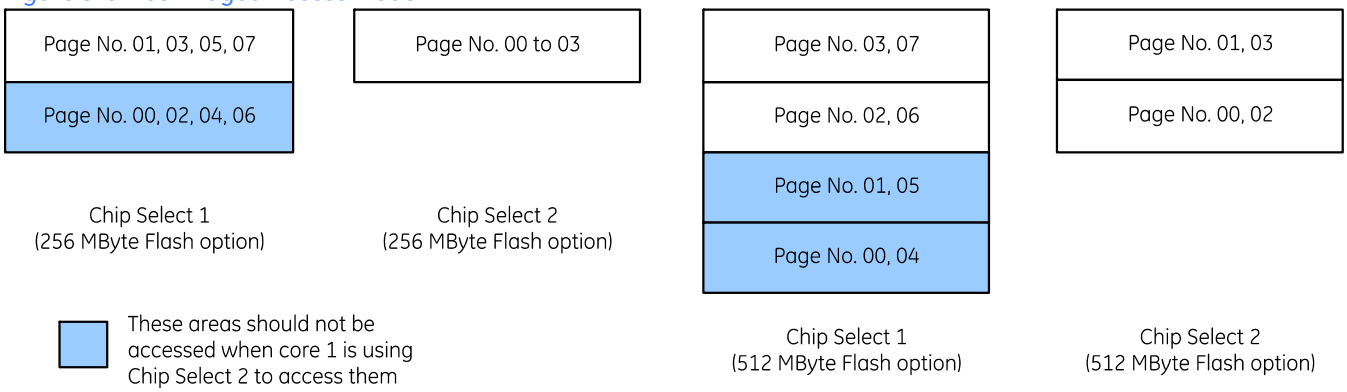
### Paged Flash Mode

Due to limitations on the size of the processor memory map, a paged mode is provided. Here, the Flash is divided into 128 MByte pages, with separate pages selectable for each processing core, allowing them independent access. This mode is enabled and controlled by the FPGA Flash Addressing Control Register (Offset 0x0050). Paging is enabled by default, with each Chip Select (CS1 and CS2) pointing to the top page of Flash (containing each processor's boot region). When accessing the Flash through CS0, the paged address bits are forced high to ensure that the top of the device is always accessed.

**NOTE**

As CS2 can only access half of the Flash, its page range is 0 to 3. For CS1, the page range is 0 to 7.

Figure 3-6 Flash Paged Access Mode



## Flash Sector Protection

The IMP3A uses Spansion S29GL family Flash devices, which provide advanced methods of sector protection to ensure the integrity of code data contained in the Flash array. Protection is defined on a per-sector basis, where a sector is 128 KBytes in size. Locked sectors cannot be erased or programmed; they may only be read.

No write protection of Flash is provided by hardware. Software must be used to configure the Flash devices to protect against corruption of Flash data. The following types of protection are provided:

1. Persistent sector protection provides non-volatile protection that remains in place when a board is power cycled or reset. Each Flash sector may be set as locked (write-protected) or unlocked (write-enabled) by writing to configuration registers within the Flash. The configuration of this protection is only possible when the Flash Protection Unlock Link (E4) is fitted or the FLASH_WE# pin on the J2 connector (B4) is driven low. If this link is fitted, the software may change the sector protection, otherwise those sectors that are locked may not be erased or reprogrammed under any circumstances.
2. Non-persistent protection may also be used. In this case, sectors locked using Persistent mode may not be erased or reprogrammed, but previously unlocked sectors may now be locked. However, this protection is only present until a power cycle or hardware reset occurs.

NOTE

Do not rely on non-persistent protection, as it may be subsequently altered by software. If further protection is required, use the Persistent protection method.

For further details of these protection mechanisms, see the S29GL Flash Family data sheet.

Software can detect the setting (fitted or not fitted) of the Flash Protection Unlock Link (E4) from the FPGA Test Registers, which read 0xAAAA or 0x5555 when the link is removed.

The Flash devices' top-sector hardware protection mechanism is used to provide the 128 KByte Recovery (BANC) boot area in the first Flash bank. This sector is protected by default and cannot be unprotected by the user.

### 3.2.3 NVRAM

The IMP3A has 128 KBytes of non-volatile RAM for configuration data storage and general purpose use. This functionality is provided by a Ramtron FRAM device, which uses ferroelectric technology to provide the non-volatile functionality. Chip select CS3 is used to access the NVRAM, which can be read from and written to in the same way as standard RAM.

The NVM Write Enable Link (E6) allows write access to the NVRAM when fitted.

### 3.2.4 Solid State Drive

A Silicon Motion SM631x Solid State Drive (SSD) is fitted to the IMP3A. The SSD device integrates an SLC NAND array and a controller with a SATA gen 2 interface, connected to SATA channel 0. The controller uses ECC and wear-levelling to provide a robust storage area.

Overall drive capacity is dictated by available technology. The IMP3A currently supports up to 8 GBytes of SSD memory, but this is scalable as the silicon becomes available.

Hardware write protection is implemented by the SSD Write Enable Link (E8). When the link is removed, the SSD is in write protection mode and all write/erase operations are inhibited.

NOTE

This link can also be "fitted" in software by means of the EEPROM DIP switch.

The presence and capacity of the SSD can be read from the FPGA Device/Bus Register 2 (Offset 0x0006).

As a build option, SATA channel 0 can be routed to the backplane instead of the SSD.

NOTE

It is not possible for an IMP3A to be fitted with on-board SSD *and* have SATA channel 0 routed to the backplane.

## 3.3 CPCI Interface

The interface to the CompactPCI backplane complies with PICMG 2.0 R3.0. It can operate at 33 MHz or 66 MHz. The frequency setting used is determined by the system, and is reported in the FPGA Device/Bus Register 1 (offset 0x0004). A Pericom PI7C9X110 provides the PCI interface. This device is 5 V tolerant, allowing the IMP3A to operate within a 5V system.

The IMP3A can function as either a System Controller or as a peripheral. The mode of operation is automatically set by the SYSEN# backplane signal (on J2 pin C2) and reflected in the FPGA Device/Bus Register 2 (offset 0x0006).

A build option allows the board to be configured in 'peripheral only' mode, which frees up J2 connector pins that are only used in the System slot and allows all 64 I/O pins from the PMC site to be available. This is reflected in the FPGA Configuration Register 2 (offset 0x000A).

CAUTION

Do not install a 'peripheral only' IMP3A in a System Controller slot.

### 3.3.1 System Controller Functions

When configured as System Controller, the IMP3A has the following features:

- 7 clock outputs, providing support for an 8 slot system
- 8-slot arbiter (provided by the Pericom PI7C9X110)
- Interrupt handling for INTA#, INTB#, INTC# and INTD#
- Drives RST# to the CPCI backplane

These functions are supported by configuring the PI7C9X110 as a transparent bridge, and configuring the P2020 PCIe port 1 into Root Complex mode when the board is in the System Controller slot.

### 3.3.2 Peripheral Functions

Peripheral functionality is supported by configuring the PI7C9X110 as a transparent bridge, and configuring the P2020 PCIe port 1 into end-point mode when the board is in a peripheral slot.

As a peripheral, the P2020 PCIe controller (endpoint) retries all incoming PCI configuration cycles until the CFG_READY bit in the PEX_CFG_READY register is set by local software. This ensures that the system controller cannot enumerate the IMP3A into the system before the board has booted, and local software is running.

As a peripheral card, the IMP3A can generate INTA#, INTB#, INTC# and INTD# on the CPCI backplane. For further details on interrupts see the Interrupts section.

## 3.4 I/O

There are several I/O options available (see the Product Codes section). The actual options selected are shown in the FPGA Configuration Register 2 (offset 0x000A). Due to pin-out restrictions, the various options share pins on the J2 connector. See the J2 Connector section for more details.

### 3.4.1 Ethernet

The IMP3A provides two Ethernet channels. Both can operate in 10BaseT, 100BaseT and 1000BaseT modes. Variant options determine which channels are available on the J2 connector, and whether the additional signals required for 1000BaseT operation are routed. The following table shows the connector pins on which the Ethernet signals appear (depending on the variant):

Table 3-4 Ethernet Channel Pin Mapping

| Signal | J2 Pin | Signal | J2 Pin |
|---|---|---|---|
| ETH0_0+ | E14 | ETH1_0+ | A16 |
| ETH0_0- | E16 | ETH1_0- | B16 |
| ETH0_1+ | C4 | ETH1_1+ | A17 |
| ETH0_1- | D4 | ETH1_1- | B17 |
| ETH0_2+ | D20 | ETH1_2+ | E19 |
| ETH0_2- | C20 | ETH1_2- | E18 |
| ETH0_3+ | D19 | ETH1_3+ | D18 |
| ETH0_3- | C19 | ETH1_3- | C18 |

The Ethernet physical interfaces are provided by two Marvell 88E1119R Phys. These are connected to the P2020's integrated eTSEC1 and eTSEC2 interfaces using the GMII protocol. The Phys are configured as addresses 0x1 and 0x2.

The Phys support a downshift function, which enables them to auto-negotiate using only two signal pairs (normally, auto-negotiation requires all four pairs to be connected). This allows the Phys to fall back to 10/100 mode when only two signal pairs are connected (i.e. when the Ethernet channel build options are configured for 10/100 operation only).

Table 3-5 Downshifted Signal Equivalence

| Gigabit Signal | 10/100 Signal |
|---|---|
| ETHx_0+ | TX+ |
| ETHx_0- | TX- |
| ETHx_1+ | RX+ |
| ETHx_1- | RX- |

The Phys support automatic Tx/Rx swapping, allowing connection between two channels without the use of a switch. The Phys also support automatic polarity correction.

Link Status LEDs are associated with each Ethernet channel. See the LEDs section.

### 3.4.2 Serial Communication Ports

Two RS232/RS422 serial ports are available on the IMP3A. For COM1, variant options determine whether RS422 is available, but as a minimum RS232 TXD and RXD are available.

COM1 and COM2 are provided by the DUART internal to the P2020 device. This interface is fully software compatible with the PC16552D.

Each port is connected to the J2 connector (where the variants allow) via ISL41334 transceiver devices. All serial COM inputs are ESD protected up to ±15 KVolts.

The following table summarizes the modes of operation available to each serial channel.

Table 3-6 COM Port Summary

| COM Channel | Available Signals[a] | Protocols |
|---|---|---|
| 1 | 2 or 4 | RS232, no RTS/CTS (minimum configuration)<br>RS232 with RTS/CTS<br>RS422 |
| 2 | 4 permanent | RS232 with RTS/CTS<br>RS422 |

a. Variant dependant.

The following table shows the connector pins on which the serial signals appear (depending on the variant):

Table 3-7 Serial Channel Pin Mapping

| Signal (RS232/RS422) | J2 Pin | Signal (RS232/RS422) | J2 Pin |
|---|---|---|---|
| COM1_TXD/TXD_A | A18 | COM2_TXD/TXD_A | B15 |
| COM1_RTS/TXD_B | C18 | COM2_RTS/TXD_B | C18 |
| COM1_RXD/RXD_A | B18 | COM2_RXD/RXD_A | B14 |
| COM1_CTS/RXD_B | D18 | COM2_CTS/RXD_B | A14 |

The COM port configurations are controllable via the FPGA Control Register 2 (offset 0x000E).

### 3.4.3 SATA

The IMP3A optionally provides up to two channels of SATA, using the Silicon Image Sil3132 device, which is connected to the P2020 via a x1 PCIe link. SATA channel 0 is normally routed to an SSD (see the SSD section for more details), but as a build option, can be routed to the backplane instead.

NOTE

It is not possible for an IMP3A to be fitted with on-board SSD *and* have SATA channel 0 routed to the backplane.

The following table shows the J2 connector pins on which the SATA signals appear (depending on the variant):

Table 3-8 SATA Channel Pin Mapping

| Signal | J2 Pin | Signal | J2 Pin |
|---|---|---|---|
| SATA1_TX+ | B6 | SATA0_TX+ | C21 |
| SATA1_TX- | A6 | SATA0_TX- | D21 |
| SATA1_RX+ | E5 | SATA0_RX+ | E21 |
| SATA1_RX- | D5 | SATA0_RX- | E19 |

Link Status LEDs are associated with the two SATA channels. See the LEDs section.

### 3.4.4 USB

The IMP3A optionally provides one channel of USB2.0. Common mode chokes are fitted on the data-lines to filter high frequency noise.

The USB controller functions are provided by the P2020 device, which is connected to a SMSC USB3300 USB Phy via the ULPI interface operating at 3.3V.

The following table shows the J2 connector pins on which the USB channel appears (depending on the variant):

Table 3-9 USB Pin Mapping

| Signal | J2 Pin |
|---|---|
| USB_D+ | C21 |
| USB_D- | D21 |
| USB_PWR | D14 |

### 3.4.5 General Purpose I/O

The IMP3A provides a total of 16 GPIO lines, all of which can tolerate 5V input voltages. All GPIO lines are controlled by the GPIO controller in the FPGA, which supports edge/both-edge/level interrupt generation, input/output control and TTL/open-drain modes. For more details see the FPGA GPIO Controller section.

The GPIO lines available at the J2 connector vary with the board's build variant. The following tables summarize the I/O mapping of the GPIO lines. The FPGA GPIO Presence Register (offset 0x0428) shows which lines are available.

Table 3-10 GPIO Pin Mapping

| GPIO Line | J2 Pin Number | GPIO Line | J2 Pin Number |
|---|---|---|---|
| 0 | E21 | 8 | C19 |
| 1 | D21 | 9 | E18 |
| 2 | C21 | 10 | D18 |
| 3 | E20 | 11 | C18 |
| 4 | D20 | 12 | C5 |
| 5 | C20 | 13 | B5 |
| 6 | E19 | 14 | A5 |
| 7 | D19 | 15 | E4 |

Table 3-11 GPIO Availability Summary

| Build Variant | GPIO | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IMP3A-xxxxx0xx | - | - | - | - | - | - | - | - | - | - | - | - | Y | Y | Y | Y |
| IMP3A-xxxxx1xx | - | - | - | - | - | - | - | - | - | - | - | - | Y | N | N | Y |
| IMP3A-xxxxx2xx | - | - | - | - | - | - | - | - | - | - | - | - | N | N | N | N |
| IMP3A-xxxxx3xx | - | - | - | - | - | - | - | - | - | - | - | - | N | N | N | N |
| IMP3A-xxxxx4x | - | - | - | - | - | - | - | - | - | - | - | - | N | N | N | N |
| IMP3A-xxxx0xxx | N | N | N | N | Y | Y | Y | Y | Y | Y | Y | Y | - | - | - | - |
| IMP3A-xxxx4xxx | N | N | N | N | N | N | N | N | N | N | N | N | - | - | - | - |
| IMP3A-xxxx6xxx | Y | Y | Y | Y | N | N | N | N | N | N | N | N | - | - | - | - |
| IMP3A-xxxx7xxx | N | N | N | N | N | N | Y | Y | Y | Y | Y | Y | - | - | - | - |
| IMP3A-xxxx8xxx | N | N | N | N | Y | Y | Y | N | N | Y | N | N | - | - | - | - |

**Key** N = not available, Y = available, - = not defined by this variant.

## 3.5 PMC Site

The IMP3A provides a single PMC site. Mechanically, it complies with the (now withdrawn) IEEE-P1386 (build levels 1 to 3) and VITA 20-2001 (build levels 4 and 5). All build levels comply with IEEE-P1386.1 (PMC specification) and VITA 39-2003 (PCI-X on PMC). Some aspects of VITA 32-2003 (Processor PMC support) are also included. See the Standard Interfaces section for more details.

The presence of a PMC in the site can be determined from the FPGA Configuration Register 2 (offset 0x000A).

### 3.5.1 VIO Selection

The PMC site can operate with either 5 V or 3.3 V VIO signaling. The connection to VIO is determined by the PMC VIO Voltage Selection Link (E7), which controls on-board FETs to switch the required voltage rail onto the VIO line. The setting of this link is reflected in the FPGA Device/Bus Register 1 (offset 0x0004).

CAUTION

Ensure that the configuration of this link is correct for any PMC fitted before powering up.

### 3.5.2 PCI Interface

The Pericom PI7C9X130 PCIe-PCI-X bridge provides a 64-bit PCI-X 133 MHz PCI interface to the PMC card.

**Bandwidth Limitation**

Due to the architecture of the IMP3A, the PCIe to PCI-X bridge is only connected using a x2 PCIe link. This limits the bandwidth in one direction to 512 MBytes/second, whereas PCI-X/133 MHz is capable of 1 GByte/second.

### 3.5.3 Rear I/O Tracking

IO(1:64) is tracked between PMC connector J14 and the rear J2 connector. In System Controller mode, only IO(1:46) are available; in Peripheral Only mode, IO(1:64) are available. All tracks are routed as 50 Ω single-ended signals where possible, and trace length is matched to within 0.25". In cases where a PMC I/O signal shares a connection to J2 with an alternate function, a $Z_0$ impedance of 50 Ω cannot be guaranteed.

The following table shows the J2 connector pins on which the J14 signals appear (depending on the variant).

Table 3-12 J14 to J2 Pin Mapping

| J14 Pin | J2 Pin (IMP3A-xxxxxxSx) | J2 Pin (IMP3A-xxxxxxPx) | J14 Pin | J2 Pin (IMP3A-xxxxxxSx) | J2 Pin (IMP3A-xxxxxxPx) |
|---|---|---|---|---|---|
| 1 | E13 | E13 | 33 | C7 | C7 |
| 2 | D13 | D13 | 34 | B7 | B7 |
| 3 | C13 | C13 | 35 | A7 | A7 |
| 4 | B13 | B13 | 36 | E6 | E6 |
| 5 | A13 | A13 | 37 | D6 | D6 |
| 6 | E12 | E12 | 38 | C6 | C6 |
| 7 | D12 | D12 | 39 | B6 | B6 |
| 8 | C12 | C12 | 40 | A6 | A6 |
| 9 | B12 | B12 | 41 | E5 | E5 |
| 10 | A12 | A12 | 42 | D5 | D5 |
| 11 | E11 | E11 | 43 | C5 | C5 |
| 12 | D11 | D11 | 44 | B5 | B5 |
| 13 | C11 | C11 | 45 | A5 | A5 |
| 14 | B11 | B11 | 46 | E4 | E4 |
| 15 | A11 | A11 | 47 | | E15 |
| 16 | E10 | E10 | 48 | | D15 |
| 17 | D10 | D10 | 49 | | B4 |
| 18 | C10 | C10 | 50 | | A4 |
| 19 | B10 | B10 | 51 | | E3 |
| 20 | A10 | A10 | 52 | | D3 |
| 21 | E9 | E9 | 53 | | C3 |
| 22 | D9 | D9 | 54 | | B3 |
| 23 | C9 | C9 | 55 | | A3 |
| 24 | B9 | B9 | 56 | | E2 |
| 25 | A9 | A9 | 57 | | D2 |
| 26 | E8 | E8 | 58 | | C2 |
| 27 | D8 | D8 | 59 | | B2 |
| 28 | C8 | C8 | 60 | | A2 |
| 29 | B8 | B8 | 61 | | E1 |
| 30 | A8 | A8 | 62 | | D1 |
| 31 | E7 | E7 | 63 | | C1 |
| 32 | D7 | D7 | 64 | | B1 |

## 3.6 I²C Buses

The P2020 device provides two I²C buses. Only one bus is used on the IMP3A to connect all I²C devices. The following table shows the devices resident on bus 1:

Table 3-13 I²C Address Summary

| Device | 7-bit Address | 8-bit Write Address |
|---|---|---|
| P2020 Configuration EEPROM | 0x50 | 0xA0 |
| Board Temperature Sensor | 0x48 | 0x90 |
| Real Time Clock | 0x51 | 0xA2 |
| CPU Temperature Sensor | 0x4C | 0x98 |
| P2020 | Programmable | |
| Elapsed Time Indicator | 0x6B | 0xD6 |
| Power Manager | 0x40 | 0x80 |
| Clock Generator | 0x6E | 0xDC |
| EEPROM DIP Switch | 0x4D | 0x9A |

I²C devices are write-enabled in Recovery mode or external program mode.

### 3.6.1 P2020 Configuration EEPROM

See section 3.1.2.

### 3.6.2 Board Temperature Sensor

The LM92 temperature sensor is capable of monitoring the ambient temperature on the PCB. The interrupt outputs of this device are able to generate interrupts at the P2020 at two software-defined temperature thresholds.

### 3.6.3 CPU Temperature Sensor

The ADT7461 temperature sensor provides the ability to measure the temperature of the PCB in the vicinity of the P2020, giving an indication of the core temperature.

The interrupt outputs of this device are able to generate interrupts to the P2020 at software defined temperature thresholds. These are wire-ORed with the LM92 board temperature sensor.

### 3.6.4 Elapsed Time Indicator

A Dallas DS1682 ETI logs the amount of time the IMP3A is powered and the number of power cycles.

### 3.6.5 EEPROM DIP Switch

The Philips PCA9560 EEPROM DIP switch device provides software control over some of the hardware links. This allows the IMP3A to be set into certain configurations without the need to fit jumpers to the board. This is mainly intended for use in deployed systems.

This device has open drain outputs, and its state is always over-ridden by a fitted link.

An override function is used to default all the outputs to a '1' (link not fitted) for recovery purposes, and programming of blank boards. This function is enabled when the board is in external programming mode or when the Recovery Link (E5) is fitted.

The following table shows which outputs are assigned to which link functions.

Table 3-14 EEPROM DIP Switch Link Assignment

| Output | Link Function[a] |
|---|---|
| A | Core 0 boot area select |
| B | Core 1 boot area select |
| C | NVM write enable |
| D | Flash password reveal |
| E | SSD write enable |

a. Set to 0 to 'fit' link.

Write access to this device is controlled by the NVM Write Enable Link (E6) and the Software Link EEPROM Write Protection bit in the FPGA Control Register 1 (offset 0x000C).

CAUTION

If the EEPROM DIP switch is used to "fit" the NVM Write Enable Link (E6), then it is not possible to hardware write-protect the Flash and the SSD, since the state of the corresponding links can be changed in software by changing the EEPROM DIP switch. To apply full hardware protection to a board, link E6 must be removed and disabled in the EEPROM DIP switch

### 3.6.6 Real Time Clock

The IMP3A provides an Epson RX8581 RTC, which has a minimum of 1 second resolution. This device can be powered from the +3.3 V backplane supply or the RTC_STDBY signal (J2 connector pin C14) when the main power supply is removed (the voltage on this pin can be between 1.8 V and 5.5 V). The interrupt output of the RTC can generate an interrupt to either processor core, via the FPGA.

### 3.6.7 Power Monitor/Manager

See section 3.7.

## 3.7 Power Manager

The IMP3A uses a Lattice POWR1014A programmable power manager to control all of the on-board power supplies to meet supply sequencing requirements.

In addition to controlling the on-board supply, the power manager also monitors each rail, and its voltage can be read from registers internal to the device, across the $I^2C$ interface. The following table lists the software monitor points.

Table 3-15 Power Manager Monitor Points

| Monitor Point | Supply Name | Nominal Voltage |
|---|---|---|
| VMON1 | VCC | 5 V (backplane) |
| VMON2 | P3V3_BP | 3.3 V (backplane) |
| VMON3 | P3V3 | 3.3 V |
| VMON4 | VCORE | 1.05 V |
| VMON5 | P1V8 | 1.8 V |
| VMON6 | P1V5 | 1.5 V |
| VMON7 | RTC_STDBY | 1.8 V to 5.5 V |
| VMON8 | VCC_PMC | 5 V |
| VMON9 | PMC_VIO | 3.3 V or 5 V |
| VMON10 | CPCI_VIO | 3.3 V or 5 V |

The Power Manager drives a green Power Good LED when all on-board power supplies are within tolerance. See the LEDs section.

## 3.8 Timers

The P2020 provides eight 32-bit general-purpose timers capable of generating interrupts to the processor. These are organized in two groups of 4 timers. Each group can be set to operate from a divider of the CCB clock (divide by 8, 16, 32 or 64) or from an on-board 14.318 MHz clock.

Each group of timers can be cascaded to form two 63-bit timers, one 95-bit timer or one 127-bit timer, if required. (The cascade process uses one bit of one of the 32-bit registers involved, hence the number of available bits being 1 less than might be expected.)

The FPGA provides two programmable 32-bit Watchdog timers, which can generate interrupts to the processor and reset the board if expired. See the FPGA Watchdog Timers section for more details.

## 3.9 Resets, Interrupts & Error Reporting

The P2020's Programmable Interrupt Controller controls resets and interrupts to the processing cores. The following table shows the various external interrupt sources to the PIC and their relative priorities. It also shows whether the previous state of the processor is recoverable.

Table 3-16 External Interrupt Inputs to the P2020

| Priority | Interrupt | Cause | Recoverability |
|---|---|---|---|
| 0 | Hard Reset | Power On, Hard Reset input | Non-recoverable |
| 1 | Machine Check | Machine Check Input (MCP#) | Non-recoverable, most cases |
| 2 | Soft Reset | Soft Reset input | Recoverable unless Machine Check occurs |
| 3 | Debug | UDE# input (unused) | Recoverable unless Machine Check or System Reset occurs |
| 4 | External | INT# input | |

The FPGA contains all of the required logic for resets and interrupts.

### 3.9.1 Hard Reset

The Local Bus FPGA generates an on-board reset signal, which is used to reset the P2020 (including the processing cores) and all other devices on the board that require resetting. This signal is asserted when any of the following events occur:

- POWER_GOOD# signal is negated
- Reset from the backplane (RST# on J1 pin C5) is asserted (if the IMP3A is in Peripheral mode)
- Push-button reset from the backplane (PRST# on J2 pin C17) is asserted (if the IMP3A is in the System Controller slot)
- CPU_HRESET_REQ# output is asserted
- COP HRESET# signal (P17 pin 5) is asserted
- Watchdog timer expired
- Software Hard Reset request generated by writing to bit 7 of the FPGA Power-On Configuration Control Register (offset 0x0070)
- Push-button reset from the TAC is asserted

The duration of the reset signal is at least 10ms. If the IMP3A is in the System Controller slot, then a hard reset event drives the CPCI backplane reset signal.

The FPGA latches the cause of a hard reset and displays it in the Configuration Register 1 (offset 0x0008) so that software may determine the reset cause.

### 3.9.2 Machine Check

The FPGA is able to assert the MCP# Machine Check signal to each processing core individually in response to any board interrupt input to the device or internal source. The routing between these interrupts and either MCP output is programmable by software through the FGPA MCP0 Interrupt Mask Register (offset 0x002C) and MCP1 Interrupt Mask Register (offset 0x0030). These interrupts are disabled by default.

### 3.9.3 Soft Reset

The FPGA drives the SRESET# input to the P2020 when the COP SRESET# signal (P17 pin 7) is asserted.

### 3.9.4 Debug Interrupts

The UDE# inputs to the P2020 are not used on the IMP3A and are pulled to their inactive state.

### 3.9.5 External Interrupts

**PCI Interrupts**

Legacy PCI interrupts from the PMC site and the CPCI backplane can optionally have their interrupts connected directly to the P2020 PIC instead of their respective PCIe to PCI bridge. This is achieved by configuring the board so that the signals are routed to one destination and not the other. As the internal INTx interrupts are shared with the IRQ pins, this configuration has no effect on software. This approach allows flexible routing of PCI interrupts and removal of latency and non-determinism associated with the use of PCI Express legacy INTx messages.

When the IMP3A is in a peripheral slot, the CPCI interrupts are automatically connected to the PI7CX110 bridge because the PI7CX110 needs to generate the interrupt signals when it is a peripheral. A special test mode is available via the FPGA Control register 1 (offset 0x000C) that allows software to override this automatic connection and connect the interrupts to the P2020 when the IMP3A is in a peripheral slot. Although this disables the ability to generate interrupts, it does allow the IMP3A to monitor all system interrupts.

Table 3-17 PCI Interrupt Mapping

| PCI Bus | INTx | Optionally Connected To |
|---|---|---|
| CPCI (PCIe port 1) | INTA | IRQ0 |
| | INTB | IRQ1 |
| | INTC | IRQ2 |
| | INTD | IRQ3 |
| PMC site (PCIe port 3) | INTA | IRQ8 |
| | INTB | IRQ9 |
| | INTC | IRQ10 |
| | INTD | IRQ11 |

NOTE

IRQ4 and IRQ5 are used by the SATA device for legacy interrupt messages for PCIe Port 2 and so are not used as external interrupts.

### FPGA Interrupts

The FPGA connects to the IRQ6 and IRQ7 interrupt inputs of the P2020 (each core has its own interrupt input to support AMP mode operation). These are configured as active-low, level-sensitive.

The FPGA provides the option to route the following internal and external interrupt sources to the interrupt outputs under software control (via the Core 0 Interrupt Mask Register at offset 0x0024 and the Core 1 Interrupt Mask Register at offset 0x0028):

- Watchdog Timer interrupts
- PHY interrupts
- RTC interrupt
- Temperature interrupts
- GPIO interrupts

The FPGA can also route any of these interrupts to either of the MCP inputs to the P2020 via the MCP0 Interrupt Mask Register (offset 0x002C) and MCP1 Interrupt Mask Register (offset 0x0030).

The FPGA allows the processor to determine the source of the interrupt by reading the Interrupt Status Register (offset 0x0020).

## 3.10 FPGA

The FPGA, which is connected to the Local bus, provides the flowing functions:

- Board Control/Status registers
- Two Watchdog timers
- GPIO controller
- Reset logic
- Local bus address generation
- Secondary interrupt controller
- Ancillary board functions
- Scratchpad RAM

Various register bits within the FPGA are classed as ‘sticky’. These are bits that can survive reset if the reset source is a software generated reset via the Software Hard Reset Request bit contained within the Power-On Configuration Control register. If the reset source is anything other than the Software Hard Reset Request control bit then the ‘sticky’ bits are reset to their default value.

## 3.11 FPGA Board Control and Status Registers

The FPGA provides several registers, accessed using CS4, to provide software with information on the configuration of the IMP3A. These are shown in the following table:

Table 3-18 Control and Status Registers

| Offset | Register | Read/Write |
|---|---|---|
| 0x0000 | Board ID 1 | Read only |
| 0x0002 | Board ID 2 | Read only |
| 0x0004 | Device/Bus 1 | Read only |
| 0x0006 | Device/Bus 2 | Read only |
| 0x0008 | Configuration 1 | Read only |
| 0x000A | Configuration 2 | Read only |
| 0x000C | Control 1 | Read/write |
| 0x000E | Control 2 | Read/write |
| 0x0010 | Test 1 | Read only |
| 0x0012 | Test 2 | Read only |
| 0x0014 | Test 3 | Read only |
| 0x0016 | Test 4 | Read only |
| 0x0018 | Test 5 | Read only |
| 0x001A | Test 6 | Read only |
| 0x001C | Scratchpad 1 | Read/write |
| 0x001E | Scratchpad 2 | Read/write |
| 0x0020 | Interrupt Status | Read only |
| 0x0030 | Core 0 Interrupt Mask | Read only |
| 0x0034 | Core 1 Interrupt Mask | Read only |
| 0x0038 | MCP0 Interrupt Mask | Read only |
| 0x003C | MCP1 Interrupt Mask | Read only |
| 0x0050 | Flash Addressing Control | Read/write |
| 0x0060 | System Semaphore | Read/write |
| 0x0070 | Power-On Configuration Control | Read/write |
| 0x0A00 | Board Semaphore 1 | Read/write |
| 0x0A02 | Board Semaphore 2 | Read/write |
| 0x0A04 | Board Semaphore 3 | Read/write |
| 0x0A06 | Board Semaphore 4 | Read/write |
| 0x0A08 | Board Semaphore 5 | Read/write |
| 0x0A0A | Board Semaphore 6 | Read/write |
| 0x0A0C | Board Semaphore 7 | Read/write |
| 0x0A0E | Board Semaphore 8 | Read/write |

### 3.11.1 Board ID Register 1 (Offset 0x0000) and Board ID Register 2 (Offset 0x0002)

These allow software to identify the specific board type and version.

Table 3-19 Board ID Register 1

| Bits | Description | Default Value |
|---|---|---|
| 0 to 7 | GEIP Board ID | 0x46 |
| 8 to 15 | PCB major revision (1, 2, 3 etc.) | - |

Table 3-20 Board ID Register 2

| Bits | Description |
|---|---|
| 0 to 7 | Board minor revision (A, B, C etc.) |
| 8 to 15 | Register FPGA revision |

### 3.11.2 Device/Bus Register 1 (Offset 0x0004)

Table 3-21 Device/Bus Register 1

| Bits | Description | Default Value |
|---|---|---|
| 0 | DRAM Controller operating frequency:<br>0 = 800 MHz<br>1 = 666 MHz | |
| 1 | Dual die DRAM devices fitted:<br>0 = Not fitted<br>1 = Fitted | |
| 2 & 3 | DRAM device size (die density):<br>00 = Reserved<br>01 = 4 Gbit<br>10 = 2 Gbit<br>11 = 1 Gbit<br>When dual die devices are fitted (determined by bit 1) the overall density is doubled | |
| 4 | Flash type:<br>0 = Spansion Flash fitted (default)<br>1 = Reserved | 0 |
| 5 | Flash banks fitted:<br>0 = Banks 0 and 1 fitted<br>1 = Reserved | 0 |
| 6 & 7 | Flash device size:<br>00 = 1 Gbit<br>01 = 2 Gbit<br>10 = Reserved<br>11 = Reserved | |
| 8 | PMC VIO signaling voltage:<br>0 = 3.3 V<br>1 = 5 V | |
| 9 to 12 | Reserved | 0000 |
| 13 to 15 | CompactPCI bus speed:<br>000 = 33 MHz<br>001 = 66 MHz<br>Other = Reserved | |

### 3.11.3 Device/Bus Register 2 (Offset 0x0006)

Table 3-22 Device/Bus Register 2

| Bits | Description | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x0 |
| 8 | SSD device fitted.<br>0 = SSD device is present<br>1 = No SSD device present | |
| 9 & 10 | SSD capacity.<br>00 = 4 GBytes<br>01 = 8 GBytes<br>10 = 16 GBytes<br>11 = 32 GBytes | |
| 11 | System Controller identifier:<br>0 = Board in Peripheral slot<br>1 = Board in System slot (system controller functions enabled) | |
| 12 to 15 | CompactPCI geographical address | |

### 3.11.4 Configuration Register 1 (Offset 0x0008)

Table 3-23 Configuration Register 1

| Bit | Description | Default Value |
|---|---|---|
| 0 | Reset monitor - P2020 reset:<br>0 = Last reset was not P2020 reset<br>1 = Last reset was P2020 reset | |
| 1 | Reset monitor - Backplane reset:<br>0 = Last reset was not X110 PCI bridge<br>1 = Last reset was X110 PCI bridge | |
| 2 | Reset monitor - Push-button reset (only valid if the IMP3A is in the System Controller slot):<br>0 = Last reset was not PRST# or Reset switch on TAC<br>1 = Last reset was PRST# or Reset switch on TAC | |
| 3 | Reset monitor - Watchdog timer 1:<br>0 = Last reset was not watchdog timer 1<br>1 = Last reset was watchdog timer 1 | |
| 4 | Reset monitor - Watchdog timer 2:<br>0 = Last reset was not watchdog timer 2<br>1 = Last reset was watchdog timer 2 | |
| 5 | Reset monitor - Software reset [write to Power-on Configuration Control Register (offset0x0070)]<br>0 = Last reset was not software reset<br>1 = Last reset was software reset | 0 |
| 6 | NVM Write Enable Link (E6) setting:<br>0 = Link not fitted<br>1 = Link fitted | |
| 7 | SSD Write Protect Link (E8) setting.<br>0 = Link not fitted<br>1 = Link fitted | |
| 8 | BIT Fast Start:[a]<br>0 = Disabled<br>1 = Enabled | |

Table 3-23 Configuration Register 1

| Bit | Description | Default Value |
|---|---|---|
| 9 | Backplane Programming Mode Link setting:<br>0 = Link not fitted<br>1 = Link fitted (board is in backplane program mode) | |
| 10 | Recovery Link (E5) setting:<br>0 = Link not fitted<br>1 = Link fitted | |
| 11 | Core 0 Boot Area Select Link (E1) setting:<br>0 = Link not fitted<br>1 = Link fitted | |
| 12 | Core 1 Boot Area Select Link (E3) setting:<br>0 = Link not fitted<br>1 = Link fitted | |
| 13 | JTAG Scanbridge Output Enable Link (E2) setting:<br>0 = Link not fitted<br>1 = Link fitted | 0 |
| 14 | BANC Area Write Enable Link setting:<br>0 = Link not fitted<br>1 = Link fitted | |
| 15 | Flash Protection Unlock Link (E4) setting:<br>0 = Link not fitted and backplane FLASH_WE# signal (J2 pin B4) is high<br>1 = Link fitted or backplane FLASH_WE# signal (J2 pin B4) is low | |

a.The hardware input for BIT fast start is shared with GPIO(0). BIT software determines whether this bit is valid or not.

### 3.11.5 Configuration Register 2 (Offset 0x000A)

Table 3-24 Configuration Register 2

| Bits | Description | Default Value |
|---|---|---|
| 0 to 3 | Reserved | 0x0 |
| 4 | PMC EREADY status:<br>0 = PMC is not ready to be enumerated<br>1 = PMC is ready to be enumerated | |
| 5 | Additional GPIO build option:<br>0 = No additional GPIO (PMCIO[43:46] is present)<br>1 = GPIO(12:15) routed to backplane (PMCIO[43:46] is not available) | |
| 6 | COM1 build option:<br>0 = COM1 is RS232 only<br>1 = COM1 is RS232 and RS422 capable | |
| 7 | SATA channel 1 build option:<br>0 = Build option not fitted<br>1 = Build option fitted | |
| 8 | SATA channel 0 build option:<br>0 = Build option not fitted<br>1 = Build option fitted | |
| 9 | USB build option:<br>0 = Build option not fitted<br>1 = Build option fitted | |
| 10 | Peripheral only build option:<br>0 = Build option not fitted - PMC I/O 1:49 available<br>1 = Build option fitted - PMC I/O 1:64 available | |
| 11 and 12 | Reserved | 00 |
| 13 | Ethernet channel 0 configuration:<br>0 = 1000BaseT capable<br>1 = 10/100BaseT | |
| 14 | Ethernet channel 1 configuration:<br>0 = 1000BaseT capable<br>1 = 10/100BaseT | |
| 15 | PMC fitted:<br>0 = PMC not fitted<br>1 = PMC fitted | |

### 3.11.6 Control Register 1 (Offset 0x000C)

Table 3-25 Control Register 1

| Bits | Description | Default Value |
|---|---|---|
| 0 to 2 | Reserved | 0x0 |
| 3 | Software Link EEPROM write protection[a]:<br>0 = Software Link EEPROM is write enabled[b]<br>1 = Software Link EEPROM is write protected | 1 |
| 4 | CPCI interrupt routing:<br>When Peripheral card:<br>0 = CPCI interrupts connected to P2020 PIC (test mode to allow monitoring of backplane interrupts)<br>1 = CPCI interrupts connected to X110 bridge (normal operation)<br>When System Controller:<br>0 = CPCI interrupts connected to P2020 PIC (read only) | |
| 5 to 14 | Reserved | 0x00 |
| 15 | Configuration EEPROM write protection[ac]:<br>0 = Configuration EEPROM devices write enabled[b]<br>1 = Configuration EEPROM devices write protected | 1 |

a.This bit can only be set low when the NVM Write Enable Link (E6) is fitted.
b.This bit is forced to a '0' when the IMP3A is in Recovery mode or external program mode.
c. This controls write protection for the P2020 EEPROM, P17CX110 EEPROM and P17C9X130 EEPROM.

### 3.11.7 Control Register 2 (Offset 0x000E)

Table 3-26 Control Register 2

| Bits | Description | Default Value |
|---|---|---|
| 0 | BIT Pass LED:<br>0 = LED off<br>1 = LED on | 0[a] |
| 1 | BIT LED 1:<br>0 = LED off<br>1 = LED on | 0[a] |
| 2 | BIT LED 2:<br>0 = LED off<br>1 = LED on | 0[a] |
| 3 | BIT Fail LED:<br>0 = LED off<br>1 = LED on | 1[a] |
| 4 | COM1/COM2 transceiver loopback mode:<br>0 = Disabled<br>1 = Enabled | 0 |
| 5 to 8 | Reserved | 0x0 |
| 9 | COM2 mode:<br>0 = RS232<br>1 = RS422 | 0 |
| 10 and 11 | Reserved | 00 |
| 12 | Spread Spectrum clock mode enable:<br>0 = PCIe Reference clocks in normal clocking mode<br>1 = PCIe Reference clocks in Spread-Spectrum mode | 0 |
| 13 | Reserved | |
| 14 | COM1 mode[b]:<br>0 = RS232<br>1 = RS422 | |
| 15 | COM1/2 transceiver enable:<br>0 = Transceiver disabled<br>1 = Transceiver enabled | |

a. 'Sticky' bit (see earlier).
b. This bit is interlocked with the COM1 Build Option bit in the Configuration Register 2 (offset 0x000A). It cannot be set for RS422 if the COM1 build option = RS232.

### 3.11.8 Test Registers

The following table shows the 16-bit test registers with their offsets, their values when the Flash Protection Unlock Link (E4) is fitted (or the backplane FLASH_WE~ signal [J2 pin B4] is active), their values when the Flash Protection Unlock Link (E4) is not fitted (and the backplane FLASH_WE# signal [J2 pin B4] is inactive) and their value on reset:

Table 3-27 Test Registers

| Register | Offset | Link Fitted | Test Pattern | Default Value |
|---|---|---|---|---|
| Test 1 | 0x0010 | Password byte 1 | 0xAAAA | - |
| Test 2 | 0x0012 | Password byte 0 | 0xAAAA | - |
| Test 3 | 0x0014 | Password byte 3 | 0x5555 | - |
| Test 4 | 0x0016 | Password byte 2 | 0x5555 | - |
| Test 5 | 0x0018 | - | 0x3341 (“3A”) | 0x3341 (“3A”) |
| Test 6 | 0x001A | - | 0x4950 (“IP”) | 0x4950 (“IP”) |

### 3.11.9 Scratchpad Registers

These are two 16-bit general purpose registers. Both have a value of 0x0000 on reset. Scratchpad Register 1 is at an offset of 0x001C and Scratchpad Register 2 is at an offset of 0x001E.

### 3.11.10 Interrupt Status Register (Offset 0x0020)

This register returns the status of all interrupt sources handled by the secondary interrupt controller. For each source, a value of 0 in the corresponding bit of this register means that the interrupt is de-asserted, and a value of 1 means that an interrupt is asserted.

Table 3-28 Interrupt Status Register

| Bits | Source | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 | GPIO controller | |
| 9 | Watchdog timer 1 | |
| 10 | Watchdog timer 0 | |
| 11 | Ethernet Phy 2 | |
| 12 | Ethernet Phy 1 | |
| 13 | Core and board critical temperature | |
| 14 | Core and board temperature | |
| 15 | RTC | |

### 3.11.11 Core 0 Interrupt Mask Register (Offset 0x0030)

This register controls which interrupt sources generate a core 0 interrupt (P2020 IRQ6). For each source, a value of 0 in the corresponding bit of this register means that the interrupt is masked, and a value of 1 means that the interrupt is enabled.

Table 3-29 Core 0 Interrupt Mask Register

| Bits | Source | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 | GPIO | |
| 9 | Watchdog timer 1 | |
| 10 | Watchdog timer 0 | |
| 11 | Ethernet Phy 2 | |
| 12 | Ethernet Phy 1 | |
| 13 | Critical Temperature | |
| 14 | Temperature | |
| 15 | RTC | |

### 3.11.12 Core 1 Interrupt Mask Register (Offset 0x0034)

This register controls which interrupt sources generate a core 0 interrupt (P2020 IRQ7). For each source, a value of 0 in the corresponding bit of this register means that the interrupt is masked, and a value of 1 means that the interrupt is enabled.

Table 3-30 Core 1 Interrupt Mask Register

| Bits | Source | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 | GPIO | |
| 9 | Watchdog timer 1 | |
| 10 | Watchdog timer 0 | |
| 11 | Ethernet Phy 2 | |
| 12 | Ethernet Phy 1 | |
| 13 | Critical Temperature | |
| 14 | Temperature | |
| 15 | RTC | |

### 3.11.13 MCP0 Interrupt Mask Register (Offset 0x0038)

This register controls which interrupt sources generate an MCP0 interrupt to the P2020. For each source, a value of 0 in the corresponding bit of this register means that the interrupt is masked, and a value of 1 means that the interrupt is enabled.

Table 3-31 MCP0 Interrupt Mask Register

| Bits | Source | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 | GPIO | |
| 9 | Watchdog timer 1 | |
| 10 | Watchdog timer 0 | |
| 11 | Ethernet Phy 2 | |
| 12 | Ethernet Phy 1 | |
| 13 | Critical Temperature | |
| 14 | Temperature | |
| 15 | RTC | |

### 3.11.14 MCP1 Interrupt Mask Register (Offset 0x003C)

This register controls which interrupt sources generate an MCP1 interrupt to the P2020. For each source, a value of 0 in the corresponding bit of this register means that the interrupt is masked, and a value of 1 means that the interrupt is enabled.

Table 3-32 MCP1 Interrupt Mask Register

| Bits | Source | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 | GPIO | |
| 9 | Watchdog timer 1 | |
| 10 | Watchdog timer 0 | |
| 11 | Ethernet Phy 2 | |
| 12 | Ethernet Phy 1 | |
| 13 | Critical Temperature | |
| 14 | Temperature | |
| 15 | RTC | |

### 3.11.15 Flash Addressing Control Register (Offset 0x0050)

This register controls the Flash addressing. The addressing bits allow software to page Flash to avoid having to map the entire array into the memory map and to allow a large amount of Flash to be accessed via a small memory window.

Table 3-33 Flash Addressing Control Register

| Bits | Description | Default Value |
|---|---|---|
| 0 to 3 | Reserved | 0x0 |
| 4 | MAC mirror mode:<br>0 = CS2 top sector accesses Flash Bank 1<br>1 = CS2 top sector accesses Flash Bank 0 (BANC area) | 1 |
| 5 | Reserved | 0 |
| 6 | Core 1 boot mode:<br>0 = Primary (core 0) boot area mapped to 0xFF80 0000<br>1 = Secondary (core 1) boot area mapped to 0xFF80 0000 | 0 |
| 7 | Page mode enable:<br>0 = Flash address derived from local bus<br>1 = Flash Address bits 1:4 derived from registers | 1 |
| 8 and 9 | Reserved | 00 |
| 10 and 11 | Flash address bits 28:27 (CS2 space[a, b])<br>When the Page Mode Enable bit (D7) is set, these bits provide the two most significant bits of the Flash address to select a 128 MByte page | 11 |
| 12 | Reserved | 0 |
| 13 to 15 | Flash address bits 29:27 (CS1 space[b])<br>When the Page Mode Enable bit (D7) is set, these bits provide the three most significant bits of the Flash address to select a 128 MByte page | 111 |

a. It is only possible to access the lower half of the Flash using CS2. The exception to this is when the MAC Mirror Mode bit (D4) is set
b. The CS1 paging requires 3 bits because CS1 can access all of the Flash. The CS2 paging requires 2 bits because CS2 can only access the lower half of Flash.

### 3.11.16 System Semaphore Register (Offset 0x0060)

This register is mapped into PCI memory space so that any board in the system can access it. To take the semaphore, a board writes its slot ID into this register.

Table 3-34 System Semaphore Register

| Bits | Description | Default Value |
|---|---|---|
| 0 to 11 | Reserved | 0x000 |
| 12 to 15 | Semaphore value (the slot number of the board that took the semaphore) | 0x0 |

This register can be accessed by the IMP3A using CS5.

### 3.11.17 Power-On Configuration Control Register (Offset 0x0070)

This register provides a way for software such as BIT to exit cleanly to another piece of software, such as VxWorks. A status value that is passed between the software domains may be written to this register, and a full board reset that places all the hardware into a known state may be generated.

This register contains four 'sticky' register bits that make up part of the power-on reset configuration value that the P2020 takes in on the local address/data bus and stores in the General-Purpose POR Configuration Register (GPPORCR) within the processor. If these bits in the GPPORCR are zero, then the software knows that the IMP3A has just been reset by hardware.

Table 3-35 Power-On Configuration Control Register

| Bits | Description | Default Value |
|---|---|---|
| 0 to 6 | Reserved | 0x00 |
| 7 | Software Hard Reset Request<br>1 = Generate a hard reset to the IMP3A (all hardware except 'sticky' bits within the FPGA will be reset)[a] | 0 |
| 8 to 11 | Reserved | 0x0 |
| 12 to 15 | General purpose s/w configuration value[b] | 0 |

a. This bit will self-clear to '0' during the reset event.
b. 'Sticky' bits (see earlier).

This register can be accessed by the IMP3A using CS4.

### 3.11.18 Semaphore Registers

A semaphore is taken by reading the appropriate register. If the value returned is zero, then the semaphore is currently in use; if the value returned is non-zero, then the semaphore take is successful. A semaphore is released by writing to the appropriate register (the value written is not significant).

Table 3-36 Semaphore Registers

| Register | Offset | Default Value |
|---|---|---|
| Semaphore 1 | 0xA00 | 0x0000 |
| Semaphore 2 | 0xA02 | 0x0000 |
| Semaphore 3 | 0xA04 | 0x0000 |
| Semaphore 4 | 0xA06 | 0x0000 |
| Semaphore 5 | 0xA08 | 0x0000 |
| Semaphore 6 | 0xA0A | 0x0000 |
| Semaphore 7 | 0xA0C | 0x0000 |
| Semaphore 8 | 0xA0E | 0x0000 |

## 3.12 GPIO Controller

The FPGA provides sixteen bits of GPIO. Each bit can be independently configured as either input or output, depending on the state of the corresponding bit in the Direction Register.

When configured as inputs, each bit is capable of generating a processor interrupt using either edge detection (high, low or both edges) or by level detection (either active high or active low). When an interrupt event occurs, the GPIO bit is set in the Board Interrupt Status register and the corresponding bit in the GPIO Interrupt Status Register is set to a '1' to indicate the bit of the port on which the event occurred.

When configured as an output, each bit can be programmed to be either Open drain output or totem-pole output.

There are several build options on the IMP3A that affect which GPIO bits are available at the J2 connector. See the General Purpose I/O section for more details. To aid software in determining which bits are available, the Presence register indicates which bits are routed to the connector.

The FPGA provides several GPIO control and status registers, accessed using CS4. These are shown in the following table:

Table 3-37 GPIO Registers

| Offset | Register | Read/Write | Default Value |
|---|---|---|---|
| 0x0400 | GPIO Direction | Read/write | 0xFFFF |
| 0x0404 | GPIO Data In | Read only | - |
| 0x0408 | GPIO Data Out | Read/write | 0x0000 |
| 0x040C | GPIO Interrupt Sensitivity | Read/write | 0x0000 |
| 0x0410 | GPIO Interrupt Polarity A | Read/write | 0x0000 |
| 0x0414 | GPIO Interrupt Polarity B | Read/write | 0x0000 |
| 0x0418 | GPIO Interrupt Status | Read/write | - |
| 0x0420 | GPIO Output Mode | Read/write | 0x0000 |
| 0x0424 | GPIO Interrupt Enable | Read/write | 0x0000 |
| 0x0428 | GPIO Presence | Read only | - |

### 3.12.1 GPIO Direction Register (Offset 0x0400)

Bits 0 to 15 of this register show the direction of the corresponding GPIO line (0 to 15), where:

0 = Output
1 = Input

### 3.12.2 GPIO Data In Register (Offset 0x0404)

Bits 0 to 15 of this register return the value on the corresponding pin (0 to 15) of the device, regardless of whether that line is set as an input or output. Each bit is triple-clocked into the device to protect against metastability and to provide an edge-detection mechanism. The value may be:

0 = Low voltage on the pin
1 = High voltage on the pin

### 3.12.3 GPIO Data Out Register (Offset 0x0408)

This register contains the values that are driven onto those pins of the device for which the corresponding Direction bit is 0 (output) (where bits 0 to 15 of this register correspond to pins 0 to 15 of the device respectively). The value may be:

0 = Line driven low
1 = Line driven high

### 3.12.4 GPIO Interrupt Sensitivity Register (Offset 0x040C)

This register configures the interrupt mode of a GPIO line (where bits 0 to 15 of this register correspond to lines 0 to 15 respectively). The value of a bit may be:

0 = Level sensitive
1 = Edge sensitive

Interrupts are only generated when a GPIO line is set as an input.

### 3.12.5 GPIO Interrupt Polarity Register A (Offset 0x0410)

This register configures the polarity of the interrupt mode of a GPIO line (where bits 0 to 15 of this register correspond to lines 0 to 15 respectively).

When a line is level sensitive, the value of a bit may be:

0 = Generate interrupt on low
1 = Generate interrupt on high

When a line is edge sensitive, the value of a bit may be:

0 = As per GPIO Polarity Register B (0ffset 0x0414)
1 = Generate interrupt on either edge

### 3.12.6 GPIO Interrupt Polarity Register B (Offset 0x0414)

This register configures the polarity of the interrupt mode of a GPIO line when in Edge Sensitive mode (where bits 0 to 15 of this register correspond to lines 0 to 15 respectively). The value of a bit may be:

0 = Generate interrupt on a low to high transition
1 = Generate interrupt on a high to low transition

### 3.12.7 GPIO Interrupt Status Register (Offset 0x0418)

This register shows the status of interrupts on the GPIO lines (where bits 0 to 15 of this register correspond to lines 0 to 15 respectively). The value of a bit may be:

0 = No interrupt pending
1 = Interrupt pending

Any bit being set in this register causes the GPIO bit in the main Interrupt Status Register to be set.

A bit is set in this register under the following circumstances:

In Level mode (i.e. when the corresponding bit is '0' at offset 0x040C):
When set for 'interrupt on low' (i.e. the corresponding bit is '0' at 0x0410) and that GPIO line is low (0).
When set for 'interrupt on high' (i.e. the corresponding bit is '1' at 0x0410) and that GPIO line is high (1).

In Edge mode (i.e. when the corresponding bit is '1' at offset 0x040C):
When set for 'interrupt on low to high transition' (i.e. the corresponding bits are '0' at 0x0410 and 0x0414) and that GPIO line has gone from low to high.
When set for 'interrupt on high to low transition' (i.e. the corresponding bit is '0' at 0x0410 and '1' at 0x0414) and that GPIO line has gone from high to low.
When set for 'interrupt on either edge' (i.e. the corresponding bit is '1' at 0x0410) and that GPIO line has gone from high to low or low to high.

Writes to this register have no effect when GPIO is configured for Level Mode. Edge mode interrupts are latched in this register, and can be cleared by writing a '1' to the corresponding bit of this register.

### 3.12.8 GPIO Output Mode Register (Offset 0x0420)

Bits 0 to 15 of this register select the output mode of the corresponding bit of the GPIO port, where:

0 = Totem-pole output
1 = Open drain output

This selection is effective only when the port is configured as an output.

### 3.12.9 GPIO Interrupt Enable Register (Offset 0x0424)

Bits 0 to 15 of this register enable or disable interrupt generation on the corresponding bit of the GPIO port, where:

0 = GPIO bit may not generate an interrupt
1 = GPIO bit may generate an interrupt

### 3.12.10 GPIO Presence Register (Offset 0x0428)

As there are several build options that can determine which GPIO bits are connected to the J2 connector (see the Product Codes section), this register is provided to allow software to determine the actual configuration (it may be used as a mask if required). Bits 0 to 15 show the configuration of the corresponding GPIO bit, where:

0 = GPIO bit is not routed to the backplane J2 connector
1 = GPIO bit is routed to the backplane J2 connector

The value of this register is generated by decoding the various I/O option configuration resistors connected to the FPGA.

## 3.13 Watchdog Timers

The FPGA provides two identical, programmable 32-bit watchdog timers. These are capable of generating interrupts to the processor and resetting the board if expired. The watchdogs are disabled following reset.

Each watchdog timer is a 32-bit count-down counter, clocked by the local bus clock, so the resolution and maximum timeout value depends on the frequency of this clock. Since the local bus clock frequency is set by software, it is advisable that software determines the frequency (by reading the LBCC register) before determining any time-out period settings. The following table shows some example values.

Table 3-38 Watchdog Typical Resolutions and Maximum Timeouts

| Platform (CCB) Frequency (MHz) | Local Bus Frequency (MHz) | Watchdog Resolution (ns) | Watchdog Maximum Timeout (Seconds) |
|---|---|---|---|
| 600 | 37.5 | 27 | 114.5 |
| 500 | 62.5 | 16 | 68.7 |
| 400 | 50 | 20 | 85.9 |

The watchdog counter is enabled/disabled by writing an “01” followed by “10” pattern to the relevant portion of the Control register. The current status of the watchdog can also be read from this register. When enabled or disabled, the counter is reloaded to the preset value and the reset and interrupt bits are cleared (assuming that the preset counter value is higher than the interrupt value).

The period of the counter is programmable. If the counter reaches zero before the watchdog is serviced, then a hard reset is generated. The watchdog is serviced by writing a “01” followed by “10” pattern to the relevant portion of the Control register. This operation clears the interrupt and reset flags, if set, and reloads the counter to the preset value.

A programmable interrupt threshold can be set. If the counter reaches this threshold, then an interrupt is generated to the interrupt controller, which may be routed to either processor core as desired.

The FPGA provides several registers, accessed using CS4, to allow software to control the Watchdogs. These are shown in the following table:

Table 3-39 Watchdog Registers

| Offset | Register | Read/Write | Default Value |
|---|---|---|---|
| 0x0800 | Watchdog 0 Control | Read/write | 0x00FF |
| 0x0802 | Watchdog 0 Preset Value Low | Read/write | 0xFFFF |
| 0x0804 | Watchdog 0 Interrupt Threshold High | Read/write | 0x0000 |
| 0x0806 | Watchdog 0 Interrupt Threshold Low | Read/write | 0x0000 |
| 0x0808 | Watchdog 1 Control | Read/write | 0x00FF |
| 0x080A | Watchdog 1 Preset Value Low | Read/write | 0xFFFF |
| 0x080C | Watchdog 1 Interrupt Threshold High | Read/write | 0x0000 |
| 0x080E | Watchdog 1 Interrupt Threshold Low | Read/write | 0x0000 |

### 3.13.1 Watchdog Control Registers

These registers control the operation of the corresponding Watchdog. They are at offsets of 0x0800 for Watchdog 0 and 0x0808 for Watchdog 1.

Table 3-40 Watchdog Control Registers

| Bits | Description | Default Value |
|---|---|---|
| 0 | Watchdog status:<br>0 = Watchdog disabled<br>1 = Watchdog enabled | 0 |
| 1 | Watchdog expiry:<br>0 = Watchdog not expired<br>1 = Watchdog counter expired (reset) | 0 |
| 2 | Watchdog interrupt:<br>0 = Watchdog interrupt inactive<br>1 = Watchdog interrupt active | 0 |
| 3 | Reserved | 0 |
| 4 and 5 | Service Watchdog<br>To services the watchdog timer, write “01” followed by “10” to these bits | 00 |
| 6 and 7 | Enable Watchdog<br>To enable/disable the watchdog timer, write “01” followed by “10” to these bits | 00 |
| 8 to 15 | Watchdog Preset Value High<br>Bits 31 to 24 of the value that is loaded by the 32-bit Watchdog counter whenever it is enabled or serviced | 0xFF |

### 3.13.2 Watchdog Preset Value Low Registers

These 16-bit registers contain bits 23 to 8 of the value that is loaded by the corresponding 32-bit Watchdog counter whenever it is enabled or serviced. Bits 7 to 0 of the value loaded by the Watchdog counter are always 0xFF.

The registers are at offsets of 0x0802 for Watchdog 0 and 0x080A for Watchdog 1.

### 3.13.3 Watchdog Interrupt Threshold High Registers

These registers contain bits 23 to 16 of the count value at which an interrupt is generated. Bits 31 to 24 are always 0x00.

The registers are at offsets of 0x0804 for Watchdog 0 and 0x080C for Watchdog 1.

Table 3-41 Watchdog Interrupt Threshold High Register

| Bits | Description | Default Value |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 to 15 | Interrupt threshold high | 0x00 |

### 3.13.4 Watchdog Interrupt Threshold Low Register (Offset 0x0)

These registers contain bits 15 to 0 of the count value at which an interrupt is generated. The registers are at offsets of 0x0806 for Watchdog 0 and 0x080E for Watchdog 1.

## 3.14 JTAG

### 3.14.1 Boundary Scan

The IMP3A provides JTAG boundary scan facilities for all IEEE1149.1 and IEEE1149.6-compliant devices. A JTAG Scanbridge device is used to partition the JTAG chain to aid debugging, as shown in the following table. The primary interface to the Scanbridge chain is available from the standard pins on the J1 connector, and from the TAC.

NOTE
The Scanbridge is only available when link E2 is fitted, either by jumper or via the software links EEPROM.

Table 3-42 On-board JTAG Chains

| Test Access Point | Device(s) |
|---|---|
| TAP1 | P2020 |
| TAP2 | Gigabit Ethernet Phys 0 and 1 |
| TAP3 | PCIe to PCI and PCIe to PCI-X bridges |
| TAP4 | SATA |
| TAP5 | PMC site |
| TAP6 | FPGA, Clock Generator |

The JTAG architecture supports the use of the JTAG Technologies Autowrite signal to accelerate Flash programming via JTAG. This signal is on J1 pin A5.

NOTE
This is a build option. Consult the factory if this option is required.

The address of the JTAG Scanbridge on the backplane is the CPCI geographic address (visible in the FPGA Device/Bus Register 2, offset 0x0006). This is used when operating a bused JTAG system with multiple boards.

The USR_STATUS_BYTE register in the Scanbridge (accessible through the primary TAP) has the format shown in the following table:

Table 3-43 USR_STATUS_BYTE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | | 1 | 1 | 1 | 0 | 0 | 1 |
| PMC2 | PMC1 | AFIX | | | ID | | |

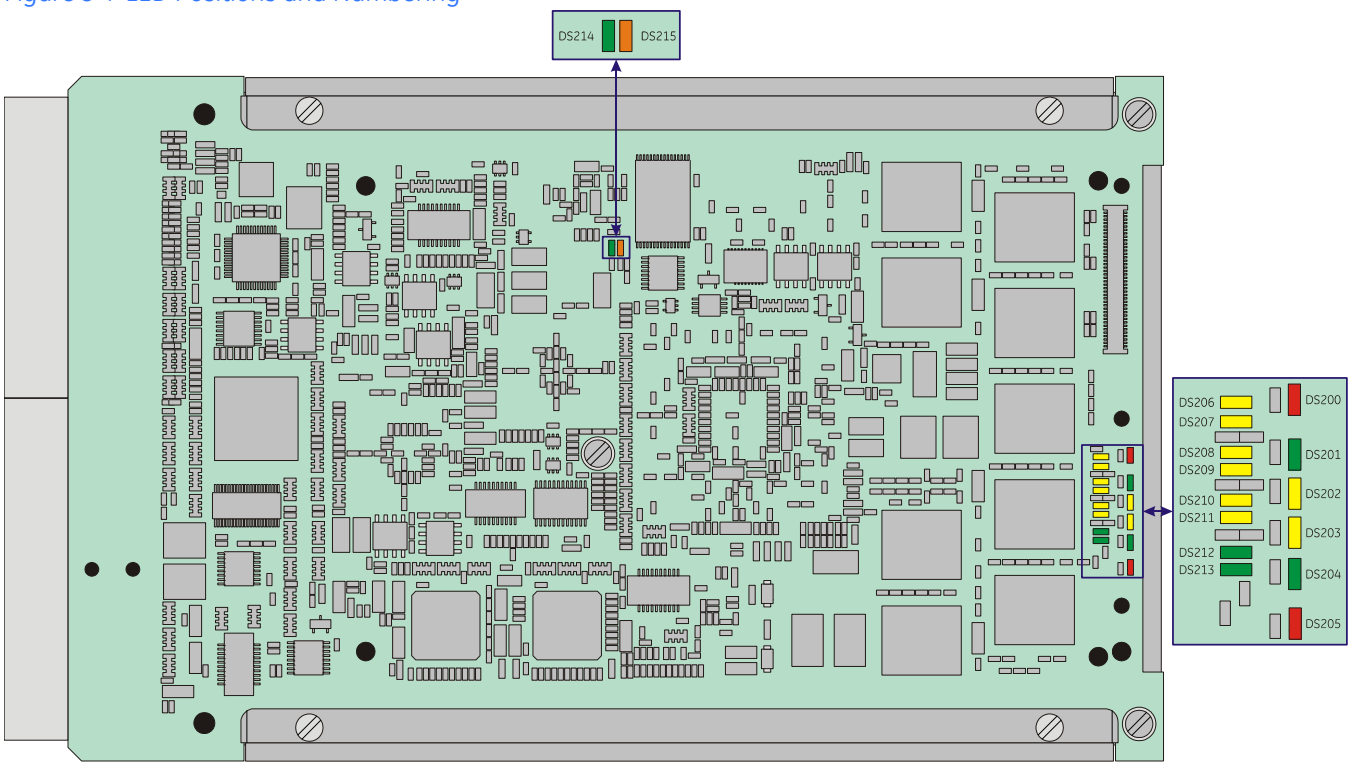
The GEIP card ID is 25 (0x19).
Bits 7 to 5 are used to determine what mezzanine cards are fitted to the IMP3A as follows:
bit 7 = Mezzanine 2 (only 1 mezzanine on IMP3A, so always 1),
bit 6 = Mezzanine 1 (0 when PMC fitted, 1 when removed),
bit 5 = AFIX card fitted (no AFIX capability on IMP3A, so always 1).

### 3.14.2 P2020 BDM Access

Access to the P2020 JTAG port is also possible via a BDM header situated on the Test Access Card. If this is being used, ensure that the Scanbridge is disabled by removing link E2.

## 3.15 LEDs

Figure 3-7 LED Positions and Numbering




### 3.15.1 Power Good LED (DS200)

This green LED is driven by the Power Manager to indicate that all on-board power supplies are within tolerance. This LED is visible on the front panel.

### 3.15.2 BIT LEDs (DS201 to DS204)

The IMP3A has four LEDs (1 red, 2 yellow and 1 green) to reflect the status of BIT or other boot firmware.

The red LED (DS201) is lit after reset and normally indicates a BIT failure if it remains lit. The two yellow LEDs (DS202 and DS203) are unlit after reset and are software driven (BIT may use them to show test progress). The green LED (DS204) is also unlit after reset and software driven. When controlled by BIT, it is normally lit to indicate BIT pass.

Once BIT or other boot firmware has finished with these LEDs, they are free for application use. They can be controlled via the FPGA Control Register 2 (offset 0x000E).

NOTE

As these LEDs are controlled by 'sticky' bits, they retain their lit/unlit states on a software reset, but revert to the default states on a hardware reset.

The BITFAIL# backplane signal (J2 pin D14, when available) is driven active low using an open-drain driver when the red LED is lit.

### 3.15.3 Board Reset LED (DS205)

The main board reset signal drives a red LED to show that the board is in reset.

### 3.15.4 Ethernet Link Status LEDs (DS206 to DS209)

Each of the Marvell 88E1119R Phys has an LED driver to indicate the link status. Each Ethernet link has two yellow LEDs to show the status of the link, as shown in the following table:

Table 3-44 Ethernet Link Status LEDs

| Phy | Associated LEDs | Meaning When Flashing[a] | Meaning When Lit | Meaning When Off |
|---|---|---|---|---|
| 0 | DS207 | 3 flashes = 1000BaseT link speed<br>2 flashes = 100BaseT link speed<br>1 flash = 10BaseT link speed | - | No link |
| | DS206 | Link activity | Link present | No link |
| 1 | DS209 | 3 flashes = 1000BaseT link speed<br>2 flashes = 100BaseT link speed<br>1 flash = 10BaseT link speed | - | No link |
| | DS208 | Link activity | Link present | No link |

a. When powered-on or rest, the LED is off for about 0.5 seconds, then flashes according to the negotiated link speed.

### 3.15.5 SATA Link Status LEDs (DS210 and DS211)

The Sil3132 SATA device has LED drivers to indicate activity on each SATA link. A yellow LED is connected to each channel's LED output. DS210 shows SATA activity for channel 0 and DS211 shows SATA activity for channel 1.

### 3.15.6 CPU Status LEDs (DS212 and DS213)

Green LEDs are connected to the 'Ready' outputs of the P2020 to show that the corresponding core has emerged from reset and is not in a low power mode. DS213 is connected to the READY_P0 output and DS212 is connected to the READY_P1 output.

### 3.15.7 SSD Status LEDs (DS214 and DS215)

A green LED (DS214) is lit when the SATA link between the SSD and the SATA controller is valid. An amber LED (DS215) flashes to indicate SSD activity.

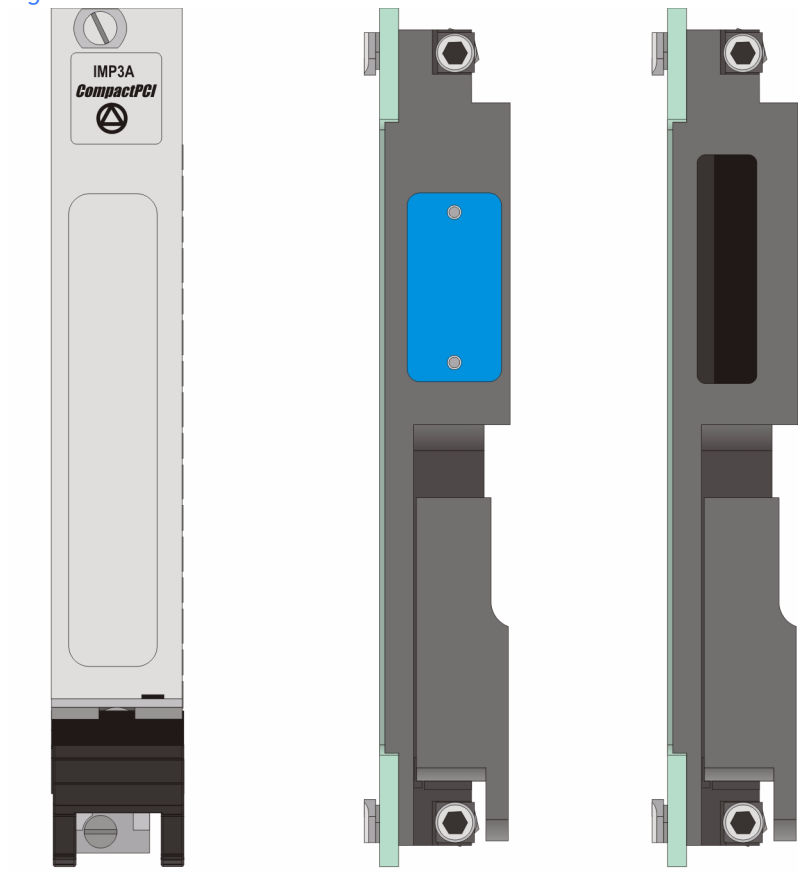
## 3.16 Front Panel

The IMP3A fully supports PMC front panel I/O, so no front I/O is available.

### 3.16.1 Glyphs

The IMP3A is labelled in accordance with the PICMG 2.0 specification regarding slot identification. Peripheral-only variants are labelled with a circle, whereas System or Peripheral variants are labelled with both a triangle and circle. In addition, the IMP3A is labelled “CompactPCI” in accordance with PICMG2.0.

Figure 3-8 Front Panels



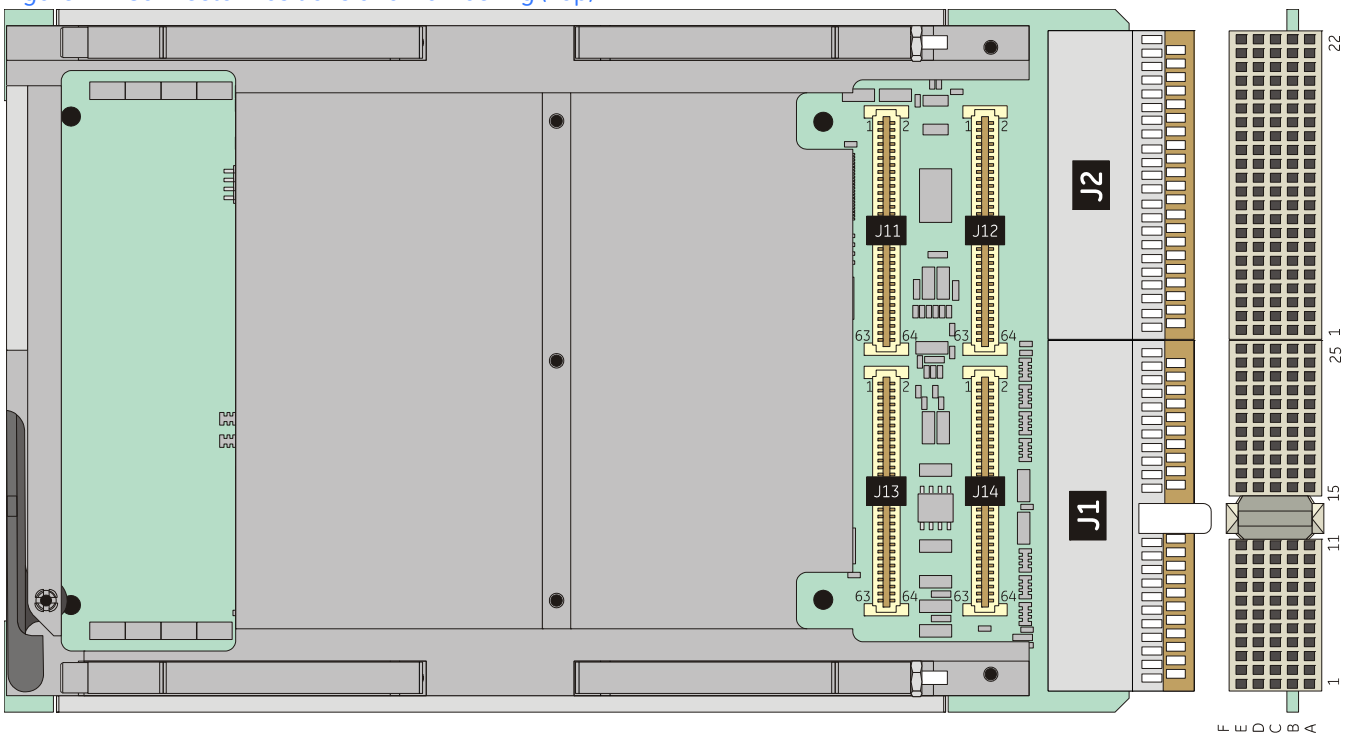
# 4 • Connectors

This section gives the pin assignments and signal descriptions for the connectors on the IMP3A. The following table shows the function of the connectors on the IMP3A.

Table 4-1 IMP3A Connector Functions

| Connector | Function |
|---|---|
| J1 | PCI |
| J2 | PCI, User I/O |
| J11, J12, J13, J14 | PMC site |
| P17 | Test Access Card connector |

Figure 4-1 Connector Positions and Numbering (Top)



## 4.1 CPCI (J1) Backplane Connector

The IMP3A J1 connector conforms with the PCI standard. For pin assignments and signal descriptions, see the Standard Interfaces section. Additional signals, shown in the following table, replace those given in the Standard table.

Table 4-2 J1 Connector Pin Assignments

| Pin | Standard Signal | IMP3A Connection |
|---|---|---|
| B17 | SDONE | No connection |
| C17 | SBO# | No connection |
| B16 | GND | Connected to GND |
| D15 | GND (BDSEL#) | Connected to GND |
| A5 | BRSVP1A4 | No connection/AUTOWR[a] |
| A4 | BRSVP1A4 | No connection |
| B4 | GND (HEALTHY#) | No connection |

a. Build option - contact the factory.

## 4.2 User I/O (J2) Backplane Connector

The following table summarizes the possible functions for each pin. Multi-function pins are shaded grey.

Table 4-3 J2 Connector Pin Assignments

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2/<br>USB_D+/<br>SATA0_TX+ | GPIO1/<br>USB_D-/<br>SATA0_TX- | GPIO0/<br><br>SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5/<br>ETH0_2- | GPIO4/<br>ETH0_2+ | GPIO3/<br>SATA0_RX- | GND |
| 19 | GND | GND | GPIO8/<br>ETH0_3- | GPIO7/<br>ETH0_3+ | GPIO6/<br>ETH1_2+ | GND |
| 18 | COM1_TXD/<br>COM1_TXD_A | COM1_RXD/<br>COM1_RXD_A | GPIO11/<br>COM1_TXD_B<br>ETH1_3- | GPIO10/<br>COM1_RXD_B<br>ETH1_3+ | GPIO9/<br><br>ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5#/<br>J14-48 | GNT5#/<br>J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL/<br>USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40/<br>SATA1_TX- | J14-39/<br>SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45/<br>GPIO14 | J14-44/<br>GPIO13 | J14-43/<br>GPIO12 | J14-42/<br>SATA1_RX- | J14-41/<br>SATA1_RX+ | GND |
| 4 | VIO/<br>J14-50 | FLASH_WE#/<br>J14-49 | ETH0_1+ | ETH0_1- | J14-46/<br>GPIO15 | GND |
| 3 | CLK4/<br>J14-55 | GND/<br>J14-54 | GNT3#/<br>J14-53 | REQ4#/<br>J14-52 | GNT4#/<br>J14-51 | GND |
| 2 | CLK2/<br>J14-60 | CLK3/<br>J14-59 | SYSEN#/<br>J14-58 | GNT2#/<br>J14-57 | REQ3#/<br>J14-56 | GND |
| 1 | CLK1 | GND/<br>J14-64 | REQ1#/<br>J14-63 | GNT1#/<br>J14-62 | REQ2#/<br>J14-61 | GND |

The following tables show the applicable signals for each variant. For a complete pinout per variant, see Appendix A.

### 4.2.1 Dual 10/100 and 8 GPIO Variant (IMP3A-xxxx0xxx)

Table 4-4 J2 Connector Pin Assignments for Dual 10/100 and 8 GPIO Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | *DOV* | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | *DOV* | *DOV* | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.6 to 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

### 4.2.2 Dual 10/100/1000 and PMC 43 to 46 Variant (IMP3A-xxxx4xxx)

Table 4-5 J2 Connector Pin Assignments for Dual 10/100/1000 and PMC 43 to 46 Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | *DOV* | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | *DOV* | *DOV* | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.6 to 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

### 4.2.3 Dual 10/100/1000 and 4 GPIO Variant (IMP3A-xxxx6xxx)

Table 4-6 J2 Connector Pin Assignments for Dual 10/100/1000 and 4 GPIO Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | *DOV* | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | *DOV* | *DOV* | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.6 to 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

### 4.2.4 Dual 10/100 and COM1 RS422 Variant (IMP3A-xxxx7xxx)

Table 4-7 J2 Connector Pin Assignments for Dual 10/100 and COM1 RS422 Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | *DOV* | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | *DOV* | *DOV* | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.6 to 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

NOTE

This option is not available on Rev 1 boards.

### 4.2.5 10/100, 10/100/1000 and 4 GPIO Variant (IMP3A-xxxx8xxx)

Table 4-8 J2 Connector Pin Assignments for 10/100, 10/100/1000 and 4 GPIO Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | *DOV* | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | *DOV* | *DOV* | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.6 to 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

### 4.2.6 GPIO and PMC 39 to 42 Variant (IMP3A-xxxxx0xx)

Table 4-9 J2 Connector Pin Assignments for GPIO & PMC 39 to 42 Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | GPIO3 | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | J14-42 | J14-41 | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.5, 4.2.11 and 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

### 4.2.7 USB and PMC 39 to 42 Variant (IMP3A-xxxxx1xx)

Table 4-10 J2 Connector Pin Assignments for USB & PMC 39 to 42 Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | GPIO3 | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | J14-42 | J14-41 | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.5, 4.2.11 and 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

### 4.2.8 SATA and PMC 39 to 42 Variant (IMP3A-xxxxx2xx)

Table 4-11 J2 Connector Pin Assignments for SATA & PMC 39 to 42 Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | SATA0_RX- | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | J14-42 | J14-41 | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.5, 4.2.11 and 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

## 4.2.9 USB and SATA Variant (IMP3A-xxxxx3xx)

Table 4-12 J2 Connector Pin Assignments for USB & SATA Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | GPIO3 | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | SATA1_RX- | SATA1_RX+ | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.5, 4.2.11 and 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

## 4.2.10 Dual SATA Variant (IMP3A-xxxxx4xx)

Table 4-13 J2 Connector Pin Assignments for Dual SATA Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | SATA0_RX- | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | *DOV* | *DOV* | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | SATA1_RX- | SATA1_RX+ | GND |
| 4 | *DOV* | *DOV* | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 2 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 1 | CLK1 | *DOV* | *DOV* | *DOV* | *DOV* | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.5, 4.2.11 and 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

## 4.2.11 System Controller Variant (IMP3A-xxxxxxSx)

Table 4-14 J2 Connector Pin Assignments for System Controller Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | *DOV* | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.10 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

## 4.2.12 Peripheral Only Variant (IMP3A-xxxxxxPx

Table 4-15 J2 Connector Pin Assignments for Peripheral Only Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | *DOV* | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Only signals affected by this option are left unshaded above. See sections 4.2.1 to 4.2.10 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

CAUTION

Do not install this variant in a System Controller slot.

### 4.2.13 Non-User I/O Signals

Table 4-16 J2 Connector Pin Assignments for Non-User I/O Signals (System Controller)

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | *DOV* | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Only non-user I/O signals are left unshaded above. These are described in more detail in the Standard Interfaces section. See sections 4.2.1 to 4.2.12 for the signals applicable in the *"DOV"* (= Depends on Other Variants) fields.

Table 4-17 J2 Connector Pin Assignments for Non-User I/O Signals (Peripheral)

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | *DOV* | *DOV* | *DOV* | GND |
| 20 | CLK5 | GND | *DOV* | *DOV* | *DOV* | GND |
| 19 | GND | GND | *DOV* | *DOV* | *DOV* | GND |
| 18 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | *DOV* | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | *DOV* | *DOV* | J14-38 | J14-37 | J14-36 | GND |
| 5 | *DOV* | *DOV* | *DOV* | *DOV* | *DOV* | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | *DOV* | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Only non-user I/O signals are left unshaded above. These are described in more detail in the Standard Interfaces section. See sections 4.2.1 to 4.2.12 for the signals applicable in the "*DOV*" (= Depends on Other Variants) fields.

## 4.2.14 Signal Descriptions

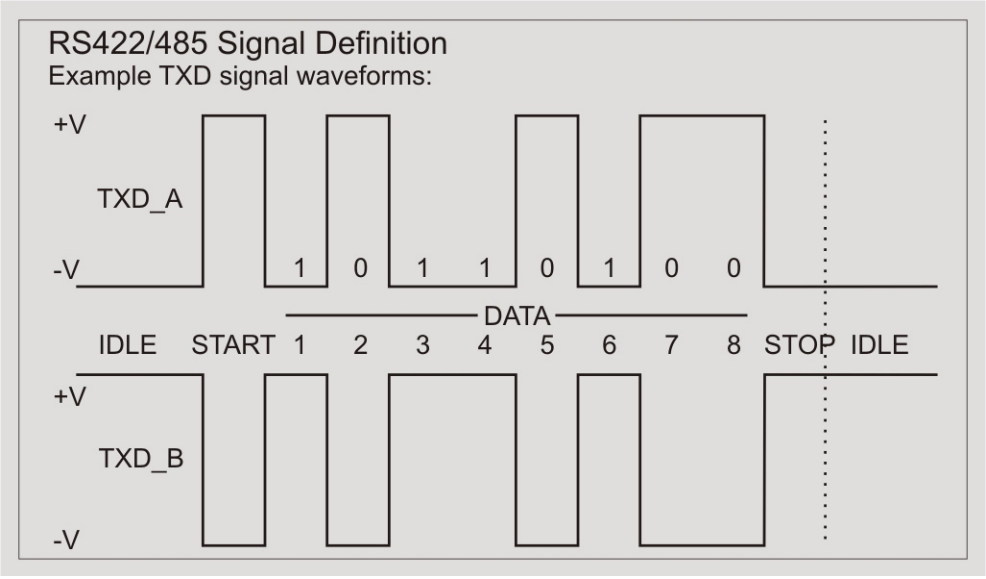
Table 4-18 Signal Descriptions

| Mnemonic | Description |
|---|---|
| GPIO[0:15] | General Purpose I/O lines 0 to 15 |
| USB_D+, USB_D-, USB_PWR | USB port |
| SATA0_TX+/TX-, SATA0_RX+/RX- | SATA port 0 |
| SATA1_TX+/TX-, SATA1_RX+/RX- | SATA port 1 |
| ETH0_0+/0-, ETH0_1+/1-, ETH0_2+/2-, ETH0_3+/3- | Ethernet port 0 |
| ETH1_0+/0-, ETH1_1+/1-, ETH1_2+/2-, ETH1_3+/3- | Ethernet port 1 |
| COM1_TXD, COM1_RXD | RS232 serial COM port 1 |
| COM1_TXD_A, COM1_RXD_A, COM1_TXD_B, COM1_RXD_B | RS422 serial COM port 1 |
| COM2_TXD_A, COM2_RXD_A, COM2_TXD_B, COM2_RXD_B | RS422 serial COM port 2[a] |
| J14-1 to J14-64 | PMC I/O from J14 |
| RTC_STDBY | Standby voltage input (1.8 to 5.5 V) |
| BITFAIL | BIT Fail output signal (open drain) |
| FLASH_WE#[b] | Flash Write Enable. This signal performs the same function as the Flash Protection Unlock Link (E4) |

a. When using COM2 as RS232, TXD_A = TXD, TXD_B = RTS, RXD_A = RXD and RXD_B = CTS. These are multifunction pins rather than a build option. RS422/RS232 functionality is controlled by the FPGA Control Register 2 (offset 0x000E).
b. Not available on Rev 1 boards.

For RS422 outputs, the non-inverting output of the differential pair is designated "B" and the inverting output is designated "A", as shown below.

Figure 4-2 RS422/485 Signal Definition



## 4.3 PMC Connectors (J11 to J14)

For pin assignments and signal descriptions, see the Standard Interfaces section. Reserved signals are not connected on the IMP3A.

## 4.4 Test Access Board Connector (P17)

Figure 4-3 Connector Position and Numbering (Back)

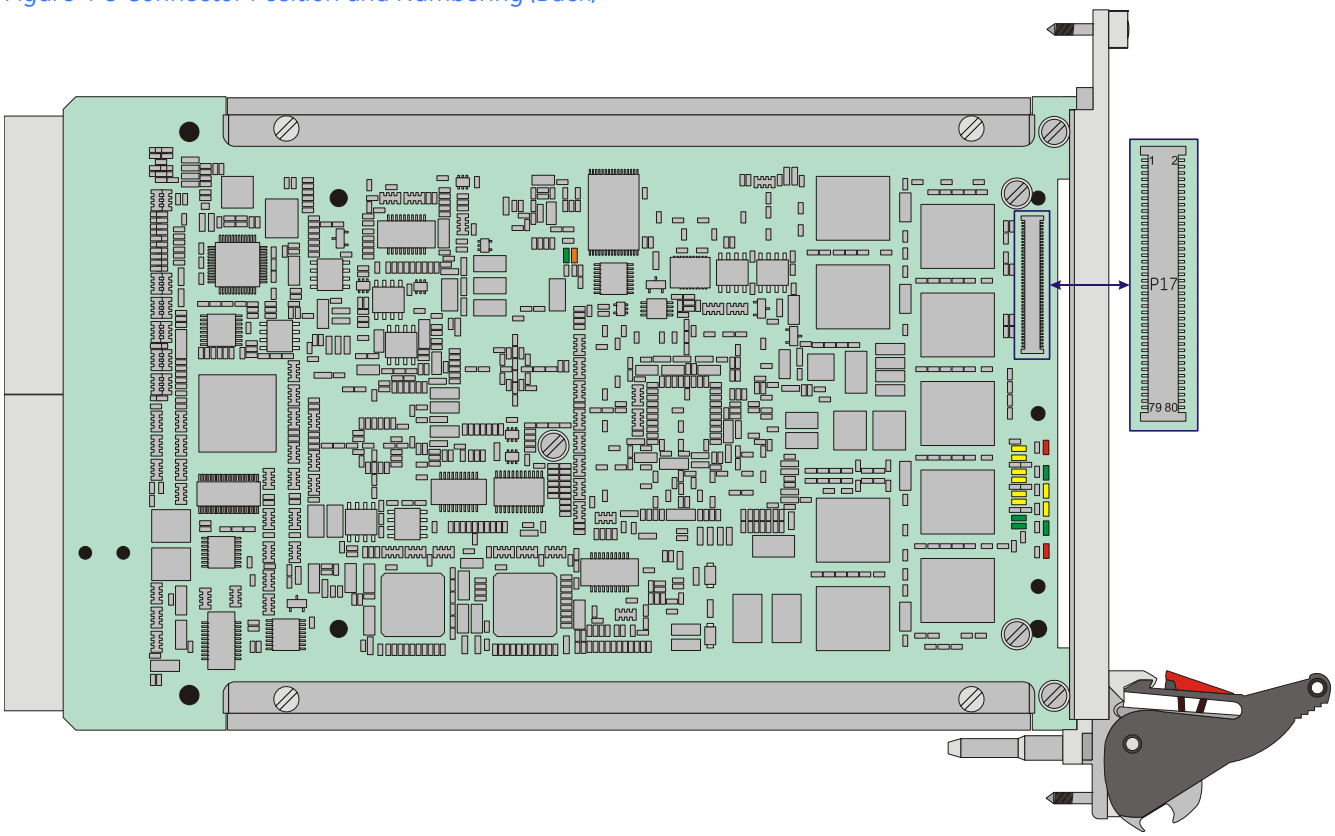


Table 4-19 Test Access Board Connector (P17) Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 79 | VCC | 80 | VCC |
| 77 | BOOTSWAP0_LINK# | 78 | SPARE_0 |
| 75 | BOOTSWAP1_LINK# | 76 | SPARE_1 |
| 73 | RECOVERY_LINK# | 74 | SPARE_2 |
| 71 | FLASH_PW_LINK# | 72 | SPARE_3 |
| 69 | No connection | 70 | SPARE_4 |
| 67 | SPARE_LINK# | 68 | PWRMGR_STATUS[0] |
| 65 | No connection | 66 | PWRMGR_STATUS[1] |
| 63 | BOOTSEQ_DIS_LINK# | 64 | PWRMGR_STATUS[2] |
| 61 | No connection | 62 | No connection |
| 59 | NVRAM_WE_LINK | 60 | SPI_MISO |
| 57 | GND | 58 | GND |
| 55 | No connection | 56 | SPI_MOSI |
| 53 | BP_JTAG_TCK | 54 | SPI_CS# |
| 51 | BP_JTAG_TDO | 52 | SPI_CLK |
| 49 | BP_JTAG_TRST# | 50 | I2C_1_SCL |
| 47 | BP_JTAG_TMS | 48 | I2C_1_SDA |
| 45 | BP_JTAG_TDI | 46 | I2C_2_SCL |
| 43 | RESET_BOARD# | 44 | I2C_2_SDA |
| 41 | +3.3V_BP | 42 | +3.3V_BP |
| 39 | PWRMGR_PGOOD# | 40 | No connection |
| 37 | BANC_WE_LINK# | 38 | SHUT_DWN# |
| 35 | SPI_BOOT_LINK# | 36 | PROG_MODE_LINK# |
| 33 | PASS_THRU_EN# | 34 | SW_LNK_OVERIDE_LINK# |
| 31 | GND | 32 | GND |
| 29 | No connection | 30 | PWR_TCK |
| 27 | PASS_THRU(2) | 28 | PWR_TMS |
| 25 | PASS_THRU(1) | 26 | PWR_TDO |
| 23 | PASS_THRU(0) | 24 | PWR_TDI |
| 21 | +3.3V | 22 | +3.3V |
| 19 | RESET_ETX# | 20 | LATT_TCK |
| 17 | COP_TDO | 18 | LATT_TMS |
| 15 | COP_TDI | 16 | LATT_ISPCLK_TDO |
| 13 | No connection | 14 | LATT_FPGA_TDI |
| 11 | COP_TCK | 12 | No connection |
| 9 | COP_TMS | 10 | SCANBR_EN_LINK# |
| 7 | COP_SRST# | 8 | No connection |
| 5 | COP_HRST# | 6 | COP_TRST# |
| 3 | P2020_CKSTP_OUT# | 4 | P2020_CKSTP_IN# |
| 1 | GND | 2 | GND |

# 5 • Specifications

## 5.1 Technical Specification

Table 5-1 Technical Details

| Feature | Details | Comments |
|---|---|---|
| Host Processor | Freescale P2020/2010 at up to 1.2 GHz | Dual e500v2 cores for P2020, single core for P2010 |
| Main Memory | 1 GByte DDR3 SDRAM | Up to 4 GBytes supported |
| Flash Memory | 256 MBytes NOR Flash,<br>8 GByte SSD | Up to 512 MByte of NOR Flash supported.<br>Higher capacities supported when available |
| Non-Volatile RAM | 128 KBytes | Ferroelectric RAM |
| Ethernet Interfaces | 2 x 10/100/1000BaseT | Various I/O options |
| Serial Ports | 2 x RS232/RS422 | |
| USB | 1 channel | |
| SATA | 2 channels, SATA1 (150 MBytes/second) | |
| Discrete Digital I/O | Up to 16 lines | Able to generate edge or level-triggered interrupts |
| PMC Site | 1 site, 64-bit 133 MHz PCI-X | 5 V or 3.3 V VIO |
| Timers | 8 x 31 bit | Configurable as 6 x 63-bit, 1 x 95-bit or 1 x 127 bit |
| Watchdog Timers | 2 x 32-bit | Provided by FPGA |
| RTC | Epson RX8581 | 1 second resolution |
| ETI | Dallas DS1682 | Powered time & number of power cycles |
| Board Temperature | LM92 | Ambient temperature |
| CPU Temperature | ADT7481 | PCB temperature near core |
| Software Links | PCA9560 EEPROM DIP Switch | Software control over hardware link settings |
| CPCI Interface | 33/66 MHz 5 V and 3.3 V VIO | System Controller and Peripheral Only I/O options |
| JTAG interface | Access via backplane J1 or on-board connector | For factory test and system boundary scan |

## 5.2 Electrical Specification

Two IEC 61076-4-101 compatible connectors that mate with rack mounted backplane connectors form the electrical connection to the IMP3A.

### 5.2.1 Voltage Supply Requirements

| | |
|---|---|
| +5 V | +5%/-3% at a maximum of 3.5 Amps (+85 °C) |
| +3.3 V | +5%/-3% at a maximum of 1.5 Amps (+85 °C) |
| $V_{ripple}$ | (+5 V and +3.3 V) = 50 mV RMS (maximum) contained within the total excursion. |

The IMP3A does not use the 12 V supply lines, but they are fed to the PMC site.

| | |
|---|---|
| +12 V | ±5% |
| -12 V | ±5% |
| $V_{ripple}$ | (+12 V and -12 V) = 240 mV |

**WARNING**

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components

### 5.2.2 Auxiliary Supply

The maximum current consumption on the RTC_STDBY supply (1.8 to 5.5 V input) is 300 µA at 5.5 V and 75 µA at 3.3 V.

### 5.2.3 Power Consumption

The IMP3A uses both +3.3 V and +5 V supply rails.

Table 5-2 Power Consumption

| Processor & Speed | +25°C | | +85°C | |
|---|---|---|---|---|
| | Typical | Maximum | Typical | Maximum |
| P2020 @ 1200 MHz | 12.7 W | 16.0 W | 15.4 W | 17.9 W |
| P2020 @ 1000 MHz | 12.3 W | 15.4 W | 14.5 W | 17.3 W |
| P2020 @ 800 MHz | 11.7 W | 15.0 W | 14.0 W | 16.8 W |

**NOTE**

These figures are for the IMP3A only and do not include any power drawn by PMCs. If a PMC is fitted, ensure that the power supply to the slot is adequate for the combined consumption.

### 5.2.4 GPIO Electrical Characteristics

Table 5-3 GPIO Electrical Characteristics

| Parameter | Minimum | Maximum |
|---|---|---|
| $Vin_l$ | -0.3 V | 0.8 V |
| $Vin_h$ | 2.0 V | 3.6 V |
| $Vout_l$ | - | 0.4 V |
| $Vout_h$ | 2.9 V | - |

**GPIO Absolute Maximum Ratings**

Table 5-4 GPIO Absolute Maximum Ratings

| Pin | Maximum (Volts) |
|---|---|
| Any GPIO pin | -0.5 to +7 |

## 5.3 Environmental Specification

See the Environmental Specification section in the PowerPact3 Product Family manual.


LINK
PowerPact3 Product Family Manual, publication number PP3-0HH.

## 5.4 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time Between Failures (MTBF) and failures per million hours (fpmh) for the IMP3A-x212xxxx (see the Product Codes section for variant details).

Table 5-5 Reliability (MTBF)

| Environment | Fail Rate (Failures Per Million Hours) | MTBF (Hours) |
|---|---|---|
| Ground Benign 30°C | 1.7592 | 568 450 |
| Ground Fixed 40°C | 7.3600 | 135 870 |
| Ground Mobile 45°C | 18.8804 | 52 965 |
| Naval Sheltered 40°C | 10.7785 | 92 777 |
| Naval Unsheltered 45°C | 26.7745 | 37 349 |
| Airborne Inhabited Cargo 55°C | 18.7821 | 53 242 |
| Airborne Inhabited Fighter 55°C | 24.4826 | 40 845 |
| Airborne Uninhabited Cargo 70°C | 47.0072 | 21 273 |
| Airborne Uninhabited Fighter 70°C | 61.2934 | 16 315 |
| Airborne Rotary Wing 55°C | 54.3280 | 18 407 |
| Space Flight 30°C | 1.3937 | 717 530 |
| Missile Flight 45°C | 29.30117 | 34 128 |
| Missile Launch 55°C | 82.7215 | 12 089 |

The predictions are carried out using MIL-HDBK-217F Notice 2, Parts Count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; πQ values have been modified according to the ANSI/VITA 51.1 specification.

## 5.5 Mechanical Specification

### 5.5.1 Dimensions

The IMP3A is constructed on a multi-layer Eurocard and conforms to the dimensions specified in PICMG 2.0 R3.0, section 4. For layout drawings, see the PowerPact3 Product Family manual.


LINK
PowerPact3 Product Family Manual, publication number PP3-0HH.

### 5.5.2 Weight

The approximate weight of the IMP3A is:

Build levels 1 to 3 = 300 g

Build levels 4 and 5 = 285 g

These figures do not include any PMC fitted.

# 5.6 Product Codes

Table 5-6 Product Codes

| IMP3A | - | x | x | x | x | x | x | x | x |
|---|---|---|---|---|---|---|---|---|---|

| | |
|---|---|
| **Software** | 3 = VxWorks |
| | 4 = BIT + VxWorks |
| | 5 = U-Boot |
| | 6 = BIT + U-Boot |
| **Slot Type** | S = System or Peripheral functions (46 x PMC I/O maximum) |
| | P = Peripheral only (up to 64 x PMC I/O) |
| **GPIO/USB/SATA Options** | 0 = 4 x GPIO, PMC I/O 39 to 42 available |
| | 1 = USB, 2 x GPIO, PMC I/O 39 to 42 available |
| | 2 = 1 x SATA, PMC I/O 39 to 42 available |
| | 3 = USB, 1 x SATA |
| | 4 = 2 x SATA |
| **Ethernet/GPIO/Serial Options** | 0 = Dual 10/100, 8 x GPIO |
| | 4 = Dual 10/100/1000, full PMC I/O |
| | 6 = Dual 10/100/1000, 4 x GPIO |
| | 7 = Dual 10/100, 6 x GPIO, COM1 RS422[a] |
| | 8 = Single 10/100/1000, single 10/100, 4 x GPIO |
| **Flash Memory** | 7 = 256 MBytes of NOR Flash + 8 GByte SSD |
| | 8 = 512 MBytes of NOR Flash + 8 GByte SSD |
| **DRAM** | 1 = 1 GByte of DDR3 SDRAM |
| | 2 = 2 GBytes of DDR3 SDRAM |
| **Processor** | 1 = P2020 @ 1200 MHz |
| | 2 = P2020 @ 1000 MHz |
| | 3 = P2020 @ 800 MHz |
| | 4 = P2010 @ 1200 MHz |
| | 5 = P2010 @ 1000 MHz |
| | 6 = P2010 @ 800 MHz |
| **Ruggedization** | 1 = Build level 1 |
| | 2 = Build level 2 |
| | 3 = Build level 3 |
| | 4 = Build level 4 |
| | 5 = Build level 5 |

a.Not available on Rev 1 boards.

NOTE

Theses are the product codes at time of writing. Contact your nearest GEIP sales office or agent for latest versions.

NOTE

Variants that call up SSD and SATA channel 0 (e.g. IMP3A-xxx7x2xx) are not permissible.

## 5.7 Software Support

Workbench/Platforms/VxWorks BSP - PP3BSP-WBV1M
Workbench/Platforms/VxWorks ESP - PP3BESP-WBV1M

LynxOS BSP - IMPBSP-LNX2M
LynxOS ESP - IMPBESP-LNX2M

PowerPact3 BIT - IMPBIT-2M
PowerPact3 BIT source code - IMPBITSRC-2M.

Contact GEIP for more details on these or availability of support for other operating systems.

## 5.8 I/O Modules

The backplane transition module for the IMP3A is the CPCI3UX606. For more information, see the I/O modules manual.


LINK
I/O Modules Manual, publication number RT5154.

## 5.9 Test Adaptor Card

For access to JTAG and other debugging functions, a test adapter card is available as IMP3ATST.

# A • User I/O Options

The following table shows the I/O options available on the J2 backplane connector. This table is hyperlinked on the 'Option' field to the appropriate table showing the full J2 pin assignments for that variant.

Table A-1 I/O Option Selector

| Option | Ethernet | GPIO | Serial | USB | SATA | PMC I/O | System/Peripheral |
|---|---|---|---|---|---|---|---|
| -xxxx00Sx | Dual 10/100 | 12 | COM1 RS232, COM2 RS422 | | | 1 to 46 | System |
| -xxxx00Px | Dual 10/100 | 12 | COM1 RS232, COM2 RS422 | | | 1 to 64 | Peripheral |
| -xxxx01Sx | Dual 10/100 | 10 | COM1 RS232, COM2 RS422 | 1 | | 1 to 46 | System |
| -xxxx01Px | Dual 10/100 | 10 | COM1 RS232, COM2 RS422 | 1 | | 1 to 64 | Peripheral |
| -xxxx02Sx | Dual 10/100 | 8 | COM1 RS232, COM2 RS422 | | 1 | 1 to 46 | System |
| -xxxx02Px | Dual 10/100 | 8 | COM1 RS232, COM2 RS422 | | 1 | 1 to 64 | Peripheral |
| -xxxx03Sx | Dual 10/100 | 10 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 46 | System |
| -xxxx03Px | Dual 10/100 | 10 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx04Sx | Dual 10/100 | 8 | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 43 to 46 | System |
| -xxxx04Px | Dual 10/100 | 8 | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx40Sx | Dual Gigabit | 4 | COM1 RS232, COM2 RS422 | | | 1 to 46 | System |
| -xxxx40Px | Dual Gigabit | 4 | COM1 RS232, COM2 RS422 | | | 1 to 64 | Peripheral |
| -xxxx41Sx | Dual Gigabit | 2 | COM1 RS232, COM2 RS422 | 1 | | 1 to 46 | System |
| -xxxx41Px | Dual Gigabit | 2 | COM1 RS232, COM2 RS422 | 1 | | 1 to 64 | Peripheral |
| -xxxx42Sx | Dual Gigabit | | COM1 RS232, COM2 RS422 | | 1 | 1 to 46 | System |
| -xxxx42Px | Dual Gigabit | | COM1 RS232, COM2 RS422 | | 1 | 1 to 64 | Peripheral |
| -xxxx43Sx | Dual Gigabit | 2 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 46 | System |
| -xxxx43Px | Dual Gigabit | 2 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx44Sx | Dual Gigabit | | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 43 to 46 | System |
| -xxxx44Px | Dual Gigabit | | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx60Sx | Dual Gigabit | 8 | COM1 RS232, COM2 RS422 | | | 1 to 42 | System |
| -xxxx60Px | Dual Gigabit | 8 | COM1 RS232, COM2 RS422 | | | 1 to 42, 47 to 64 | Peripheral |
| -xxxx61Sx | Dual Gigabit | 6 | COM1 RS232, COM2 RS422 | 1 | | 1 to 42 | System |
| -xxxx61Px | Dual Gigabit | 6 | COM1 RS232, COM2 RS422 | 1 | | 1 to 42, 47 to 64 | Peripheral |
| -xxxx62Sx | Dual Gigabit | 4 | COM1 RS232, COM2 RS422 | | 1 | 1 to 42 | System |
| -xxxx62Px | Dual Gigabit | 4 | COM1 RS232, COM2 RS422 | | 1 | 1 to 42, 47 to 64 | Peripheral |
| -xxxx63Sx | Dual Gigabit | 6 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38 | System |
| -xxxx63Px | Dual Gigabit | 6 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 47 to 64 | Peripheral |
| -xxxx64Sx | Dual Gigabit | 4 | COM1 RS232, COM2 RS422 | | 2 | 1 to 38 | System |
| -xxxx64Px | Dual Gigabit | 4 | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 47 to 64 | Peripheral |
| -xxxx70Sx[a] | Dual 10/100 | 10 | COM1 RS422, COM2 RS422 | | | 1 to 46 | System |
| -xxxx70Px[a] | Dual 10/100 | 10 | COM1 RS422, COM2 RS422 | | | 1 to 64 | Peripheral |
| -xxxx71Sx[a] | Dual 10/100 | 8 | COM1 RS422, COM2 RS422 | 1 | | 1 to 46 | System |
| -xxxx71Px[a] | Dual 10/100 | 8 | COM1 RS422, COM2 RS422 | 1 | | 1 to 64 | Peripheral |
| -xxxx72Sx[a] | Dual 10/100 | 6 | COM1 RS422, COM2 RS422 | | 1 | 1 to 46 | System |

Table A-1 I/O Option Selector

| Option | Ethernet | GPIO | Serial | USB | SATA | PMC I/O | System/Peripheral |
|---|---|---|---|---|---|---|---|
| -xxxx72Px[a] | Dual 10/100 | 6 | COM1 RS422, COM2 RS422 | | 1 | 1 to 64 | Peripheral |
| -xxxx73Sx[a] | Dual 10/100 | 8 | COM1 RS422, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 46 | System |
| -xxxx73Px[a] | Dual 10/100 | 8 | COM1 RS422, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx74Sx[a] | Dual 10/100 | 6 | COM1 RS422, COM2 RS422 | | 2 | 1 to 38, 43 to 46 | System |
| -xxxx74Px[a] | Dual 10/100 | 6 | COM1 RS422, COM2 RS422 | | 2 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx80Sx | Single Gigabit, single 10/100 | 8 | COM1 RS232, COM2 RS422 | | | 1 to 46 | System |
| -xxxx80Px | Single Gigabit, single 10/100 | 8 | COM1 RS232, COM2 RS422 | | | 1 to 64 | Peripheral |
| -xxxx81Sx | Single Gigabit, single 10/100 | 6 | COM1 RS232, COM2 RS422 | 1 | | 1 to 46 | System |
| -xxxx81Px | Single Gigabit, single 10/100 | 6 | COM1 RS232, COM2 RS422 | 1 | | 1 to 64 | Peripheral |
| -xxxx82Sx | Single Gigabit single 10/100 | 4 | COM1 RS232, COM2 RS422 | | 1 | 1 to 46 | System |
| -xxxx82Px | Single Gigabit, single 10/100 | 4 | COM1 RS232, COM2 RS422 | | 1 | 1 to 64 | Peripheral |
| -xxxx83Sx | Single Gigabit, single 10/100 | 6 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 46 | System |
| -xxxx83Px | Single Gigabit, single 10/100 | 6 | COM1 RS232, COM2 RS422 | 1 | 1 | 1 to 38, 43 to 64 | Peripheral |
| -xxxx84Sx | Single Gigabit, single 10/100 | 4 | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 43 to 46 | System |
| -xxxx84Px | Single Gigabit, single 10/100 | 4 | COM1 RS232, COM2 RS422 | | 2 | 1 to 38, 43 to 64 | Peripheral |

a. Not available on Rev 1 boards.

## A.1 IMP3A-xxxx00Sx

Table A-2 J2 Connector Pin Assignments for IMP3A-xxxx00Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.2 IMP3A-xxxx00Px

Table A-3 J2 Connector Pin Assignments for IMP3A-xxxx00Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.3 IMP3A-xxxx01Sx

Table A-4 J2 Connector Pin Assignments for IMP3A-xxxx01Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.4 IMP3A-xxxx01Px

Table A-5 J2 Connector Pin Assignments for IMP3A-xxxx01Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.5 IMP3A-xxxx02Sx

Table A-6 J2 Connector Pin Assignments for IMP3A-xxxx02Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.6 IMP3A-xxxx02Px

Table A-7 J2 Connector Pin Assignments for IMP3A-xxxx02Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.7 IMP3A-xxxx03Sx

Table A-8 J2 Connector Pin Assignments for IMP3A-xxxx03Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.8 IMP3A-xxxx03Px

Table A-9 J2 Connector Pin Assignments for IMP3A-xxxx03Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.9 IMP3A-xxxx04Sx

Table A-10 J2 Connector Pin Assignments for IMP3A-xxxx04Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.10 IMP3A-xxxx04Px

Table A-11 J2 Connector Pin Assignments for IMP3A-xxxx04Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.11 IMP3A-xxxx40Sx

Table A-12 J2 Connector Pin Assignments for IMP3A-xxxx40Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.12 IMP3A-xxxx40Px

Table A-13 J2 Connector Pin Assignments for IMP3A-xxxx40Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.13 IMP3A-xxxx41Sx

Table A-14 J2 Connector Pin Assignments for IMP3A-xxxx41Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.14 IMP3A-xxxx41Px

Table A-15 J2 Connector Pin Assignments for IMP3A-xxxx41Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.15 IMP3A-xxxx42Sx

Table A-16 J2 Connector Pin Assignments for IMP3A-xxxx42Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.16 IMP3A-xxxx42Px

Table A-17 J2 Connector Pin Assignments for IMP3A-xxxx42Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.17 IMP3A-xxxx43Sx

Table A-18 J2 Connector Pin Assignments for IMP3A-xxxx43Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.18 IMP3A-xxxx43Px

Table A-19 J2 Connector Pin Assignments for IMP3A-xxxx43Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.19 IMP3A-xxxx44Sx

Table A-20 J2 Connector Pin Assignments for IMP3A-xxxx44Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.20 IMP3A-xxxx44Px

Table A-21 J2 Connector Pin Assignments for IMP3A-xxxx44Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.21 IMP3A-xxxx60Sx

Table A-22 J2 Connector Pin Assignments for IMP3A-xxxx60Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.22 IMP3A-xxxx60Px

Table A-23 J2 Connector Pin Assignments for IMP3A-xxxx60Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.23 IMP3A-xxxx61Sx

Table A-24 J2 Connector Pin Assignments for IMP3A-xxxx61Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.24 IMP3A-xxxx61Px

Table A-25 J2 Connector Pin Assignments for IMP3A-xxxx61Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.25 IMP3A-xxxx62Sx

Table A-26 J2 Connector Pin Assignments for IMP3A-xxxx62Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.26 IMP3A-xxxx62Px

Table A-27 J2 Connector Pin Assignments for IMP3A-xxxx62Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.27 IMP3A-xxxx63Sx

Table A-28 J2 Connector Pin Assignments for IMP3A-xxxx63Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.28 IMP3A-xxxx63Px

Table A-29 J2 Connector Pin Assignments for IMP3A-xxxx63Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.29 IMP3A-xxxx64Sx

Table A-30 J2 Connector Pin Assignments for IMP3A-xxxx64Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

# A.30 IMP3A-xxxx64Px

Table A-31 J2 Connector Pin Assignments for IMP3A-xxxx64Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | ETH1_2+ | GND |
| 18 | COM1_TXD | COM1_RXD | ETH1_3- | ETH1_3+ | ETH1_2- | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | GPIO14 | GPIO13 | GPIO12 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | GPIO15 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

# A.31 IMP3A-xxxx70Sx

Table A-32 J2 Connector Pin Assignments for IMP3A-xxxx70Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**NOTE**

This option is not available on Rev 1 boards.

# A.32 IMP3A-xxxx70Px

Table A-33 J2 Connector Pin Assignments for IMP3A-xxxx70Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

**NOTE**

This option is not available on Rev 1 boards.

## A.33 IMP3A-xxxx71Sx

Table A-34 J2 Connector Pin Assignments for IMP3A-xxxx71Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**NOTE**

This option is not available on Rev 1 boards.

## A.34 IMP3A-xxxx71Px

Table A-35 J2 Connector Pin Assignments for IMP3A-xxxx71Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

**NOTE**

This option is not available on Rev 1 boards.

## A.35 IMP3A-xxxx72Sx

Table A-36 J2 Connector Pin Assignments for IMP3A-xxxx72Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**NOTE**

This option is not available on Rev 1 boards.

# A.36 IMP3A-xxxx72Px

Table A-37 J2 Connector Pin Assignments for IMP3A-xxxx72Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

**NOTE**

This option is not available on Rev 1 boards.

# A.37 IMP3A-xxxx73Sx

Table A-38 J2 Connector Pin Assignments for IMP3A-xxxx73Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**NOTE**

This option is not available on Rev 1 boards.

## A.38 IMP3A-xxxx73Px

Table A-39 J2 Connector Pin Assignments for IMP3A-xxxx73Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | GPIO3 | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

**NOTE**

This option is not available on Rev 1 boards.

## A.39 IMP3A-xxxx74Sx

Table A-40 J2 Connector Pin Assignments for IMP3A-xxxx74Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**NOTE**

This option is not available on Rev 1 boards.

# A.40 IMP3A-xxxx74Px

Table A-41 J2 Connector Pin Assignments for IMP3A-xxxx74Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | GPIO5 | GPIO4 | SATA0_RX- | GND |
| 19 | GND | GND | GPIO8 | GPIO7 | GPIO6 | GND |
| 18 | COM1_TXD_A | COM1_RXD_A | COM1_TXD_B | COM1_RXD_B | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

**NOTE**

This option is not available on Rev 1 boards.

## A.41 IMP3A-xxxx80Sx

Table A-42 J2 Connector Pin Assignments for IMP3A-xxxx80Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.42 IMP3A-xxxx80Px

Table A-43 J2 Connector Pin Assignments for IMP3A-xxxx80Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | GPIO2 | GPIO1 | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.43 IMP3A-xxxx81Sx

Table A-44 J2 Connector Pin Assignments for IMP3A-xxxx81Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.44 IMP3A-xxxx81Px

Table A-45 J2 Connector Pin Assignments for IMP3A-xxxx81Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.45 IMP3A-xxxx82Sx

Table A-46 J2 Connector Pin Assignments for IMP3A-xxxx82Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.46 IMP3A-xxxx82Px

Table A-47 J2 Connector Pin Assignments for IMP3A-xxxx82Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | J14-40 | J14-39 | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | J14-42 | J14-41 | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.47 IMP3A-xxxx83Sx

Table A-48 J2 Connector Pin Assignments for IMP3A-xxxx83Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

## A.48 IMP3A-xxxx83Px

Table A-49 J2 Connector Pin Assignments for IMP3A-xxxx83Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | USB_D+ | USB_D- | GPIO0 | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | GPIO3 | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | USB_PWR | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.

## A.49 IMP3A-xxxx84Sx

Table A-50 J2 Connector Pin Assignments for IMP3A-xxxx84Sx Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | REQ5# | GNT5# | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | VIO | FLASH_WE# | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2 | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| 1 | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

# A.50 IMP3A-xxxx84Px

Table A-51 J2 Connector Pin Assignments for IMP3A-xxxx84Px Variant

| Pin | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 22 | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | CLK6 | GND | SATA0_TX+ | SATA0_TX- | SATA0_RX+ | GND |
| 20 | CLK5 | GND | ETH0_2- | ETH0_2+ | SATA0_RX- | GND |
| 19 | GND | GND | ETH0_3- | ETH0_3+ | GPIO6 | GND |
| 18 | COM1_TXD | COM1_RXD | GPIO11 | GPIO10 | GPIO9 | GND |
| 17 | ETH1_1+ | ETH1_1- | PRST# | REQ6# | GNT6# | GND |
| 16 | ETH1_0+ | ETH1_0- | DEG# | GND | ETH0_0- | GND |
| 15 | COM2_TXD_B | COM2_TXD_A | FAL# | J14-48 | J14-47 | GND |
| 14 | COM2_RXD_B | COM2_RXD_A | RTC_STDBY | BITFAIL | ETH0_0+ | GND |
| 13 | J14-5 | J14-4 | J14-3 | J14-2 | J14-1 | GND |
| 12 | J14-10 | J14-9 | J14-8 | J14-7 | J14-6 | GND |
| 11 | J14-15 | J14-14 | J14-13 | J14-12 | J14-11 | GND |
| 10 | J14-20 | J14-19 | J14-18 | J14-17 | J14-16 | GND |
| 9 | J14-25 | J14-24 | J14-23 | J14-22 | J14-21 | GND |
| 8 | J14-30 | J14-29 | J14-28 | J14-27 | J14-26 | GND |
| 7 | J14-35 | J14-34 | J14-33 | J14-32 | J14-31 | GND |
| 6 | SATA1_TX- | SATA1_TX+ | J14-38 | J14-37 | J14-36 | GND |
| 5 | J14-45 | J14-44 | J14-43 | SATA1_RX- | SATA1_RX+ | GND |
| 4 | J14-50 | J14-49 | ETH0_1+ | ETH0_1- | J14-46 | GND |
| 3 | J14-55 | J14-54 | J14-53 | J14-52 | J14-51 | GND |
| 2 | J14-60 | J14-59 | J14-58 | J14-57 | J14-56 | GND |
| 1 | CLK1 | J14-64 | J14-63 | J14-62 | J14-61 | GND |

Key:

- GPIO
- PMC I/O
- Ethernet
- Serial
- USB
- SATA
- Non I/O signals. See the Standard Interfaces section.

**CAUTION**

Do not install this variant in a System Controller slot.


LINK
Also see the general Glossary, publication number GLOS1.

**CCB** Core Complex Bus (also called the Platform Bus).

**eLBC** Enhanced Local Bus Controller (integrated into the P2020).

**eTSEC** Enhanced Three (or Triple) Speed Ethernet Controller.

**FCM** Flash Chip-state Machine.

**GEIP** GE Intelligent Platforms.

**GPCM** General Purpose Chip-select Machine.

**SSD** Solid State Drive.

**TAC** Test Access Card.

**UDE** Unconditional Debug Exception.

**ULPI** UTMI + Low Pin-count Interface (the interface between the P2020 USB controller and the USB Phy).

**UTMI** USB2.0 Transceiver Macrocell Interface.

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## Additional Resources

For more information, please visit the GE Intelligent Platforms Embedded Systems web site at:

www.ge-ip.com

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