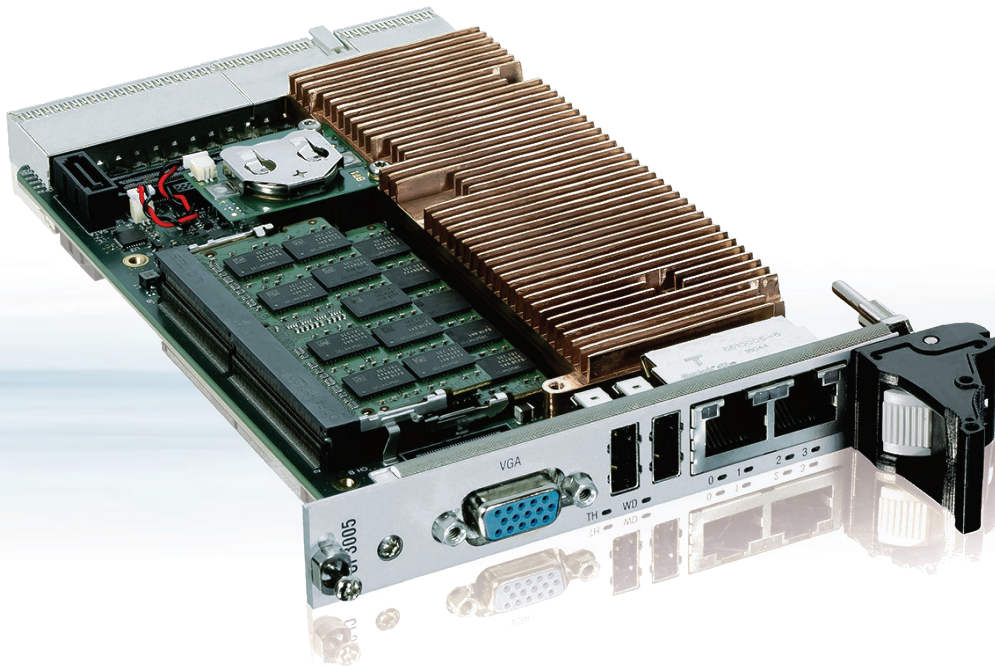




CP3005-SA

Doc. Rev. 0.6 Preliminary

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 CP3005-SA – USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author
0.1	Initial Issue	2018-Jan-27	hjs
0.3	title photo, M2 instead of CFast	2018-Nov-19	hjs
0.4	Corrections from Bastian and Rudolf	2019-Jan-08	hjs
0.5	extension boards, BIOS chapter, battery	2019-Feb-07	hjs
0.6	chap. 6.1 deleted, table 6 memory changed,	2019-Feb-25	hjs

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Symbols

The following symbols may be used in this user guide

⚠ DANGER

DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.

⚠ WARNING

WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.

NOTICE

NOTICE indicates a property damage message.

⚠ CAUTION

CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.



Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.



ESD Sensitive Device!

This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.



HOT Surface!

Do NOT touch! Allow to cool before servicing.



Laser!

This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.



This symbol indicates general information about the product and the user guide.

This symbol also indicates detail information about the specific product configuration.



This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠ CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠ CAUTION



Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠ CAUTION

Danger of explosion if the battery is replaced incorrectly.

- ▶ Replace only with same or equivalent battery type recommended by the manufacturer.
- ▶ Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit <http://www.kontron.com/about-kontron/corporate-responsibility/quality-management>.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- ▶ Reduce waste arising from electrical and electronic equipment (EEE)
- ▶ Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- ▶ Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- ▶ Improve the environmental performance of all those involved during the lifecycle of EEE



Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

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1/ Introduction

The CP3005-SA is a highly integrated 3U CompactPCI® processor board based on the 8th generation Intel® Core i5 and Xeon processors in combination with the appropriate Chipset.

With two to six core processors, the CP3005-SA offers extraordinary performance-per-watt values and highest graphics performance. The CP3005-SA is a highly integrated 3U CompactPCI CPU.

Key Feature Overview:

- ▶ 3U CompactPCI CPU blade with 2, 4 or 6- core CPU options
- ▶ Based on 8th Gen Intel® Core technology
- ▶ Processors are
 - ▶ Xeon 6C/12T, vPro, ECC 45W/35W,
 - ▶ Core i5, 4C/8T, vPro, non ECC, 45W/35W
- ▶ Up to 32GB DDR4-2400 with ECC memory via 2x SODIMM sockets
- ▶ M.2 module for onboard data storage
- ▶ Optional TPM support
- ▶ Up to 3x Gigabit Ethernet, WOL support
- ▶ Version for extended temperature range E1X (-40°C up to 70°C)
- ▶ Up to 3x independent graphics outputs
- ▶ SATA Gen 3 & USB 3.0 support
- ▶ Two High Speed Extension connectors for easy customization
- ▶ Support of "Controllable TDP" SW feature
- ▶ Rear I/O compliant to CP305/CP307/CP308/CP3002/CP3003/CP3004 boards

The board is offered with various board support packages including Windows, VxWorks and Linux operating systems. For further information concerning the operating systems available for the CP3005-SA, please contact Kontron.

Figure 1: CompactPCI-Board CP3005-SA



2/ System Expansion Capabilities

2.1. MMEXT05 Module with 8 Horizontal Pitches (HP)

The MMEXT05 module for the 8HP CP3005-SA version provides various I/O ports. On the front panel, it includes two DisplayPort connectors, one Gigabit Ethernet port, one USB 3.0 port, and one RS-232 COM port. Onboard ports include one SATA connector for SATA 2.5" HDD or SSD devices as well as a M.2 card socket. For further information about the MMEXT05 module, refer to Chapter 7/.

2.2. MMEXT-XMC02 Module (8HP)

The MMEXT-XMC02 module for the 8HP CP3005-SA version provides one XMC mezzanine interface for support of one x8, x4 or x1 PCI Express 2.0 XMC module. Support of one XMC module with two x4 or x1 PCI Express 2.0 interfaces is also provided upon request. In addition, the MMEXT-XMC02 module provides a M.2 socket for a SSD module (type: 2280).

For further information about the MMEXT-XMC02 module, refer to Chapter 8/.

2.2.1. CP-RI03-04 Rear I/O Module (4HP/8HP) and CP-RI03-04S

The CP-RI03-04 rear I/O module has been designed for use with the CP3005-SA board from Kontron and provides comprehensive rear I/O functionality.

For further information about the CP-RI03-04 rear I/O module with 4HP, refer to Chapter 9/.

For further information about the CP-RI03-04 rear I/O module with 8HP, refer to Chapter 9/.

For further information about the CP-RI03-04S rear I/O module, refer to Chapter 10/.

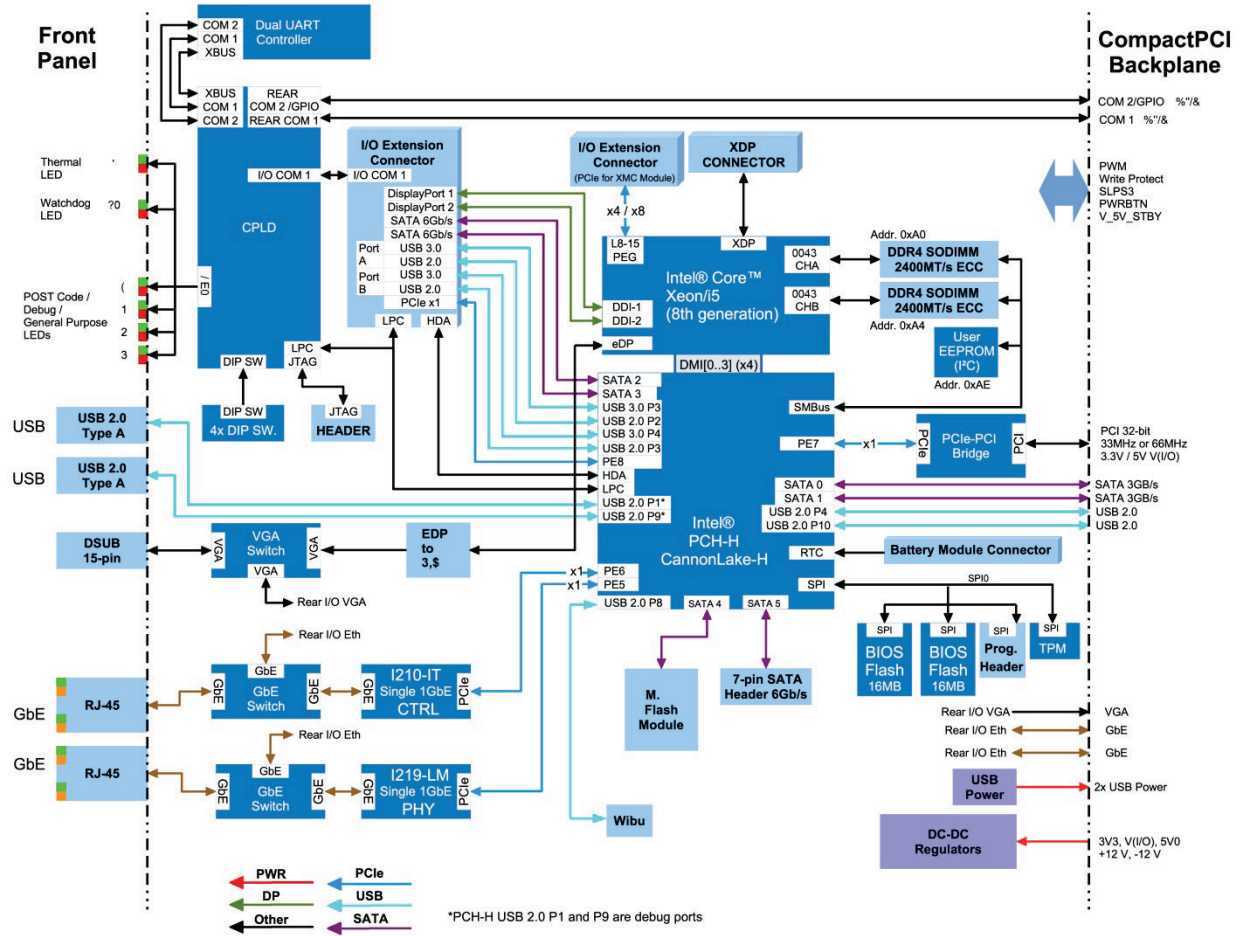
2.2.2. SATA SSD Flash Module

CP3005-SA provides support for SATA SSD Flash memory in combination with an optional M.2 storage device, connected to a respective onboard connector. Market available M.2 devices of suitable size and keying currently provide storage capacities of 32 GB up to 512 GB. The feature is available for 4HP as well as 8HP versions of CP3005-SA. For further information about the SATA Flash module, refer to Chapter 11/.

2.3. Block Diagram

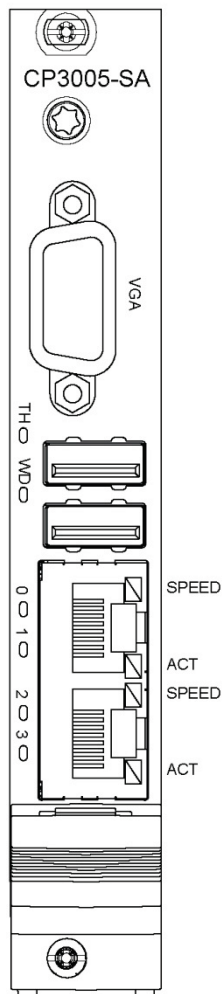
The following diagrams provide additional information concerning board functionality and component layout.

Figure 2: Block Diagram ((TO BE CHANGED))



2.4. Front Panel

Figure 3: 4HP CP3005-SA Front Panel with LED Status



System Status LEDs

TH (red/green): Temperature Status

WD (green): Watchdog Status

General Purpose LEDs

LED3..0 (red/green/red+green): General Purpose / POST Code

Note: If the General Purpose LEDs 3..0 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

Integral Ethernet LEDs

ACT (green): Ethernet Link/Activity

SPEED (orange): 1000BASE-T Ethernet Speed

SPEED (green): 100BASE-TX Ethernet Speed

SPEED (off) + ACT on: 10BASE-T Ethernet Speed

2.5. Board Layout

Figure 4: 4HP CP3005-SA Board Layout (Top View)

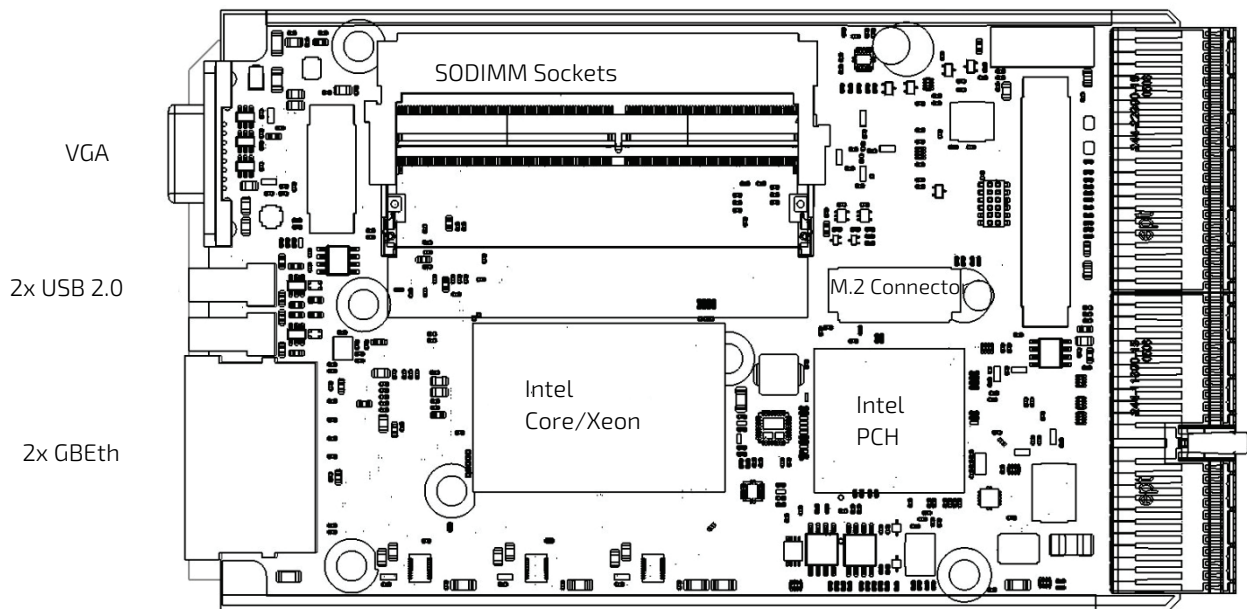
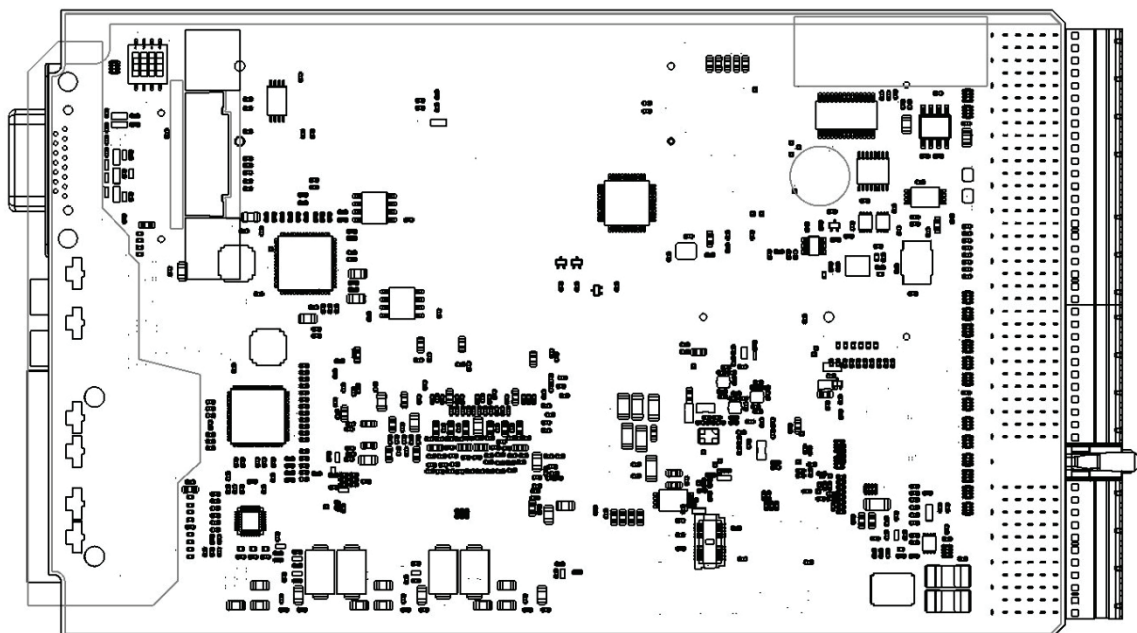


Figure 5: 4HP CP3005-SA Board Layout (Bottom View)



2.6. Technical Specification

Table 1: CP3005-SA Main Specifications

	Features	Specifications
Form factor	3U, 4HP CompactPCI (100 mm x 160 mm) 8HP with mezzanine	
Processor	CPU & Graphics Controller	The CP3005-SA supports the following processors: Xeon 6C/12T, 2.7 GHz, 45W Core i5, 4C/8T, 2.5 GHz, 45W
Chipset	PCH	Intel® QM370 Chipset for Core i5, CM246 for Xeon
Onboard Controllers	VGA Interface	Via eDP to VGA converter (CH7517)
	Gigabit Ethernet	2x Ethernet Controller (Intel® i210 and i219LM)
	Trusted Platform Module	TPM 2.0 Infineon SLB9670 using SPI WIBU CodeMeter ASIC 1504-03
	Embedded Controller	Altera MAX V 5M1270ZF256I5N (CPLD)
	Dual UART	EXAR XR16L2750
	PCIe-to-PCI bridge	CPCI: Pericom PI7C9X110
Memory	System Memory	Up to 32 GB DDR4 SDRAM memory with ECC running at 2400 MT/s, 1.2V on two SODIMM sockets
	BIOS Flash	2x 16 MB SPI boot flash chips for two separate uEFI BIOS images
	Customized EEPROM	I ² C EEPROM with 64 kbit
	Config Memories for Ethernet interfaces	i210: 16 Mbit SPI Flash
Interfaces	CompactPCI	32-bit/66MHz PCI interface with dedicated PCIe-to-PCI bridge System controller operation 3.3V or 5V signaling levels (universal signaling support) Hot Swap support: Passive mode hot swappable (automatic detection when plugged into the respective CompactPCI slot)
	Standard Rear I/O	The following interfaces are routed to the rear I/O connector J2: COM1 and COM2 (RS-232 signaling) 2x Gigabit Ethernet 2x SATA gen I (1.5 Gbit/s) CPCI RESET 4x GPIs and 4x GPOs (LVTTTL signaling), multiplexed with COM2
	Rear I/O with modules CP-RI003- 04 or CP-RI003-045	2x USB2.0 1x VGA
	Gigabit Ethernet	Two 10 BASE-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on one Intel® I219LM and one Intel® I210 Gigabit switchable to the front panel or the rear I/O
	USB	Two type A USB 2.0 connectors on the front panel, two USB 2.0 ports on the rear I/O module CP-RI003-04 One combined USB2.0/USB3.0 port on the MMEXT05 module

	Features	Specifications
	Serial	Two 16C550-compatible UARTs are available only with the rear I/O module CP-RIO03-04 CP3005-SA 8HP: One COM port to front I/O (with extension module MMEXT05) and one to rear I/O, or both COM ports to rear I/O module.
	SATA	Two SATA 6 Gb/s (gen 3) interfaces for: Onboard M.2 SSD socket One standard SATA 6 Gb/s (gen 3) interface for the standard SATA connector Two SATA 3 Gbit/s (gen 2) ports accessible via rear I/O High-performance RAID 0/1/5/10 functionality on all SATA ports
	XMC	XMC interface: XMC connector over the XMC Extension module to connect up to x8 PCI Express 2.0 ports operating at 5 GT/s
	I/O Extension	2x DisplayPort with Extension module MMEXT05, High Definition Audio (HDA), COM1 (with Extension module MMEXT05), 1x SATA 3 Gb/s 1x SATA 6 Gb/s 1x USB3.0 (with Extension module MMEXT05), LPC 1x PCIe x1
Sockets	Front Panel connectors	VGA: one 15-pin D-Sub connector USB: two type A connectors Ethernet: two 8-pin RJ-45 connectors
	Onboard connectors	2x Mezzanine connector for a I/O extension module 1x 7-pin standard SATA connector 1x SATA M.2 socket 1x JTAG connector for CPLD programming 1x XDP (debug) footprint: CMC_GEN1_MOUNTING_HOLE_DEBUG_PORT 1x 2-pin BTW connector for the battery module 2x 260-pin DDR4 SODIMM sockets SPI Flash debug/programming header
	CompactPCI connectors	Two CompactPCI connectors J1, J2
LEDs	System Status LEDs	Temperature LED, Watchdog status LED (green)
	General Purpose LEDs	LED3-0 (red/green/amber): General purpose / POST code
	Ethernet LEDs	ACT (green): Network link / activity SPEED (green/orange): Network speed
Switch	DIP Switch	One onboard DIP switch, SW1 for board configuration on the bottom side of the board
Timer	Real-Time Clock	Real-time clock with 256 Byte CMOS RAM; battery-backup available
	Watchdog Timer	Software-configurable, two-stage Watchdog with programmable timeout settings. The timeout values range from 125 ms to 4096 s. The Watchdog serves for generating an IRQ and/or a hardware reset.

	Features	Specifications
	System Timer	The processor contains three 8254-style counters with fixed uses. In addition to the three 8254-style counters, the CPU includes eight individual high-precision event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.
Thermal Management	Temperature Sensors	One thermal sensor (DTS) inside the CPU
	Heat sink	Specially designed heat sink
Security	TPM	Trusted Platform Module (TPM) 2.0 for enhanced hardware- and software-based data and system security
	WIBU	WIBU Optional available is a CodeMeter ASIC from WIBU for Digital Rights Management
Miscellaneous	Temperature Range	Operational: E1X: -40°C to +70°C
	Battery	3.0 V lithium battery for RTC with battery socket Battery type: UL-approved CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical refer to the battery manufacturer's specifications for exact range Storage (no load): -40°C to +70°C typical

2.7. Standards

This product complies with the requirements of the following standards.

Table 2: CP3005-SA Main Standards

Type	Aspect	Standard	Remarks
CE	Emission	EN55022, EN61000-6-3	
	Immunity	EN55024, EN61000-6-2	
	Electrical Safety	EN60950-1	
Mechanical	Mechanical Dimensions	IEEE 1102.1	The CP3005-SA will comply to IEEE 1102.1 (ANSI/VITA-30-199x)
Environmental	Climatic Humidity	IEC60068-2-78 (see note below)	
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS 2	Directive 2011/65/EU	Restriction of the use of certain hazardous substances in electrical and electronic equipment
	Vibration (Sinusoidal)	IEC60068-2-6	Test parameters: 10-300 (Hz) frequency range 5 (g) acceleration 1 (oct/min) sweep rate 10 cycles/axis 3 axes
	Single Shock	IEC60068-2-27	Test parameters:

Type	Aspect	Standard	Remarks
			30 (g) acceleration 9 (ms) shock duration half sine 3 number of shocks per direction (total: 18) 6 directions 5 (s) recovery time
	Bump Shock	IEC60068-2-29	Test parameters: 15 (g) acceleration 11 (ms) shock duration half sine 500 number of shocks per direction 6 directions 5 (s) recovery time

NOTICE

Customers desiring to perform further environmental testing of the CP3005-SA must contact Kontron for assistance prior to performing any such testing.

Boards without conformal coating must not be exposed to a change of temperature which can lead to condensation, as it may cause irreversible damage especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

3/ Functional Description

3.1. Processor

The CP3005-SA supports the Intel® Core i5-8400H and the Intel® Xeon® E-2176M processors in combination with the mobile Intel® QM370 Express Chipset.

Table 3: Features of the Processors Supported on the CP3005-SA

Processor	Cores/Threads	Frequency nom./Turbo	Cache	TDP/T _{Junction}	Graphics
Core i5-8400H	4/8	2.5/4.2 GHz	8 MByte Smart Cache	45 W/100°C	UHD- Graphics 630
Xeon® E-2176M	6/12	2.7/4.4 GHz	12 MByte Smart Cache	45 W/100°C	UHD- Graphics P630

3.2. Integrated Processor Graphics Controller

The 8th gen. Intel® Core™ i5/Xeon processor includes a highly integrated processor graphics controller delivering high-performance 3D and 2D graphics capabilities. The integrated processor graphics controller provides with Extension module MMEXT05 three digital ports capable of driving the following resolutions:

Table 4: Features of the Processors Graphics

Processor Graphics	max Resolution DP
UHD-Graphics P630	4096x2304@60 Hz
UHD- Graphics 630	4096x2304@60 Hz

NOTICE

The CP3005-SA supports with Extension module MMEXT05 up to two DisplayPort interfaces. The board supports up to three displays (1x VGA + 2x DP).

3.3. Chipset

The CP3005-SA is a two-chip solution implementing the CPU with CM246 and QM370 Platform Controller Hub. The following table lists the PCH QM370 and CM246 features.

Table 5: PCH QM370 and CM246 Features

Feature	QM370	CM246
USB Configuration	10x total USB 3.1 ports: - up to 6 USB 3.1 Gen 2 Ports - up to 10 USB 3.1 Gen 1 Ports 14 USB 2.0 Ports	10x total USB 3.1 ports: - up to 6 USB 3.1 Gen 2 Ports - up to 10 USB 3.1 Gen 1 Ports 14 USB 2.0 Ports
Displays	3	3
PCIe lanes	20	24
PCIe Configurations	x1, x2, x4	x1, x2, x4
Smart Sound	yes	yes
vPRO Technology	yes	yes
TDP	3 W	3 W
SATA Ports	4	8

3.4. System Memory

The CP3005-SA supports a dual DDR4 memory interface with one SO-DIMM socket per channel. The sockets support the following system memory features.

Table 6: System Memory

Feature	Remark
Socket	2x/4x SO-DIMM DDR4
Memory Type	standard: 2x SO-DIMM DDR4, max 16 GB per DIMM 2133/2400 MHz non-ECC/ECC extended: 4x SO-DIMMs DDR4, max 16 GB per DIMM 2133/2400 MHz non-ECC/ECC
Memory Module Size	4 GB, 8GB, 16 GB

3.5. Watchdog Timer

The CP3005-SA provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps.

The Watchdog timer provides the following modes of operation:

- ▶ Timer-only mode
- ▶ Reset mode
- ▶ Interrupt mode
- ▶ Dual-stage mode

In dual-stage mode, a combination of both interrupt and reset is generated if the Watchdog is not serviced.

3.6. Battery

The CP3005-SA is provided with an UL-recognized CR2025, 3.0 V, "coin cell" lithium battery for the RTC. When a battery is installed, refer to the operational specifications of the battery as this determines the operating and storage temperature of the CP3005-SA.

NOTICE

The battery is mounted on a battery module (MMBAT02) on the CP3005-SA board or on the MMEXT05 extension module – but never on both devices.

3.7. Flash Memory

The CP3005-SA provides flash interfaces for the uEFI BIOS and a M.2 Flash module.

3.7.1. SPI Boot Flash for uEFI BIOS

The CP3005-SA provides two 2x 16 MB SPI boot flashes for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The fail-over mechanism for the uEFI BIOS recovery can be controlled via the DIP switch SW1, switch 2.

NOTICE

The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

3.7.2. M.2 Flash Module

The M.2 connector (Type 2242) can be used for a SSD flash module for operating system and data.

3.8. Trusted Platform Module

The CP3005-SA supports the Trusted Platform Module (TPM) 2.0. TPM 2.0 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. It is based on Infineon's SLB9670. Infineon's Trusted Platform Module (TPM) SLB9670 is featuring a fully TCG TPM 1.2/2.0 standard compliant module with a SPI interface. TPMs are widely used as a root of trust for platform integrity, remote attestation and cryptographic services.

3.9. Board Interfaces

3.9.1. Front Panel LEDs

The CP3005-SA provides two system status LEDs: one temperature status LED (TH LED) and one Watchdog status LED (WD LED). It also provides four General Purpose/POST code LEDs (LED3..0). Their functionality is described in the following sections.

3.9.1.1. System Status LEDs

Table 7: System Status LEDs Function on the CP3005-SA

LED	Color	State	Function
TH LED	red / green	Off	Power failure
		Green	Board in normal operation
		Red	CPU has reached maximum allowable operating temperature and the performance has been reduced
		Red blinking	CPU temperature above 125°C, CPU has been shut off. In this event, all General Purpose LEDs (LED3..0) are blinking red as well.
WD LED	red / green	OFF	Watchdog inactive
		Green	Watchdog active, waiting to be triggered
		Red	Watchdog expired

NOTICE

If the TH LED flashes red at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur and the processor has been shut off. To turn to normal operation, the power must be switched off and then on again.

3.9.1.2. General Purpose LEDs

The General Purpose LEDs (LED3..0) are designed to indicate the boot-up POST code after which they are available to the application. If the LED3..0 are lit red during boot-up, a failure is indicated. In this event, please contact Kontron for further assistance.

Table 8: General Purpose LEDs Function

LED	Color	Function During Boot-Up	Function During Uefi Bios Post (If Post Code Config. Is Enabled)	Function After Boot-Up
LED3	red	Power failure	--	General Purpose or Port 80 Default: General Purpose
	green	--	uEFI BIOS POST bit 3 and bit 7	
	red+green	--	--	
LED2	red	CPU catastrophic error	CPU catastrophic error	General Purpose or Port 80 Default: General Purpose
	green	--	uEFI BIOS POST bit 2 and bit 6	
	red+green	--	--	
LED1	red	Hardware reset	--	General Purpose or Port

LED	Color	Function During Boot-Up	Function During Uefi Bios Post (If Post Code Config. Is Enabled)	Function After Boot-Up
LED0	green	--	uEFI BIOS POST bit 1 and bit 5	80 Default: General Purpose
	red+green	--	--	
	red	uEFI BIOS boot failure	--	General Purpose or Port 80 Default: General Purpose
	green	--	uEFI BIOS POST bit 0 and bit 4	
	red+green	--	--	

NOTICE

The bit allocation for Port 80 is the same as for the POST code.

How to read the 8-Bit POST Code

Due to the fact that only 4 LEDs are available and 8 bits must be displayed, the POST code output is multiplexed on the General Purpose LEDs.

Table 9: POST Code Sequence

State	General Purpose Leds
0	All LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following is an example of the General Purpose LEDs' operation if the POST configuration is enabled.

Table 10: POST Code Example

	LED3	LED2	LED1	LED0	Result
High Nibble	off (0)	on (1)	off (0)	off (0)	0x4
Low Nibble	off (0)	off (0)	off (0)	on (1)	0x1
Post Code		0x41			

NOTICE

Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CP3005-SA does not boot, please contact Kontron for further assistance.

3.9.2. USB Interfaces

The CP3005-SA provides five USB ports:

- ▶ Two USB 2.0 ports on the front I/O
- ▶ Two USB 2.0 ports on the CompactPCI rear I/O interface only with RIO-Modul CP-RIO3-04 4HP and 8HP, but not with CP-RIO3-04S.
- ▶ One USB 3.0 port on the high-speed I/O extension connector, J14, for the MMEXT05 extension module

NOTICE

Boards with a USB 3.0 flash drive installed on the front panel USB 3.0 port have been found to slightly exceed the electromagnetic interference limits. If permanent USB 3.0 type external storage is required to be connected to the USB 3.0 port, it is recommended to use an external hard disk drive.

On the front panel, the CP3005-SA has two standard, type A, USB 2.0 connectors, J5 and J6.

3.9.3. VGA Interface

The CP3005-SA provides one standard VGA interface for connection to a monitor. The VGA interface is implemented as a standard HD15 VGA connector, J4, on the front panel.

3.9.4. Serial Ports

The CP3005-SA provides two serial ports:

- ▶ COMA available either on the CompactPCI rear I/O connector (3.3V LVTTTL) or on the MMEXT05 extension module
- ▶ COMB on the CompactPCI rear I/O connector (3.3V LVTTTL)

COMA and COMB are fully compatible with the 16C550 controller and include a complete set of handshaking and modem control signals. The COMA and COMB ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

3.9.5. Gigabit Ethernet

The CP3005-SA board includes two 10/100/1000Base-T Ethernet ports based on one Intel i210-IT controller and one Intel i219-LM PHY. Both are connected to x1 PCIExpress interfaces of the PCH. These two on-board Gigabit Ethernet interfaces are individually switchable between front I/O and rear I/O and provide Wake-on-LAN support. In addition, one 10/100/1000Base-T Ethernet interface based on a intel i210-IT controller is available with the MMEXT05 module.

NOTICE

In order to use the Wake-on-LAN feature available only with the two Ethernet controllers, the power supply must not be switched off or the +5V stand-by voltage on the rear I/O module must be available. The CP3005-SA does not turn off the main power supply after an operating system shutdown in order to support Wake-on-LAN.

3.9.6. SATA Interfaces

The CP3005-SA provides six SATA ports:

- ▶ One SATA 6 Gb/s port on the onboard standard, 7-pin SATA connector, J3, for connection to SATA devices via cable
- ▶ One SATA 6 Gb/s port for the 2.5" HDD/SSD on the MMEXT05 extension module (8HP)
- ▶ Two SATA 3 Gb/s ports on the CompactPCI rear I/O interface

All six SATA interfaces provide high-performance RAID 0/1/5/10 functionality.

3.9.7. Debug Interface

The CP3005-SA provides several onboard options for hardware and software debugging, such as:

- ▶ Four bicolor general purpose LEDs (LED0 to LED3), which indicate hardware failures, uEFI BIOS POST codes and user-configurable outputs
- ▶ One JTAG connector, J13, for programming the onboard logic
- ▶ One CMC 35-pin ITP adapter port with XDP connector for processor debugging (J15)
- ▶ Two USB2.0-based debug ports, J5 and J6, for facilitating the debug of the operating system and the device driver

3.9.8. CompactPCI Interface

The CP3005-SA supports a flexible CompactPCI interface with a hot plug power interface (no PCI hot swap). In the system slot the PCI interface is in transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

3.9.8.1. Board Functionality when Installed in System Slot

In a system slot, the CompactPCI interface is provided as 32-bit/33 MHz (66 MHz upon request) PCI interface. The CP3005-SA supports up to seven peripheral slots through a CompactPCI backplane.

NOTICE

The PCI clock signals to unpopulated peripheral slots must be disabled by using the kboardconfig uEFI Shell command. This is essential to maintain conformity to the CE mark and the FCC EMI requirements. Please contact Kontron for further information.

NOTICE

The CP3005-SA supports universal PCI V(I/O) signaling voltages with one common resistor configuration. For both 5V and 3.3 V PCI signaling voltages, 2.7 kW pull-up resistors are used.

3.9.8.2. Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

3.9.8.3. Front/Rear I/O Configuration

The CP3005-SA is available in two versions:

- ▶ CP3005-SA front I/O version
- ▶ CP3005-SA rear I/O version

Please ensure that the correct version is stated on the order. If the CP3005-SA is ordered with rear I/O configuration, various I/O interfaces and signals are available via the CompactPCI connector J2, such as USB, SATA, GbE, VGA, COM, power and management signals. If the CP3005-SA is ordered with front I/O configuration, the I/O interfaces and signals mentioned above are isolated from the CompactPCI connector J2.

NOTICE

The CP3005-SA front I/O version does not provide 64-bit CompactPCI terminations to the backplane via the CompactPCI connector J2. With regard to this aspect, the CP3005-SA differs from previous boards such as CP307 or CP308 where 64-bit CompactPCI terminations are provided.

3.9.8.4. Board Insertion/Replacement under Power

The following features are implemented on the CP3005-SA:

- ▶ Power ramping
- ▶ ENUM signal handling (hot swapping of peripheral boards)

Power ramping on the CP3005-SA provides the hot plug functionality on the power interface. The PCI interface does not support hot swap functionality. No microswitch, no blue LED, and no signal precharge are provided on the CP3005-SA.

The ENUM signal on the CP3005-SA allows for hot swapping of peripheral boards with hot swap capability when the CP3005-SA is installed in the system slot.

NOTICE

The CP3005-SA itself is not hot swappable when inserted in a system slot. When inserted in a peripheral slot, the CP3005-SA is hot pluggable.

3.9.8.5. Power Ramping

On the CP3005-SA a special power controller is used to ramp up the onboard supply voltages. This is done to avoid transients on the +3.3V and +5V power supplies from the system. When the power supply is stable, the power controller generates an onboard reset to put the board into a defined state.

3.9.8.6. ENUM# Interrupt

If the board is operated in the system slot, the ENUM signal is an input.

4/ Configuration

4.1. DIP Switch Configuration

The quad DIP switch SW1 provides the following switches for board configuration: POST code indication, SPI boot flash selection, and uEFI BIOS configuration.

Figure 6: DIP Switch SW1

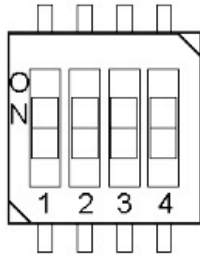


Table 11: DIP Switch SW1 Functionality

Switch	Setting	Functionality
1	OFF	Boot-up with POST code indication on LED3..0
	ON	Boot-up without POST code indication on LED3..0
2	OFF	Boot from the standard SPI boot flash
	ON	Boot from the recovery SPI boot flash
3	OFF	Standard QM370 reset implementation
	ON	Reset does a power cycle (reset event drops the QM370 PWROK input)
4	OFF	Boot using the currently saved uEFI BIOS settings
	ON	Clear the uEFI BIOS settings and use the default values

The default setting is indicated by using bold fonts.

To clear the uEFI BIOS settings and the passwords, proceed as follows:

1. Set DIP switch SW1, switch 4, to the ON position.
2. Apply power to the system.
3. Wait 30 seconds and then remove power from the system. During this time period no messages are displayed.
4. Set DIP switch SW1, switch 4, to the OFF position.

4.2. System Write Protection

The CP3005-SA provides write protection for non-volatile memories via the onboard configuration resistor JMP2 (R242) (only available upon request), the uEFI Shell, and the CompactPCI rear I/O connector J2, pin B15 (REAR_FANSENSE_SYS_WP#). If one of these sources is enabled, the system is write protected. Please contact Kontron for further information before using these functions.

4.3. CP3005-SA-Specific Registers

Table 12: CP3005-SA-Specific Registers

Address	Device
0x280	Status Register 0 (STAT0)
0x281	Status Register 1 (STAT1)
0x282	Control Register 0 (CTRL0)
0x283	Control Register 1 (CTRL1)
0x284	Device Protection Register (DPROT)
0x285	Reset Status Register (RSTAT)
0x286	Board Interrupt Configuration Register (BICFG)
0x287	Status Register 2 (STAT2)
0x288	Board ID High-Byte Register (BIDH)
0x289	Board and PLD Revision Register (BREV)
0x28A	Geographic Addressing Register (GEOAD)
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low-Byte Register (BIDL)
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292	General Purpose Output Register (GPOUT)
0x293	General Purpose Input Register (GPIN)

4.3.1. Status Register 0 (STAT0)

The Status Register 0 holds general / common status information.

Table 13: Status Register 0 (STAT0)

Address	0x280							
Bit	7	6	5	4	3	2	1	0
Name	Reserved	BBEI	BFSS		DIP4	DIP3	DIP2	DIP1
Access	R	R	R		R	R	R	R
Reset	0	0	N/A		N/A	N/A	N/A	N/A

Bitfield	Description
6	BBEI uEFI BIOS boot end indication: 0 = uEFI BIOS is booting 1 = uEFI BIOS boot is finished
5 - 4	BFSS SPI boot flash selection status: 00 = Standard SPI boot flash active 01 = Recovery SPI boot flash active 10 = External SPI boot flash active 11 = Reserved
3	DIP4 DIP switch SW1, switch 4 (clear the uEFI BIOS settings): 0 = Switch on (clear the uEFI BIOS settings) 1 = Switch off (boot using the currently saved uEFI BIOS settings)

Bitfield	Description
2	DIP3 DIP switch SW1, switch 3 (reset configuration): 0 = Switch on (reset does a power cycle) 1 = Switch off (standard reset configuration)
1	DIP2 DIP switch SW1, switch 2 (select SPI flash): 0 = Switch on (boot from recovery SPI boot flash) 1 = Switch off (boot from standard SPI boot flash)
0	DIP1 DIP switch SW1, switch 1 (POST code indication on LED0..3): 0 = Switch on (boot-up without POST code indication on LED0..3) 1 = Switch off (boot-up with POST code indication on LED0..3)

4.3.2. Status Register 1 (STAT1)

The Status Register 1 holds board-specific status information.

Table 14: Status Register 1 (STAT1)

Address	0x281							
Bit	7	6	5	4	3	2	1	0
Name	C66EN	Reserved			CSYS	CENUM	CFAL	CDEG
Access	R	R			R	R	R	R
Reset	N/A	000			N/A	N/A	N/A	N/A

Bitfield	Description
7	C66EN CPCI PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz
3	CSYS CPCI system slot identification (SYSEN signal): 0 = Installed in a system slot 1 = Installed in a peripheral slot
2	CENUM CPCI system enumeration (ENUM signal): 0 = Indicates the insertion or removal of a hot swap peripheral board when the CP3005-SA operates as the system controller board 1 = No hot swap event
1	CFAL CPCI power supply status (FAL signal): 0 = Power supply failure 1 = Power in normal state
0	CDEG CPCI power supply status (DEG signal): 0 = Power derating 1 = Power in normal state

4.3.3. Control Register 0 (CTRL0)

The Control Register 0 holds a series of bits defining general/common configuration functions.

Table 15: Control Register 0 (CTRL0)

Address	0x282							
Bit	7	6	5	4	3	2	1	0
Name	VGAM		BFUS		Reserved			
Access	R/W		R/W		R			
Reset	01		0		00000			

Bitfield	Description
7 - 6	VGAM DESCRIPTION 7 - 6 VGAM VGA mode configuration: 00 = Automatic VGA front detection 01 = Front VGA (uEFI BIOS default) 10 = Rear VGA 11 = VGA disabled
5	BFUS SPI boot flash selection: 0 = Select the standard SPI boot flash for update 1 = Select the recovery SPI boot flash for update

4.3.4. Control Register 1 (CTRL1)

The Control Register 0 holds a series of bits defining general/common configuration functions.

Table 16: Control Register 1 (CTRL1)

Address	0x283							
Bit	7	6	5	4	3	2	1	0
Name	VGAM		BFUS		Reserved			
Access	R/W		R/W		R			
Reset	01		0		00000			

Bitfield	Description
7	SRST SATA Flash module configuration: 0 = Reset of SATA Flash module 1 = SATA Flash module running
6	VRST Integrated processor graphics controller configuration: 0 = Processor graphics controller disabled 1 = Processor graphics controller enabled
5	TRST Trusted Platform Module (TPM) configuration: 0 = TPM disabled 1 = TPM enabled
4	CRST CPCI reset input when the CP3005-SA is in a peripheral slot:

Bitfield	Description
	0 = Disable CPCI reset to board 1 = Enable CPCI reset to board
2	SCOMA COMA routing selection: 0 = Rear I/O 1 = Extension module

NOTICE

The reset value of the SCOMA bit depends on the board version ordered. If the CP3005-SA is ordered as a rear I/O version, the reset value is 0. If the CP3005-SA is ordered as a front I/O version, an automatic switch over to the 8HP extension module is processed per default.

4.3.5. Device Protection Register (DPROT)

The Device Protection Register holds the write protect signals for non-volatile devices.

Table 17: Device Protection Register (DPROT)

Address	0x284							
Bit	7	6	5	4	3	2	1	0
Name	SWP	Reserved			SFWP	JMP2	BSWP	SSWP
Access	R	R			R/W	R	R	R/W
Reset	0	000			0	0	0	0

Bitfield	Description
7	SWP System write protection status: 0 = Onboard non-volatile memory devices not write protected 1 = Onboard non-volatile memory devices write protected
3	SFWP SATA Flash module write protection status: 0 = SATA Flash module write protection included in system write protection 1 = SATA Flash module write protection not included in system write protection This bit is read-only if the system write protection bit is activated (SWP = '1').
2	JMP2 System write protection via configuration resistors JMP2: 0 = System not write protected via JMP2 1 = System write protected via JMP2
1	BSWP System write protection via backplane (SYS_WP#): 0 = System not write protected via backplane 1 = System write protected via backplane
0	SSWP System write protection via software: 0 = System devices not write protected via software 1 = System write protected via software Writing a '1' to this bit clears it. If this bit is set, it cannot be cleared.

4.3.6. Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 18: Reset Status Register (RSTAT)

Address	0x285							
Bit	7	6	5	4	3	2	1	0
Name	PORS	Reserved				FPRS	CPRS	WTRS
Access	R/W	R				R/W	R/W	R/W
Reset	N/A	0000				0	0	0

Bitfield	Description	
7	PORS	Power-on reset status: 0 = System reset generated by warm reset 1 = System reset generated by power-on (cold) reset Writing a '1' to this bit clears it.
2	FPRS	Front panel push button reset status (MMEXT05/MMEXT05-CMC02): 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears it.
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CompactPCI reset input 1 = System reset generated by CompactPCI reset input Writing a '1' to this bit clears it.
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears it.

NOTICE

The Reset Status Register is set to default values by power-on (cold) reset, not by a warm reset.

4.3.7. Board Interrupt Configuration Register (BICFG)

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing.

Table 19: Board Interrupt Configuration Register (BICFG)

Address	0x286							
Bit	7	6	5	4	3	2	1	0
Name	UICF	CFICF	CEICF	CDICF	Reserved		WICF	
Access	R/W	R/W	R/W	R/W	R		R/W	
Reset	1	0	0	0	00		00	

Bitfield	Description	
7	UICF	UART IRQ3 and IRQ4 interrupt configuration: 0 = IRQ3 and IRQ4 interrupt disabled 1 = IRQ3 and IRQ4 interrupt enabled
6	CFICF	CPCI fail signal interrupt configuration (FAL signal): 0 = IRQ5 disabled 1 = IRQ5 enabled
5	CEICF	CPCI enumeration signal interrupt configuration (ENUM signal): 0 = IRQ5 disabled 1 = IRQ5 enabled
4	CDICF	CPCI derate signal interrupt configuration (DEG signal): 0 = IRQ5 disabled 1 = IRQ5 enabled
1 - 0	WICF	Watchdog interrupt configuration: 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved

4.3.8. Status Register 2 (STAT2)

The Status Register 2 holds status information related to the rear I/O configuration.

Table 20: Status Register 2 (STAT2)

Address	0x287							
Bit	7	6	5	4	3	2	1	0
Name	Reserved		RCFG		MEZC			
Access	R		R		R			
Reset	00		N/A*		N/A*			

Bitfield	Description	
5 - 4	RCFG	Rear I/O configuration: 00 = Rear I/O disabled (CP3005-SA front I/O version) 01 = COMA, GPIO 10 = Reserved

Bitfield	Description
	11 = COMA, COMB
3 - 0	MEZC Mezzanine configuration: 0000 = None / Smart Extension Module 0001 = MMEXT-XMC02 extension module 0010 = MMEXT05 extension module 0011...FFFF = Reserved

* The default value depends on the CP3005-SA version ordered (front I/O or rear I/O) and the rear I/O module used.

4.3.9. Board ID High-Byte Register (BIDH)

Table 21: Board ID High-Byte Register (BIDH)

Address	0x288							
Bit	7	6	5	4	3	2	1	0
Name	BIDH							
Access	R							
Reset	0xB4							

Bitfield	Description
7 - 0	BIDH Board identification: CP3005-SA: 0xB430

NOTICE

The Board ID Low Byte Register is located at the address 0x28D.

4.3.10. Board and PLD Revision Register (BREV)

The Board and PLD Revision Register signals to the software when differences in the board and the Programmable Logic Device (PLD) require different handling by the software. It starts with the value 0x00 and will be incremented with each necessary change.

Table 22: Board and PLD Revision Register (BREV)

Address	0x289							
Bit	7	6	5	4	3	2	1	0
Name	BREV				PREV			
Access	R				R			
Reset	N/A				N/A			

Bitfield	Description
7 - 4	BREV Board revision
3 - 0	PREV PLD revision

4.3.11. Geographic Addressing Register (GEOAD)

The Geographic Addressing Register holds the CompactPCI geographic address (backplane-unique physical slot number).

Table 23: Geographic Addressing Register (GEOD)

Address	0x28A							
Bit	7	6	5	4	3	2	1	0
Name	Reserved				GA			
Access	R				R			
Reset	000				N/A			

Bitfield	Description	
7 - 5	Res	Reserved
4 - 0	GA	Geographic Address

4.3.12. Watchdog Timer Control Register (WTIM)

Table 24: Watchdog Timer Control Register (WTIM)

Address	0x28C							
Bit	7	6	5	4	3	2	1	0
Name	WTE	WMD		WEN/WTR	WTM			
Access	R/W	R/W		R/W	R/W			
Reset	0	00		0	0000			

Bitfield	Description	
7	WTE	WTE Watchdog timer expired status bit: 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.
6 - 5	WMD	Watchdog mode: 00 = Timer mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by WTM.
3 - 0	WTM	WTM Watchdog timeout settings: 0000 = 0.125 s 1000 = 32 s 0001 = 0.25 s 1001 = 64 s 0010 = 0.5 s 1010 = 128 s

Bitfield	Description
	0011 = 1 s 1011 = 256 s
	0100 = 2 s 1100 = 512 s
	0101 = 4 s 1101 = 1024 s
	0110 = 8 s 1110 = 2048 s
	0111 = 16 s 1111 = 4096 s

The CP3005-SA has one Watchdog timer function with a programmable timeout ranging from 125 milliseconds to 4096 seconds. Failure to strobe the Watchdog timer within the programmed timeout delay results in a system reset or an interrupt.

There are four possible modes of operation:

- ▶ Timer mode
- ▶ Reset mode
- ▶ Interrupt mode
- ▶ Dual-stage mode

After the initial CP3005-SA power-on, the Watchdog is not enabled. To operate the Watchdog, the mode and timeout period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a '1' to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to '1'. What happens after this depends on the mode selected. The four operational Watchdog timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer mode

In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a '1' to the WTR bit. In the event a timeout occurs, the WTE bit is set to '1'. This bit can be polled by the application and handled accordingly. Once a Watchdog timeout occurs, the Watchdog is deactivated (WEN bit gets reset to '0'). To continue using the Watchdog, write a '1' to the WTE bit to reset it, and then restart the Watchdog using WEN.

Reset mode

This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available, if necessary, to determine the status of the Watchdog prior to the reset.

Interrupt mode

This mode generates an interrupt if a Watchdog timeout occurs. Configure the Watchdog interrupt in the Board Interrupt Configuration Register (0x286), otherwise no interrupt will be generated. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred. Once a Watchdog timeout occurs, the Watchdog is deactivated (WEN bit gets reset to '0').

Dual-stage mode

This is a complex mode where in the event of a timeout two things occur:

- ▶ an interrupt is generated, and
- ▶ the Watchdog is retriggered automatically.

In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use. Configure the Watchdog interrupt in the Board Interrupt Configuration Register (0x286), otherwise no interrupt will be generated.

4.3.13. Board ID Low-Byte Register (BIDL)

Table 25: Board ID Low-Byte Register (BIDL)

Address	0x28D							
Bit	7	6	5	4	3	2	1	0
Name	BIDL							
Access	R							
Reset	0x30							

Bitfield	Description
7 - 0	BIDL Board identification: CP3005-SA: 0xB430

NOTICE

The Board ID High Byte Register is located at the address 0x288.

4.3.14. LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel General Purpose LEDs.

Table 26: LED Configuration Register (LCFG)

Address	0x290							
Bit	7	6	5	4	3	2	1	0
Name	Reserved				LCON			
Access	R				R/W			
Reset	0000				0000			

Bitfield	Description
3 - 0	LCON LED3..0 configuration: 0000 = POST Mode (LEDs build a binary vector to display the Port 80 value) 0001 = General Purpose Mode (LEDs are controlled via the LCTRL register) 0010 - 1111 = Reserved

NOTICE

Beside the configurable functions described above, LED3..0 fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. For further information on reading the 8-bit uEFI BIOS POST Code, refer to section 3.9.1.2.

4.3.15. LED Control Register (LCTRL)

The LED Control Register enables the user to switch on and off the front panel General Purpose LEDs.

Table 27: LED Control Register (LCTRL)

Address	0x291							
Bit	7	6	5	4	3	2	1	0
Name	LCMD				LCOL			
Access	R/W				R/W			
Reset	0000				0000			

Bitfield		Description
7 - 4	LCMD	LED command: 0000 = Get LED0 1000 = Set LED0 0001 = Get LED1 1001 = Set LED1 0010 = Get LED2 1010 = Set LED2 0011 = Get LED3 1011 = Set LED3 0100 - 0111 = Reserved 1100 - 1111 = Reserved
3 - 0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+Green 0100 - 1111 = Reserved

NOTICE

The LED Control Register can only be used if the General Purpose LEDs indicated in the "LED Configuration Register" are configured in General Purpose Mode. The status of certain LEDs can be obtained by writing a "Get LEDX" command where "x" is the LED number (color bits are ignored) followed by a simple read.

4.3.16. General Purpose Output Register (GPOUT)

The General Purpose Output Register holds the general purpose output signals of the rear I/O CompactPCI connector J2. This register can only be used if the CP3005-SA is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear transition module configuration signal on the CompactPCI connector J2.

Table 28: General Purpose Output Register (GPOUT)

Address	0x292							
Bit	7	6	5	4	3	2	1	0
Name	Reserved					GPO2	GPO1	GPO0
Access	R					R/W	R/W	R/W
Reset	00000					0	0	00

Bitfield		Description
2 - 0	GPO2..0	GPO2..0 General purpose output signals (3.3V LVTTTL): 0 = Output low 1 = Output high

4.3.17. General Purpose Input Register (GPIN)

The General Purpose Input Register holds the general purpose input signals of the rear I/O CompactPCI connector J2. This register can only be used if the CP3005-SA is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear transition module configuration signal on the CompactPCI connector J2.

Table 29: General Purpose Input Register (GPIN)

Address	0x293							
Bit	7	6	5	4	3	2	1	0
Name	Reserved			GPI4	GPI3	GPI2	GPI1	GPI0
Access	R			R	R	R	R	R
Reset	000			1	1	1	1	1

Bitfield	Description
4 - 0	GPI4..0 General purpose input signals (3.3V LVTTL): 0 = Input low 1 = Input high

NOTICE

The CP3005-SA provides pull-up resistors on the rear I/O signal pins GPI[4..0], which leads to the default setting "input high" if the inputs are not connected. The general purpose inputs support 3.3V LVTTL signaling only (not 5V-tolerant).

5/ Power Considerations

5.1. CP3005-SA Voltage Ranges

The CP3005-SA has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The system power supply must comply with the CompactPCI® specification.

The following table specifies the ranges for the input power voltage within which the board is functional.

Table 30: DC Operational Input Voltage Range

Input Supply Voltage	Absolute Range	Recommended Range
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+5 V STDBY (optional)	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.

NOTICE

Failure to comply with the instructions above may result in damage to the board or improper operation.

5.2. Power Consumption of the CP3005-SA

The goal of this description is to provide a method to calculate the power consumption for the CP3005-SA baseboard and for additional configurations. The processor and the memory dissipate the majority of the thermal power.

The power consumption measurements were carried out using the following testing parameters:

- ▶ CP3005-SA installed in the system slot of a Kontron 2-slot backplane with a CPA250-4530G power supply
- ▶ Two Ethernet ports (i210) connected in 1000Base-T mode
- ▶ 16 GB DDR3L SDRAM in dual-channel mode
- ▶ One self-powered USB 2.0 hub (for mouse and keyboard)

The operating systems used were uEFI Shell and Windows® 8.1, 64-bit. All measurements were conducted at an ambient temperature of 25 °C. The power consumption values indicated in the tables below can vary depending on the ambient temperature.

The power consumption was measured using the following the processors:

- ▶ Quad-core Intel® Core™ i7-5700EQ, 2.6 GHz, 6 MB L3 cache, GT2, Intel® HD Graphics 5600
- ▶ Dual-core Intel® Core™ i5-4410E, 2.9 GHz, 3 MB L3 cache, GT2, Intel® HD Graphics 4600
- ▶ Dual-core Intel® Core™ i3-4112E, 1.8 GHz, 3 MB L3 cache, GT2, Intel® HD Graphics 4600

The power consumption was measured using the following configurations:

- ▶ Workload uEFI Shell: For this measurement the processor cores were active, the graphics controller was in idle state (no application running).
- ▶ Workload Idle: For this measurement all processor cores and the graphics controller were in idle state (no application running).
- ▶ Workload Typical: For this measurement all processor cores were operating at maximum workload and the graphics controller was performing basic operation (e.g. dual-screen output configuration with no 3D graphics application running). These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.

- Workload Maximum: These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores and graphics controller. These values are unlikely to be reached in real applications.

Table 31: CP3005-SA Power Consumption

Workload	Intel® Core™ i7-5700EQ 2.6 GHz	Intel® Core™ i5-4410E 2.9 GHz	Intel® Core™ i3-4112E 1.8 GHz
uEFI Shell	22.0 W	19.2 W	13.8 W
Idle	11.8 W	12.7 W	11.7 W
Typical	44.9 W	47.3 W	21.2 W

5.3. Power Consumption of CP3005-SA Accessories

The following table indicates the power consumption of the CP3005-SA accessories.

Table 32: Power Consumption of CP3005-SA Accessories

Module	Power Consumption
DDR3L SDRAM from one to two 18-chip memory modules (JEDEC raw card D)	approx. 5.8 W
SATA Flash module	less than 0.5 W
Gigabit Ethernet (per interface)	less than 0.5 W

5.4. Maximum Power Consumption of XMC Modules

A maximum power of 15 W is available on the XMC slot (located on the MMEXT-XMC02 module) and it can be arbitrarily divided on the 3.3 V and 5 V (VPWR) voltage lines. XMC modules are based on 3.3 V power along with variable power (VPWR) defined as either 5 V or 12 V in the ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard specification. On the CP3005-SA, the VPWR is configured to 5 V.

The following table indicates the current of a XMC module.

Table 33: XMC Module Current

Voltage	Continuous Current	Peak Current
3.3 V	0.75 A	1.0 A
5 V (VPWR)	2.5 A	3.0 A
+12 V	0.6 A	0.8 A

NOTICE

XMC integrators should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation of an XMC module on the 8HP CP3005-SA with MMEXT-XMC02 extension module.

5.5. Current Limits

The CP3005-SA has a hot swap controller for the +3.3V and +5V input voltage. The trip current limits in case of catastrophic failure are:

- +3.3 V: 16.5 A minimum, 21.9 A maximum
- +5 V: 33.0 A minimum, 43.8 A maximum

The maximum thermal operating current is 11.0 A for the +3.3 V supply and 17.6 A for the +5 V supply. The customer configuration/application shall not exceed these limits for a maximum operating ambient temperature of 60°C.

6/ Thermal Considerations

The thermal characteristic graphs shown in the following sections are intended to serve as guidance for reconciling the required computing power with the necessary system volumetric airflow over the ambient temperature. The graphs contain two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs without any intervention of thermal supervision (all four processors have a T_{JUNCTION} from 100°C). When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop (the CPU is at 130°C) in order to protect the CPU from thermal destruction (in this case the power must be switched off and then on again). In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 3.0 m/s or a volumetric flow rate of 15 CFM to 20 CFM is a typical value for a standard Kontron ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be determined for such environments.

How to read the diagram in Figures 7 and 9

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

How to read the diagram in Figure 8

Select a specific working point. For a given CPU frequency there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active by reducing the CPU frequency to protect the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in m³/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m³/h; 1 m³/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the thermal operational limits of the CP3005-SA taking into consideration power consumption vs. ambient air temperature vs. airflow rate.

NOTICE

The CP3005-SA must be operated within the thermal operational limits indicated below.

7/ MMEXT05 Extension Module

7.1. Overview

The MMEXT05 is a factory-installed mezzanine extension module which along with an 8HP front panel provides additional interfaces, such as:

- ▶ Two DisplayPorts
- ▶ One Gigabit Ethernet port
- ▶ One USB 3.0 port
- ▶ One COM port (RJ-45 connector)
- ▶ One Reset switch
- ▶ One SATA activity LED
- ▶ One onboard M.2 card socket (Socket 3, SATA-based, Key: M, Add-In-Card type: 2280)
- ▶ One onboard SATA HDD/SSD connector for connecting a 2.5" SATA HDD/SSD
- ▶ Battery socket

NOTICE

If a MMEXT05 module is used on the CP3005-SA, either the CP3005-SA or the MMEXT05 module may be equipped with a battery. Using one battery on the CP3005-SA and one on the MMEXT05 module simultaneously may result in premature discharge of the batteries.

7.2. Technical Specifications

Table 34: MMEXT05 Module Specifications

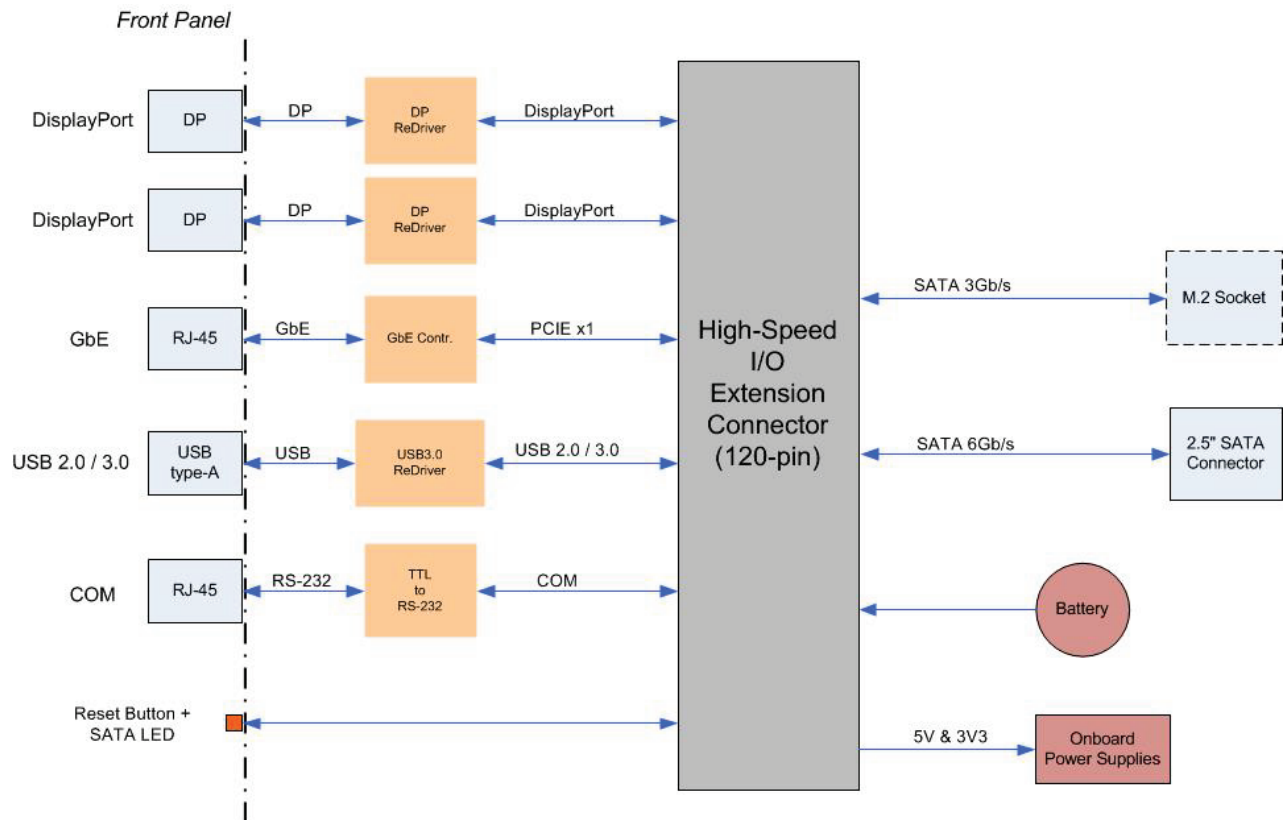
	Features	Specifications		
Front Panel Interfaces	DisplayPort	Two 20-pin DisplayPort connectors, J1 and J2, for connecting two monitors equipped with a DisplayPort interface (DVI / HDMI-capable through passive cable adapter)		
	Gigabit Ethernet	One 10 Base-T/100 Base-TX/1000 Base-T Ethernet interface based on the Intel® i210-IT Ethernet PCI Express bus controller: ▶ RJ-45 connector, J5 (GbE) ▶ Automatic mode recognition (Auto-Negotiation) ▶ Automatic cabling configuration recognition (Auto-MDI/X) ▶ Wake-on-LAN support		
	USB	One USB 3.0, type A connector, J7		
	Serial Port	One 16C550-compatible serial port, COM, RJ-45 connector, J8		
Onboard Interfaces	SATA	SATA connector, J6, for connecting a SATA 2.5" HDD/SSD (8HP)		
	M.2	One M.2 (Socket 3, SATA-based, Key: M) for 2280 SSD Add-In-Cards		
	Board-to-Board	One 120-pin connector (bottom-side) for connecting high-speed I/O extension connector to the MMEXT05 to the CP3005-SA		
LEDs/Switches	HDD LED	One LED (green) monitors SATA HDD/SSD activity		
	Front Panel Switch	Reset button, guarded		
General	Power Consumption	Power consumption without hard disk, M.2 card and peripheral devices connected: 200 mA at 3.3 V		
	Temperature Range	Operational:	0°C to +60°C	Standard
		Storage:	-40°C to +85°C	Without hard disk and without battery
			-40°C to +65°C	With hard disk
	Battery	3.0V lithium battery for RTC; Battery type: UL-recognized CR2025, Temperature ranges:		
		Operational (load, depends on battery type):	-20°C to +70°C	
		Storage (no load, depends on battery type):	-40°C to +70°C	
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)		
	Dimensions	MMEXT05: 100 mm x 160 mm, CP3005-SA with MMEXT05: 3U, 8HP, CompactPCI-compliant form factor		
	Board Weight	8HP CP3005-SA with MMEXT05: 459 grams (with heat sink, front panel, two 2 GB SODIMM memory modules and battery, but without M.2 card and without 2.5" HDD/SSD)		

NOTICE

When a battery is installed, refer to its operational specifications as this may limit the operating and storage temperature of the CP3005-SA.

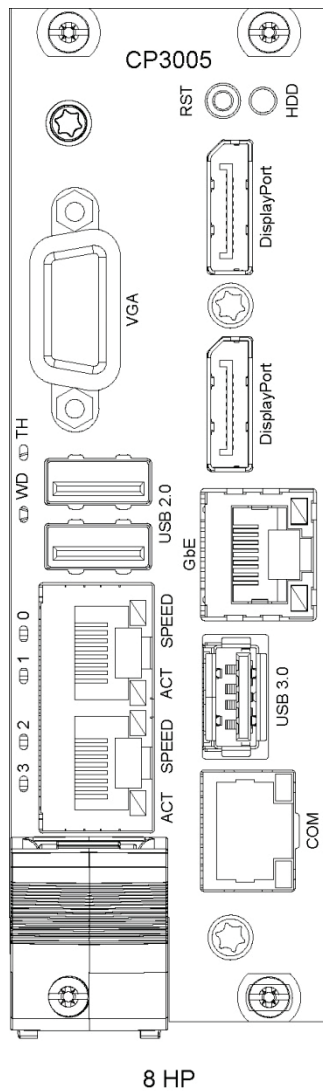
7.3. MMEXT05 Module Functional Block Diagram

Figure 7: MMEXT05 Module Functional Block Diagram



7.4. Front Panel of the CP3005-SA with MMEXT05 Module

Figure 6: Front Panel of the 8HP CP3005-SA with MMEXT05 Module



Watchdog and Overtemperature Status LEDs

WD (green):	Watchdog Status
TH (red/green):	Overtemperature Status

Integral Ethernet LEDs

ACT (green):	Ethernet Link/Activity
SPEED (green/orange/off):	Ethernet Speed

General Purpose LEDs

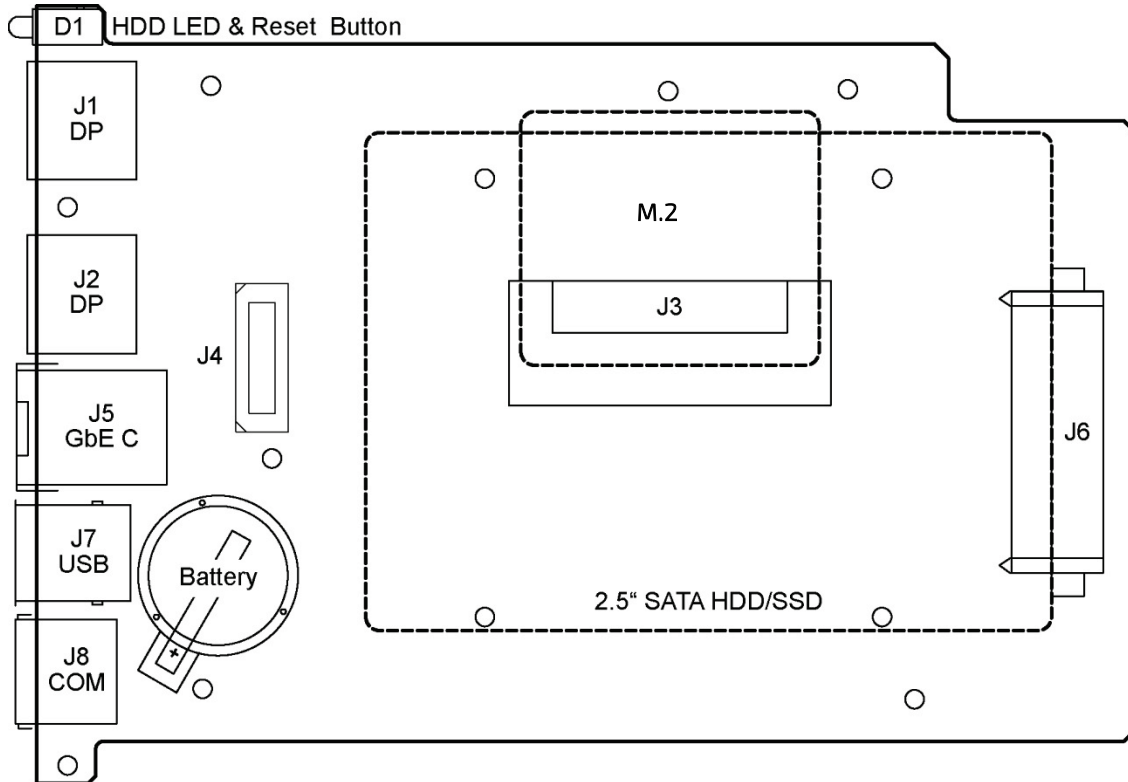
LED0..3 (red/green/red+green):	General Purpose / POST Code
--------------------------------	-----------------------------

NOTICE

If the General Purpose LEDs 0..3 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

7.5. MMEXT05 Module Layout

Figure 8: MMEXT05 Module Layout for 8HP Board Version (Top View)



7.6. Module Interfaces

7.6.1. DisplayPort Interfaces

The MMEXT05 provides two standard DisplayPort interfaces for connection to two monitors. The interfaces are implemented as standard DisplayPort connectors, J1 and J2, on the front panel.

7.6.2. Gigabit Ethernet Interface

The MMEXT05 extension module includes one 10Base-T/100Base-TX/1000Base-T Ethernet port based on one Intel® i210-IT Gigabit Ethernet controller, which is connected to the x1 PCI Express interfaces of the Chipset. The Wake-on-LAN feature is supported.

The Gigabit Ethernet interface is implemented as one standard, RJ-45 connector, J5 (GbE) on the front panel.

7.6.3. USB Interface

The MMEXT05 provides one standard, type A, USB 3.0 connector, J7.

NOTICE

Boards with a USB 3.0 flash drive installed on the front panel USB 3.0 port have been found to slightly exceed the electromagnetic interference limits. If permanent USB 3.0 type external storage is required to be connected to the USB 3.0 port, it is recommended to use an external hard disk drive.

7.6.4. Serial Port (J8)

One PC-compatible, serial RS-232 port (COM) is available, which is fully compatible with the 16C550 controller. This port includes a complete set of handshaking and modem control signals. Data transfer rates up to 115.2 kb/s are supported. The serial port is implemented as an 8-pin RJ-45 connector, J8.

Figure 9: Serial Port Connector J8

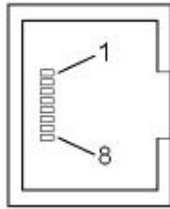


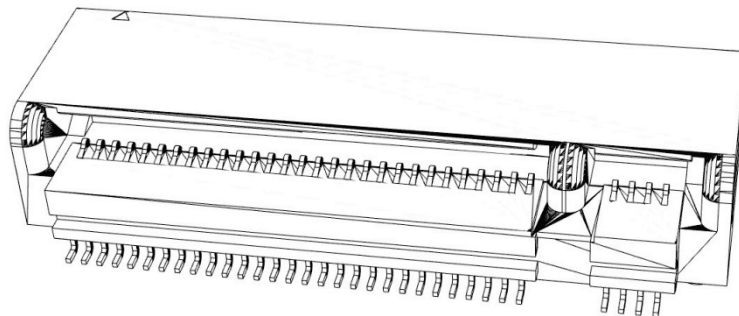
Table 35: Serial Port Connector J8 Pinout

Pin	Signal	Description	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data send request	I
8	CTS	Clear to send	I

7.6.5. M.2 Interface (J3)

To enable flexible flash expansion, a standard M.2 card socket is available on the MMEXT05. The socket is keyed in the M position. There is one position for the mounting screw, accepting 2280 sizes of M.2 modules.

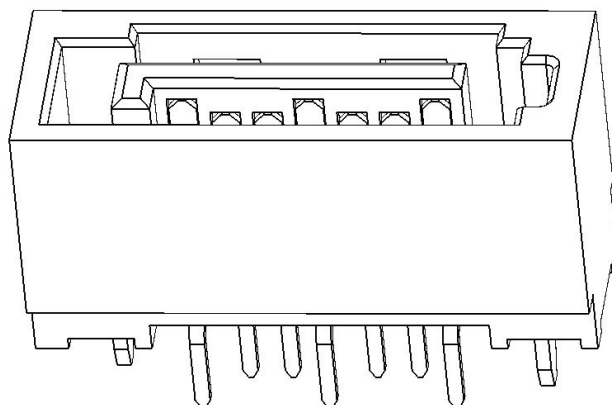
Figure 10: M.2 Connector



7.6.6. SATA Interface

The MMEXT05 extension module provides two SATA connectors, one 29-pin standard SATA connector, J6, for connection to 2.5" SATA HDD/SSD.

Figure 11: SATA Connector



8/ MMEXT-XMC02 Extension Module

8.1. Overview

The MMEXT-XMC02 is a factory-installed mezzanine extension module which along with an 8HP front panel provides additional interfaces, such as:

- ▶ One onboard XMC connector for connecting one x8, x4, or x1 PCI Express 2.0 XMC module over Highspeed Extension
- ▶ One onboard M.2 card socket (Socket 3, SATA-based, Key: M, Add-In-Card type: 2280)
- ▶ One Reset switch
- ▶ One SATA activity LED

NOTICE

XMC modules providing support for one x8 PCI Express 2.0 interface with up to 5.0 GT/s, compliant with the ANSI/VITA 42.0 and ANSI/VITA 42.3 specifications, and with a power consumption of up to 15 W can be used on the MMEXT-XMC02 module.

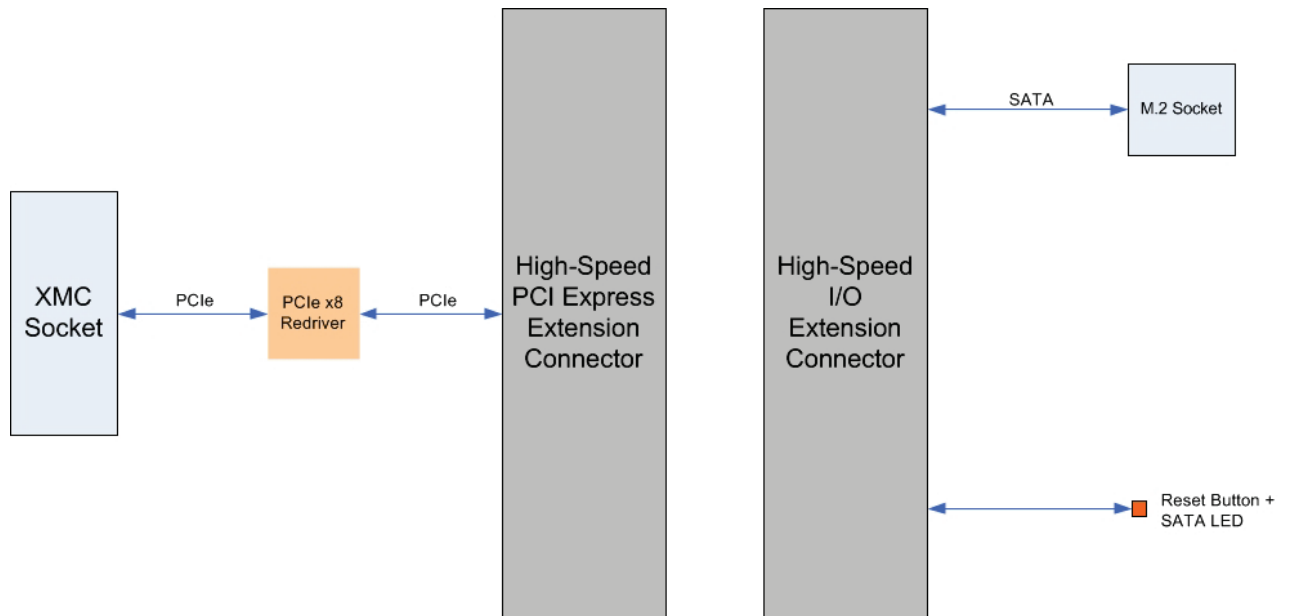
8.2. Technical Specifications

Table 36: MMEXT-XMC02 Module Specifications

	Features	Specifications
Onboard Interfaces	XMC	XMC interface for support of one x8, x4, or x1 PCI Express 2.0 XMC module via a standard XMC connector, J1
	M.2	One M.2 (Socket 3, SATA-based, Key: M) for 2280 SSD Add-In-Cards
	Board-to-Board	Two board-to-board connectors: ▶ One 60-pin, high-speed PCI Express extension connector, J5 ▶ One 120-pin, high-speed I/O extension connector, J6
LEDs/Switches	HDD LED	One LED (green) monitors SATA HDD/SSD activity
	Front Panel Switch	Reset button, guarded
General	Power Consumption	Power consumption without hard disk, CFast card and peripheral devices connected: ▶ 50 mA at 3.3 V ▶ 50 mA at 5 V
	Temperature Range	Operational: ▶ 0°C to +60°C, standard Storage: ▶ -40°C to +85°C, without battery
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	MMEXT05-CMC02: 100 mm x 160 mm CP3005-SA with MMEXT05-CMC02: 3U, 8HP CompactPCI-compliant form factor
	Board Weight	8HP CP3005-SA with MMEXT05-CMC02: 434 grams (with heat sink, front panel, and two 2 GB SODIMM memory modules, but without CFast card)

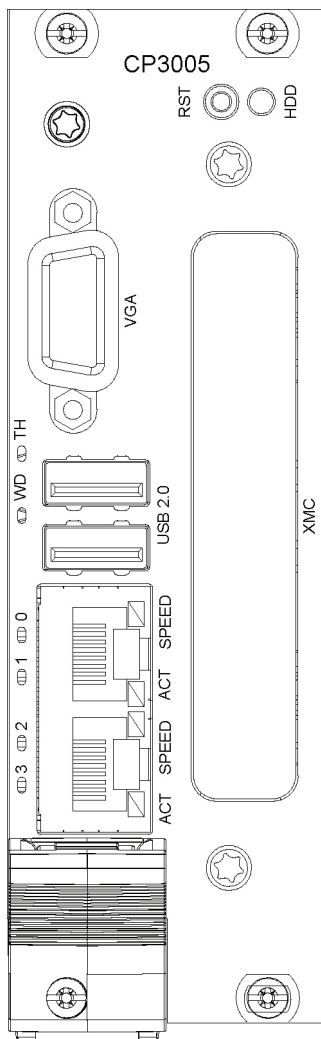
8.3. MMEXT-XMC02 Module Functional Block Diagram

Figure 12: MMEXT-XMC02 Module Functional Block Diagram



8.4. Front Panel of the CP3005-SA with MMEXT-XMC02 Module

Figure 13: Front Panel of the 8HP CP3005-SA with MMEXT-XMC02 Module



Watchdog and Overtemperature Status LEDs

WD (green): Watchdog Status
 TH (red/green): Temperature Status

Integral Ethernet LEDs

ACT (green): Ethernet Link/Activity
 SPEED (green / orange/off): Ethernet Speed

General Purpose LEDs

LED0..3 (red/green/red+green): General Purpose / POST Code

NOTICE

If the General Purpose LEDs 0..3 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

8.5. MMEXT-XMC02 Module Layout

Figure 14: MMEXT-XMC02 Module Layout for 8HP Board Version (Top View)

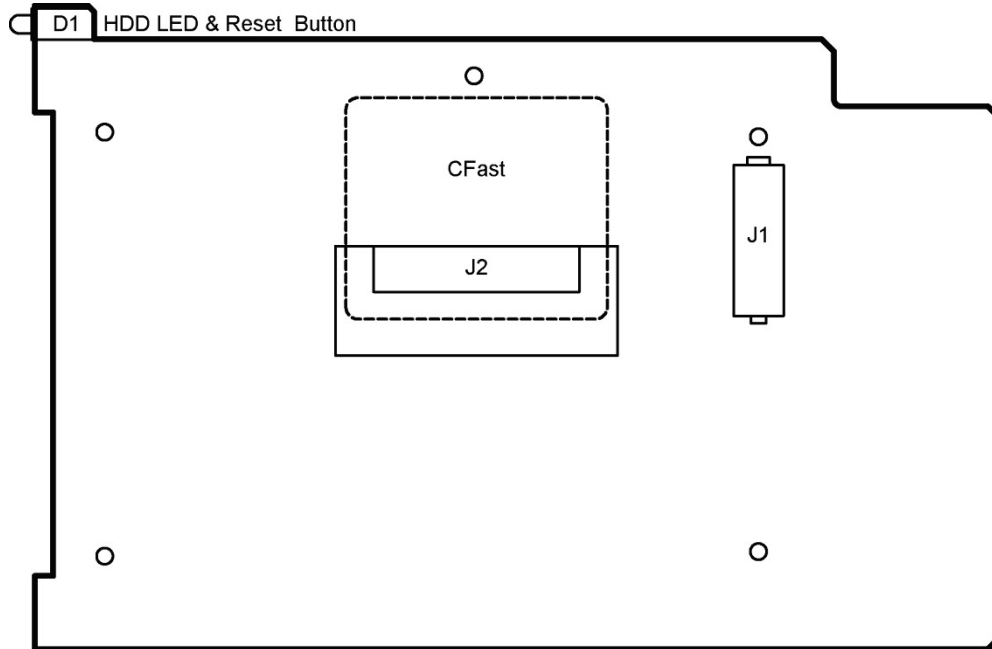
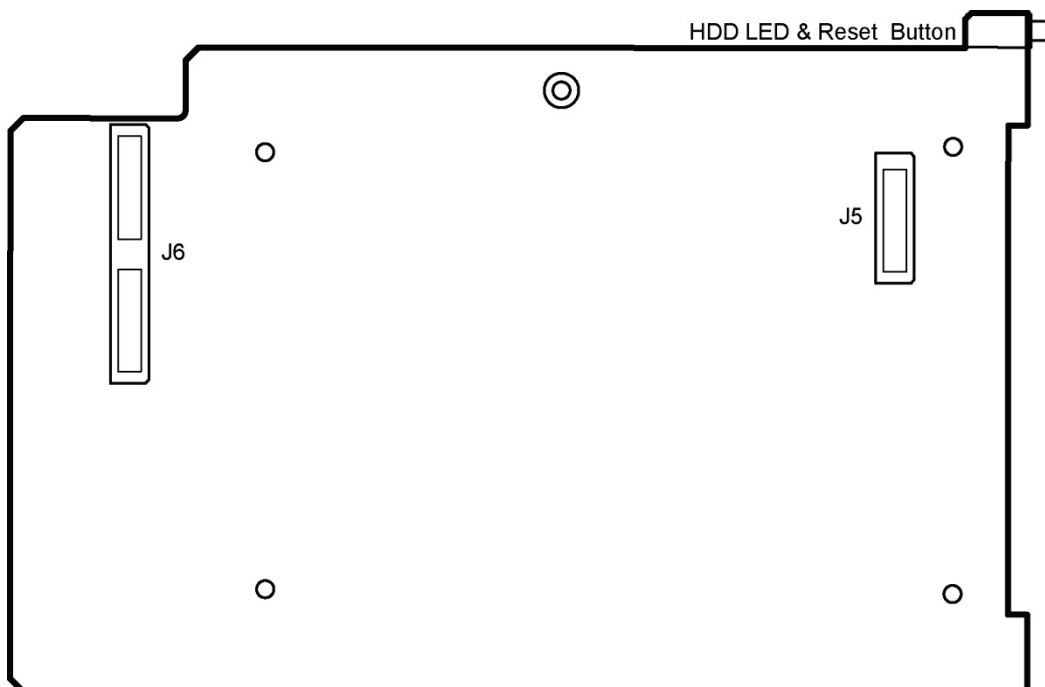


Figure 15: MMEXT-XMC02 Module Layout for 8HP Board Version (Bottom View)

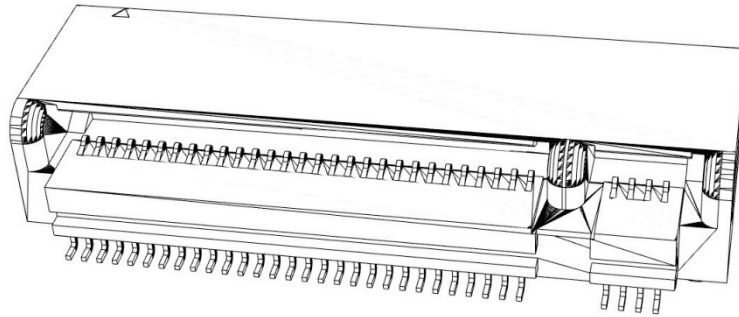


8.6. Module Interfaces

8.6.1. M.2 Interface (J2)

To enable flexible flash expansion, a standard M.2 card socket is available on the CP3005-SA. The socket is keyed in the M position. There is one position for the mounting screw, accepting 2280 sizes of M.2 modules.

Figure 16: M.2 Connector



8.6.2. XMC Interface

The MMEXT-XMC02 uses one x8 PCI Express 2.0 interface operating at up to 5.0 GT/s and compliant with the ANSI/VITA 42.0 and ANSI/VITA 42.3 specifications. It provides one standard XMC connector, J1, for connection to an XMC module. The MMEXT-XMC02 supports XMC modules with a maximum power consumption of 15 W.

9/ CP-RIO3-04 4HP and CP-RIO3-04 8HP Rear Transition Module

9.1. Overview

The CP3005-SA provides optional rear I/O connectivity for peripherals. Some standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connector J2 on the CP3005-SA. When the CP-RIO3-04 rear transition module is used, some signals of main board/front panel connectors are routed to the module interface.

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. The CP-RIO3-04 rear transition module provides the following interfaces.

- ▶ CompactPCI rear I/O
- ▶ Two USB 2.0 ports
- ▶ Two Gigabit Ethernet ports without LED signals
- ▶ Two COM ports
- ▶ One VGA analog port
- ▶ Two SATA ports
- ▶ Peripheral Control (Power supply management)

9.2. Technical Specifications

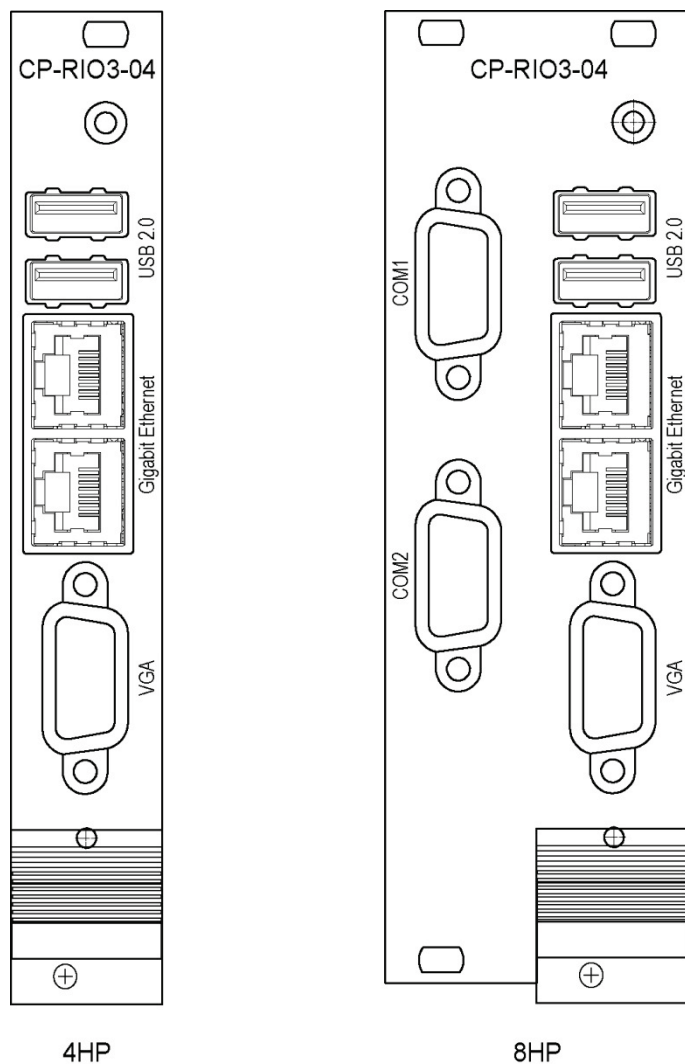
Table 37: CP-RIO3-04 Rear Transition Module Specifications

	Features	Specifications
External Interfaces	USB 2.0	Two USB 2.0 type A connectors, J11 and J12
	VGA	One VGA interface implemented as a 15-pin, D-Sub connector, J7
	Ethernet	Two Gigabit Ethernet interfaces implemented as a dual RJ-45 connector without LEDs, J10A/B
	Serial	Two onboard RS-232 serial ports with full modem support COMA (COM1) and COMB (COM2) implemented as: ▶ 10-pin onboard connectors J2 (COMA) and J3 (COMB) on the 4HP version ▶ 9-pin, D-Sub connectors, J2a (COMA) and J3a (COMB) on the 8HP version
Internal Interfaces	CompactPCI	CompactPCI connector, rJ2, for rear I/O backplane connection
	SATA	Two SATA interfaces implemented as two 7-pin, L-form standard SATA connectors
	Serial	Two COM ports (COMA and COMB) implemented as two 10-pin, 2.54 mm onboard connectors with full modem support, J2 (COMB) and J3 (COMA). On the 8HP version, the serial ports are routed to the front panel and implemented as two 9-pin, D-Sub connectors, J2a (COM1) and J3a (COM2).
	Peripheral Control	One 10-pin, 2.54 mm onboard connector for power supply management, J13
General	Temperature Range	Operational: 0°C to +60°C Storage: 55°C to +85°C

	Features	Specifications
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 80 mm
	Board Weight	4HP: 120 grams 8HP: 150 grams

9.3. Front Panels

Figure 17: CP-RIO3-04 4HP and 8HP Front Panels



9.4. CP-RI03-04 Rear Transition Module Layout

Figure 18: CP-RI03-04 4HP Rear Transition Module Layout

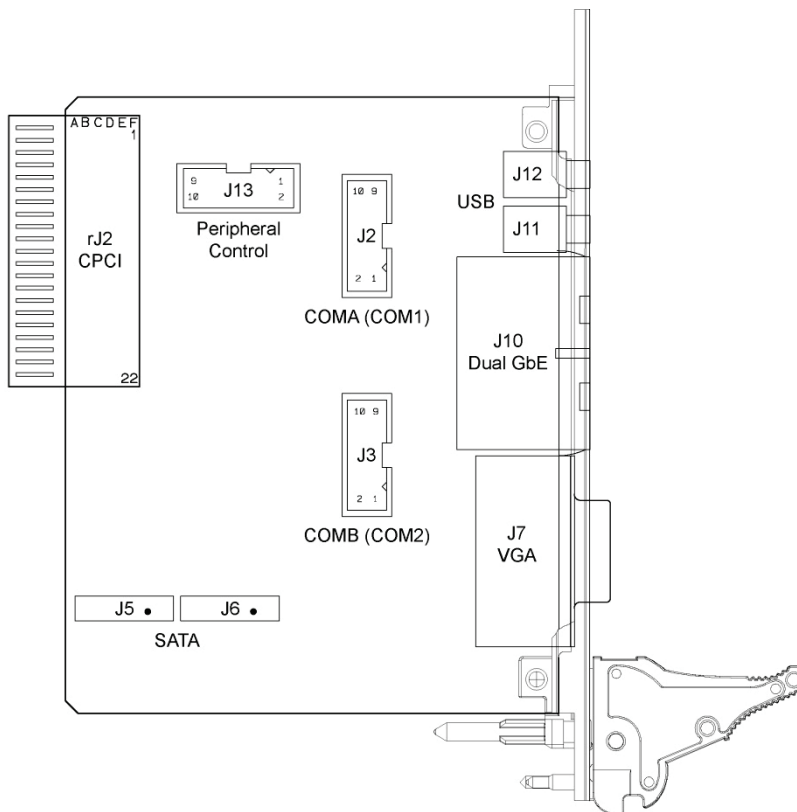
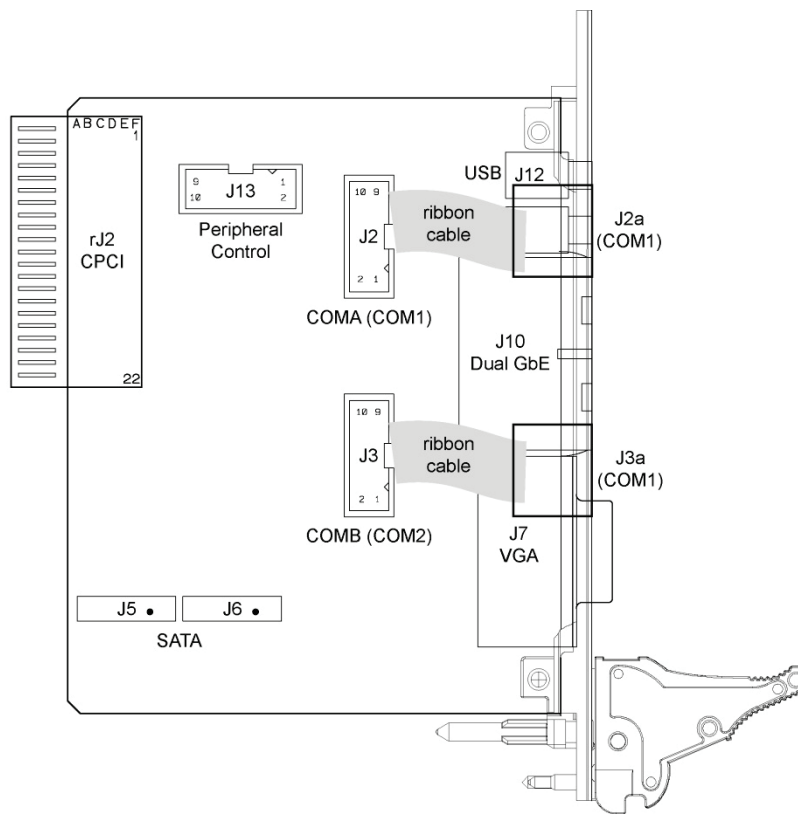


Figure 19: CP-RI03-04 8HP Rear Transition Module Layout



9.5. Module Interfaces

9.5.1. USB Interfaces

The CP-RI03-04 rear transition module provides two standard, type A, USB 2.0 connectors, J11 and J12, on the front panel.

9.5.2. VGA Interface

The CP-RI03-04 provides one standard VGA interface for connection to a monitor. The VGA interface is implemented as a standard VGA connector, J7, on the front panel.

9.5.3. Gigabit Ethernet Interface

The CP-RI03-04 provides two Gigabit Ethernet interfaces realized as RJ-45 connectors without LEDs. The status information of these both interfaces are indicated on the front Ethernet connector. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

9.5.4. COM Interface

The CP-RI03-04 rear transition module provides two identical COM ports for connection to RS-232 devices. On the 8HP version, the onboard 10-pin serial connectors J2 and J3 are routed to the 9-pin D-Sub COM connectors J2a and J3a located on the front panel. On the 4HP version, the COM signals are available only on the onboard 10-pin serial port connectors J2 and J3.

The following table provides pinout information for the onboard serial port connectors J2 and J3. Refer to the module layout for connector and pin locations.

Table 38: Serial Port Connectors J2 (COMB) and J3 (COMA) Pinout

Pin	Signal	Description	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

9.5.5. Peripheral Control Interface

A power supply with power management can be connected to the CP-RIO3-04 rear transition module via the peripheral control connector J13.

The following table provides pinout information for the peripheral control connector J13. Refer to the module layout for connector and pin locations.

Table 39: Peripheral Control Connector J13 Pinout

Pin	Signal	Description	I/O
1	GND	Signal ground	--
2	PWR_5VSTDBY	+5V standby power (optional)	I
3	RSV	Reserved	--
4	VCC5V	Power +5V	O
5	RSV	Reserved	--
6	VCC3V3	Power +3.3V	O
7	PWR_SLPS3#	Power supply sleep mode	O
8	GND	Signal ground	--
9	PWR_BTN#	Wake-up / sleep input	I
10	GND	Signal ground	--

9.5.6. SATA Interfaces

The onboard SATA connectors J5 and J6 allow the connection of standard HDDs/SSDs and other SATA devices to the CP-RIO3-04 rear transition module.

9.5.7. Rear I/O Interface on CompactPCI Connector rJ2

The CP-RI03-04 rear transition module conducts a wide range of I/O signals through the rear I/O connector rJ2.

NOTICE

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. Do not plug a rear I/O configured board in a backplane without rear I/O support. Failure to comply with the above will result in damage to your board.

Figure 20: Rear I/O CompactPCI Connector rJ2

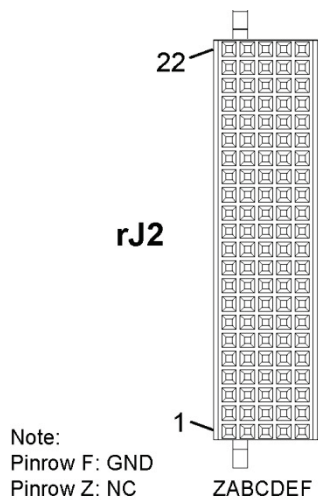


Table 40: Rear I/O CompactPCI Connector rJ2 Pinout

Pin	Z	A	B	C	D	E	F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	NC	GND	USBA+ /bi	USBB+ /bi	USBA_PWR_5V / in	GND
20	NC	NC	GND	USBA- /bi	USBB- /bi	USBB_PWR_5V / in	GND
19	NC	GND	GND	PWR_BTN# / out	PWR_SLP S3# / in	RIO_3.3V / in	GND
18	NC	COMA_RXD / out	COMA_DCD# / out	COMA_DTR# / in	COMB_CTS# / out	COMA_CTS# / out	GND
17	NC	COMA_TXD / in	COMB_RXD / out	NC	NC	NC	GND
16	NC	COMA_DSR# / out	COMA_RTS# / in	NC	RSV	COMA_RI# / out	GND
15	NC	PWR_5VSTDBY / out	RSV	NC	NC	NC	GND
14	NC	IPA_DA+ /bi	IPA_DA- /bi	COMB_RTS# / in	IPA_DC+ / bi	IPA_DC- /bi	GND

Pin	Z	A	B	C	D	E	F
13	NC	IPA_DB+/bi	IPA_DB-/bi	COMB_RI#/out	IPA_DD+/bi	IPA_DD-/bi	GND
12	NC	IPB_DA+/bi	IPB_DA-/bi	RIO_XFO_CT	IPB_DC+/bi	IPB_DC-/bi	GND
11	NC	IPB_DB+/bi	IPB_DB-/bi	COMB_DCD#/out	IPB_DD+/bi	IPB_DD-/bi	GND
10	NC	GND	COMB_TXD/in	VGA_RED/in	COMB_DTR#/in	GND	GND
9	NC	SATAATX+/in	GND	VGA_HSYNC/in	GND	SATABTX+/in	GND
8	NC	SATAATX-/in	GND	VGA_BLUE/in	GND	SATABTX-/in	GND
7	NC	GND	COMB_DSR#/out	VGA_DDC_DATA/bi	RSV	GND	GND
6	NC	SATAARX+/out	GND	VGA_GREEN/in	GND	SATABRX+/out	GND
5	NC	SATAARX-/out	GND	VGA_VSYNC/in	GND	SATABRX-/out	GND
4	NC	NC	RIO_5V/in	VGA_DDC_CLK/in	GPIO_CFG0/out	GND	GND
3	NC	NC	GND	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	NC	GND

NOTICE

The RIO_XXX signals are power supply INPUTS to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

Table 41: Rear I/O Signal Description

Signal	Description
COMAx	COMA port LVTTTL (3.3V)
COMBx	COMB port LVTTTL (3.3V)
GPIO_CFG0	GPIO or COMB configuration
IPx	Gigabit Ethernet copper port
SATAx	SATA port
USBx	USB interface and power
VGAx	VGA signal
RIOx/V(I/O)	Power supply signal
PWRx	Power management signal
RSV	Reserved
GND	Ground signal

10/ CP-RI03-04S Rear Transition Module

10.1. Overview

The rear variant CP3005-SA provides optional rear I/O connectivity for peripherals. Some standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connector J2 on the CP3005-SA. When the CP-RI03-04 rear transition module is used, some signals of main board/front panel connectors are routed to the module interface.

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. The CP-RI03-04S rear transition module provides the following interfaces.

- ▶ Two Gigabit Ethernet ports without LED signals
- ▶ One COM port
- ▶ One VGA analog port
- ▶ Two SATA ports
- ▶ CompactPCI rear I/O
- ▶ Power Management

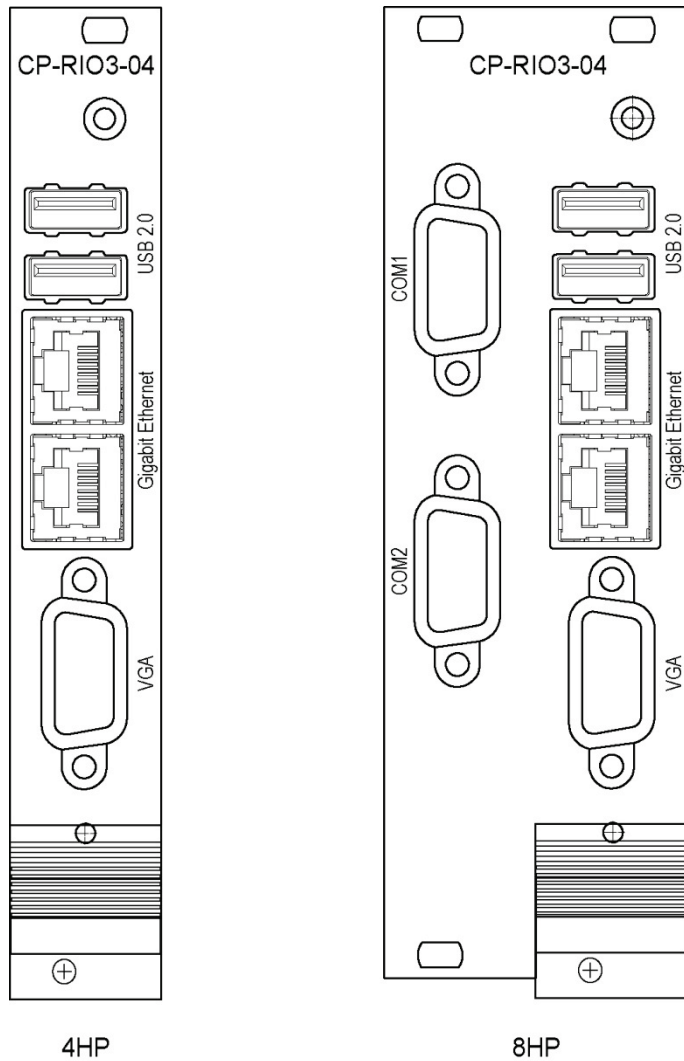
Technical Specifications

Table 42: CP-RI03-04S Rear Transition Module Specifications

	Features	Specifications
External Interfaces	VGA	One VGA interface implemented as a 15-pin, D-Sub connector, J7
	Ethernet	Two Gigabit Ethernet interfaces implemented as a dual RJ-45 connector without LEDs, J10A/B
	Serial	One onboard RS-232 serial ports with 8 pins (RJ45)
Internal Interfaces	CompactPCI	CompactPCI connector, J2, for rear I/O backplane connection
	SATA	Two SATA interfaces implemented as two 7-pin, L-form standard SATA connectors
	Serial	One COM port
	Peripheral Control	One 10-pin, 2.54 mm onboard connector for power supply management, J13
General	Temperature Range	Operational: 0°C to +60°C Storage: 55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 80 mm
	Board Weight	120 grams

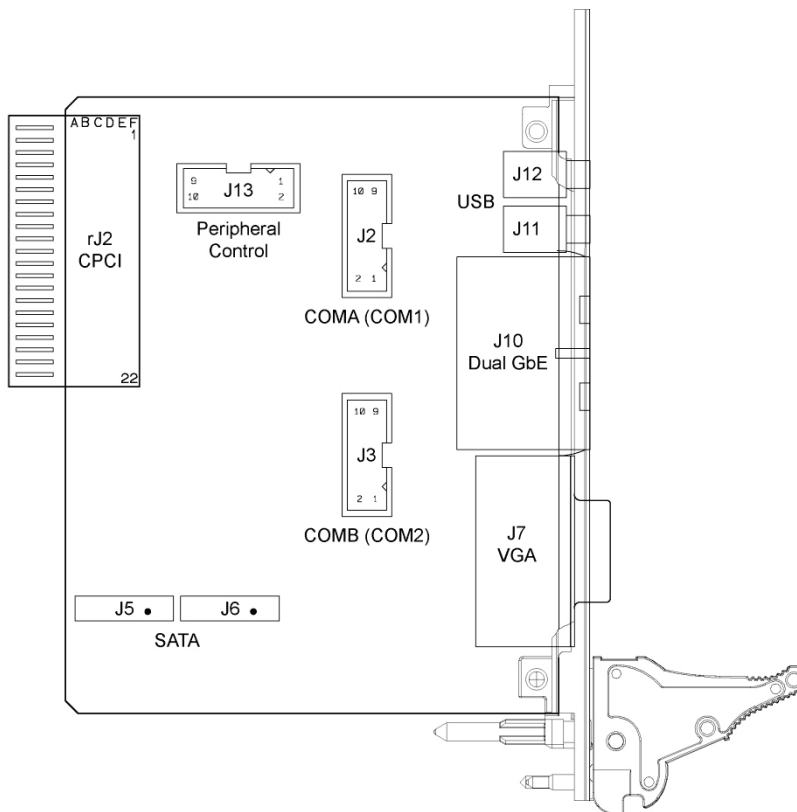
10.2. CP-RIO3-04S Front Panels

Figure 21: CP-RIO3-04S Front Panels



10.3. CP-RI03-04S Rear Transition Module Layout

Figure 22: CP-RI03-04S Rear Transition Module Layout



10.4. Module Interfaces

10.4.1. VGA Interface

The CP-RI03-04s provides one standard VGA interface for connection to a monitor. The VGA interface is implemented as a standard VGA connector, **J7**, on the front panel.

10.4.2. Gigabit Ethernet Interface

The CP-RI03-04S provides two Gigabit Ethernet interfaces realized as RJ-45 connectors without LEDs. The status information of these both interfaces are indicated on the front Ethernet connector. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

10.4.3. COM Interface

The CP-RI03-04S rear transition module provides one COM port for connection to RS-232 devices.

Table 43: Serial Port Connectors **J2 (COMB) and **J3 (COMA)** Pinout**

Pin	Signal	Description	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

10.4.4. Peripheral Control Interface

A power supply with power management can be connected to the CP-RI03-04S rear transition module via the peripheral control connector **J13**.

Table 44: Peripheral Control Connector **J13 Pinout**

Pin	Signal	Description	I/O
1	GND	Signal ground	--
2	PWR_5VSTDBY	+5V standby power (optional)	I
3	RSV	Reserved	--
4	VCC5V	Power +5V	O
5	RSV	Reserved	--
6	VCC3V3	Power +3.3V	O
7	PWR_SLP53#	Power supply sleep mode	O
8	GND	Signal ground	--
9	PWR_BTN#	Wake-up / sleep input	I

Pin	Signal	Description	I/O
10	GND	Signal ground	--

10.4.5. SATA Interfaces

The onboard SATA connectors **J5** and **J6** allow the connection of standard HDDs/SSDs and other SATA devices to the CP-RI03-04 rear transition module.

10.4.6. Rear I/O Interface on CompactPCI Connector **rJ2**

The CP-RI03-04S rear transition module conducts a wide range of I/O signals through the rear I/O connector **rJ2**.

NOTICE

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. Do not plug a rear I/O configured board in a backplane without rear I/O support. Failure to comply with the above will result in damage to your board.

Figure 23: Rear I/O CompactPCI Connector **rJ2**

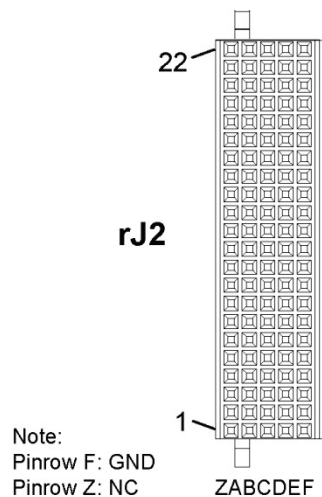


Table 45: Rear I/O CompactPCI Connector **rJ2** Pinout

Pin	Z	A	B	C	D	E	F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	NC	GND	USBA+ /bi	USBB+ /bi	USBA_PWR_5V/ in	GND
20	NC	NC	GND	USBA- /bi	USBB- /bi	USBB_PWR_5V/ in	GND
19	NC	GND	GND	PWR_BTN#/	PWR_SLP	RIO_3.3V/in	GND

Pin	Z	A	B	C	D	E	F
				out	S3#/in		
18	NC	COMA_RXD/out	COMA_DCD#/out	COMA_DTR#/in	COMB_CTS#/out	COMA_CTS#/out	GND
17	NC	COMA_TXD/in	COMB_RXD/out	NC	NC	NC	GND
16	NC	COMA_DSR#/out	COMA_RTS#/in	NC	RSV	COMA_RI#/out	GND
15	NC	PWR_5VSTDBY/out	RSV	NC	NC	NC	GND
14	NC	IPA_DA+/bi	IPA_DA-/bi	COMB_RTS#/in	IPA_DC+/bi	IPA_DC-/bi	GND
13	NC	IPA_DB+/bi	IPA_DB-/bi	COMB_RI#/out	IPA_DD+/bi	IPA_DD-/bi	GND
12	NC	IPB_DA+/bi	IPB_DA-/bi	RIO_XFO_CT	IPB_DC+/bi	IPB_DC-/bi	GND
11	NC	IPB_DB+/bi	IPB_DB-/bi	COMB_DCD#/out	IPB_DD+/bi	IPB_DD-/bi	GND
10	NC	GND	COMB_TXD/in	VGA_RED/in	COMB_DTR#/in	GND	GND
9	NC	SATAATX+/in	GND	VGA_HSYNC/in	GND	SATABTX+/in	GND
8	NC	SATAATX-/in	GND	VGA_BLUE/in	GND	SATABTX-/in	GND
7	NC	GND	COMB_DSR#/out	VGA_DDC_DATA/bi	RSV	GND	GND
6	NC	SATAARX+/out	GND	VGA_GREEN/in	GND	SATABRX+/out	GND
5	NC	SATAARX-/out	GND	VGA_VSYNC/in	GND	SATABRX-/out	GND
4	NC	NC	RIO_5V/in	VGA_DDC_CLK/in	GPIO_CFG0/out	GND	GND
3	NC	NC	GND	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	NC	GND

NOTICE

The RIO_XXX signals are power supply INPUTS to supply the rear I/O module with power. These pins MUST NOT be connected to any other power source, either within the backplane itself or within a rear I/O module. Failure to comply with the above will result in damage to your board.

Table 46: Rear I/O Signal Description

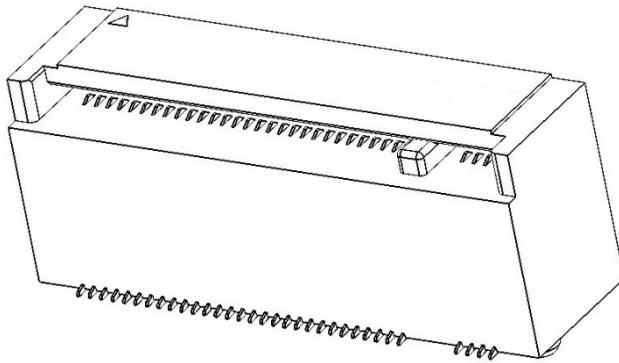
Signal	Description
COMAx	COMA port LVTTTL (3.3V)
COMBx	COMB port LVTTTL (3.3V)
GPIO_CFG0	GPIO or COMB configuration
IPx	Gigabit Ethernet copper port

Signal	Description
SATAx	SATA port
USBx	USB interface and power
VGAx	VGA signal
RIOx/V(I/O)	Power supply signal
PWRx	Power management signal
RSV	Reserved
GND	Ground signal

11/ SATA SSD Flash Module

The M.2 connector (Type 2242) on the CP3005-SA is meant to be used for a SSD flash module, e.g. for as hard disk for operating system and data. Keying "B" or "M", Type "S" (single sided) or "D" (double-sided) with heights from "1" to "4".

Figure 24: M.2 Connector



12/ Installation

This chapter is oriented towards an application environment. Some aspects may, however, be applicable to a development environment.

12.1. Safety

To ensure personnel safety and correct operation of this product, the following safety precautions must be observed:

All operations involving the CP3005-SA require that personnel be familiar with system equipment, safety requirements and the CP3005-SA.

This product contains electrostatically sensitive components which can be seriously damaged by electrical static discharge (ESD). Therefore, proper handling must be ensured at all times.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Do not touch components, connector-pins or traces.

Kontron assumes no liability for any damage resulting from failure to comply with these requirements.

12.2. Board Installation

The CP3005-SA is designed for use either as a CompactPCI system controller or as an autonomous CPU board in a CompactPCI peripheral slot.

When installed in the system slot, the CP3005-SA provides all required functions for supporting the hot swapping of peripheral boards which are capable of being hot swapped. In this configuration the CP3005-SA itself is not hot-swappable.

When installed in a CompactPCI peripheral slot, the CP3005-SA operates autonomously, meaning that it only draws power from the CompactPCI backplane. There is no interfacing with the CompactPCI bus, clocks or other control signals. In this configuration, the CP3005-SA supports hot plugging. This simply means that the board can be installed or removed from the system while under power.

NOTICE

Always ensure that all functions in progress are properly terminated or put into a safe state prior to hot plugging the CP3005-SA. Failure to comply with the above may result in improper operation or damage to other system components, e.g. operating system failure, data loss, uncontrolled processing, etc.

NOTICE

In order to use the hot plug function of the CP3005-SA, a hot swap-capable backplane is required.

12.2.1. Standard Board Insertion

Prior to following the steps below, ensure that the safety requirements are met.

To insert the CP3005-SA in a system proceed as follows:

1. Ensure that no power is applied to the system before proceeding.
2. Insert the board into the slot designated until it makes contact with the backplane connectors.
3. Using the ejector handle, engage the board with the backplane. When the ejector handle is closed, the board is engaged.

4. Fasten the front panel retaining screws.
5. Connect all external interfacing cables to the board as required.

12.2.2. Standard Board Removal

Prior to following the steps below, ensure that the safety requirements are met. When removing a board from the system, particular attention must be paid to the components which may be hot, such as heat sink, etc.

To remove the CP3005-SA from a system proceed as follows:

1. Ensure that no power is applied to the system before proceeding.
2. Disconnect any interfacing cables that may be connected to the board.
3. Unscrew the front panel retaining screws.
4. Unlock the ejector handle.
5. Disengage the board from the backplane by pressing the handle as required and remove the board from the system.

12.3. Installation of CP3005-SA Peripheral Devices

The CP3005-SA is designed to accommodate various peripheral devices, such as USB devices, SATA devices, a M.2 card, etc. The following figures show the placement of modules and peripheral devices on the CP3005-SA.

Figure 25: 4HP CP3005-SA with SATA Flash Module

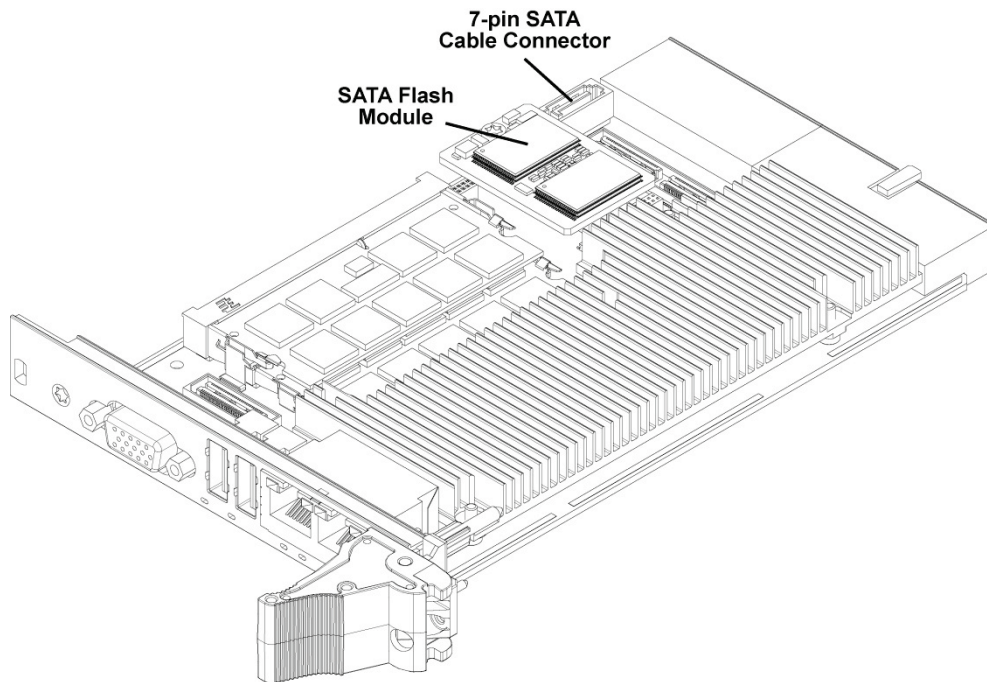


Figure 26: HP CP3005-SA with MMEXT-XMC02 Module

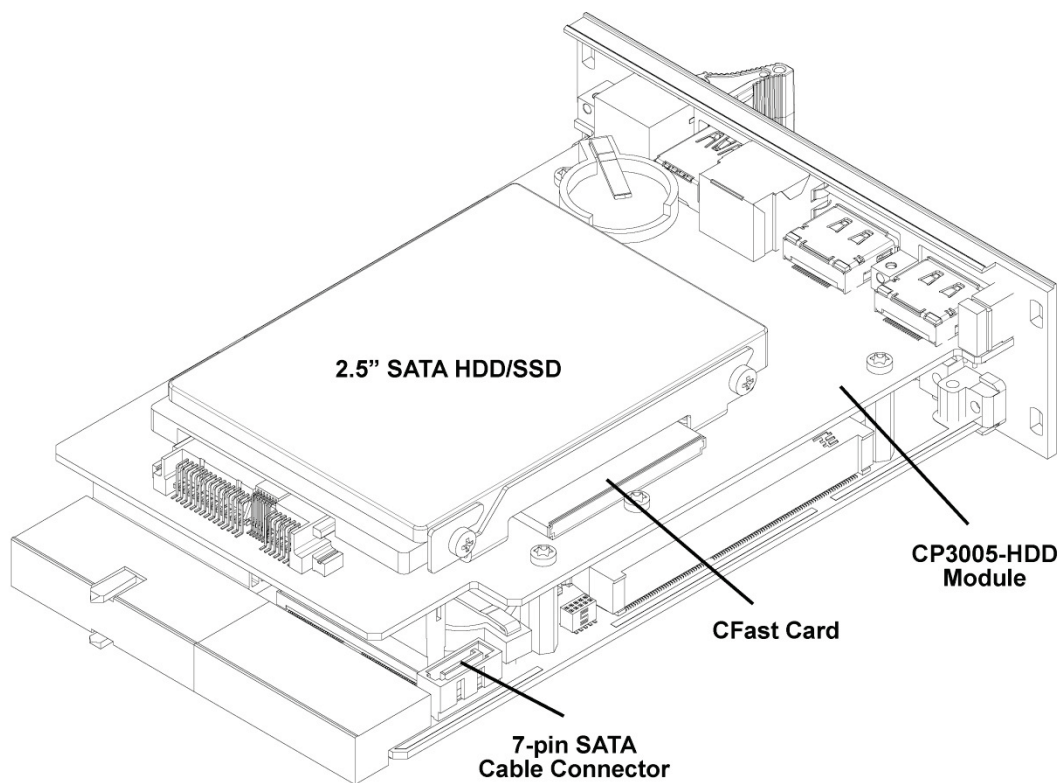
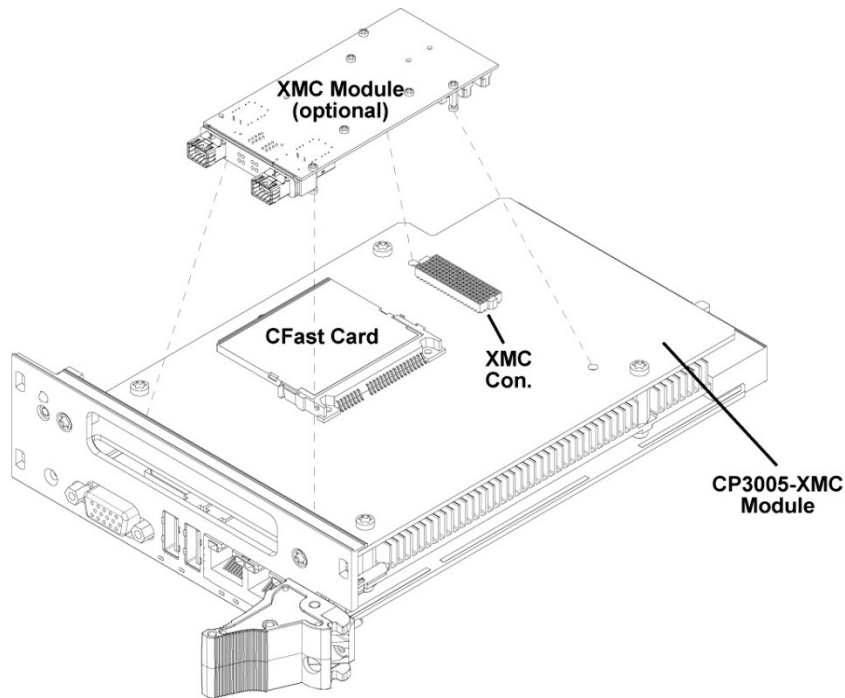


Figure 27: CP3005-SA 8HP with MMEXT-XMC02 Module

12.3.1. Installation of External SATA Devices

The following information pertains to external SATA devices which may be connected to the CP3005-SA via normal cabling.

Some symptoms of incorrectly installed SATA devices are:

- ▶ Device on a SATA channel does not spin up: check power cables and cabling. May also result from a bad power supply or SATA device. The SATA connector on the CP3005-SA provides only a data connection. The power for this device must be supplied by a separate connector. For further information, refer to the respective documentation of the device.
- ▶ SATA device fail message at boot-up: may be a bad cable or lack of power going to the drive.

12.3.2. 2.5" HDD/SSD Installation

One 2.5" SATA HDD/SSD may be connected to the CP3005-SA. The HDD/SSD may be connected to the 8HP CP3005-SA board version equipped with an MMEXT05 extension module via the SATA connector J6 located on the extension module. Please refer to **Figure 26: HP CP3005-SA with MMEXT-XMC02 Module** for the placement of the 2.5" HDD/SSD.

12.3.3. XMC Module Installation

The 8HP CP3005-SA equipped with the MMEXT-XMC02 module provides an XMC connector, J1, for connection to an XMC module such as the Kontron XMC 401, XMC402, etc.

The XMC module must be installed on the MMEXT-XMC02 prior to installation of the CP3005-SA with the MMEXT-XMC02 in a system.

Before installing an XMC module on the CP3005-SA equipped with an MMEXT-XMC02 extension module, ensure that the safety requirements on page 75 are observed.

NOTICE

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

To install an XMC module on the CP3005-SA equipped with an MMEXT-XMC02 extension module, refer to the figures shown below and proceed as follows:

Figure 28: Screws Securing the Front Panel and the MMEXT-XMC02 to the CP3005-SA

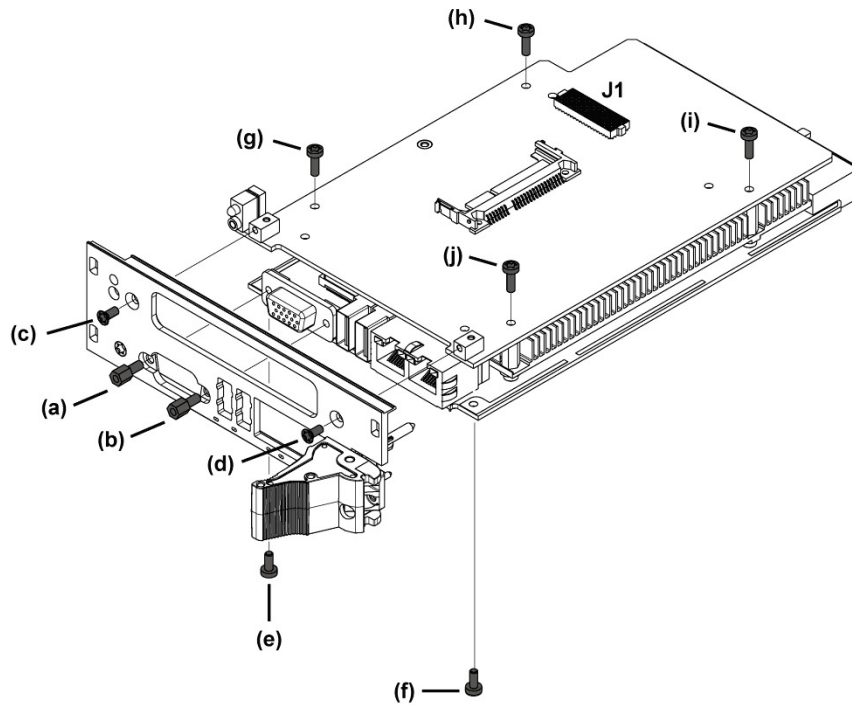


Figure 29: Screws Securing the XMC Module to the MMEXT-XMC02 Extension Module

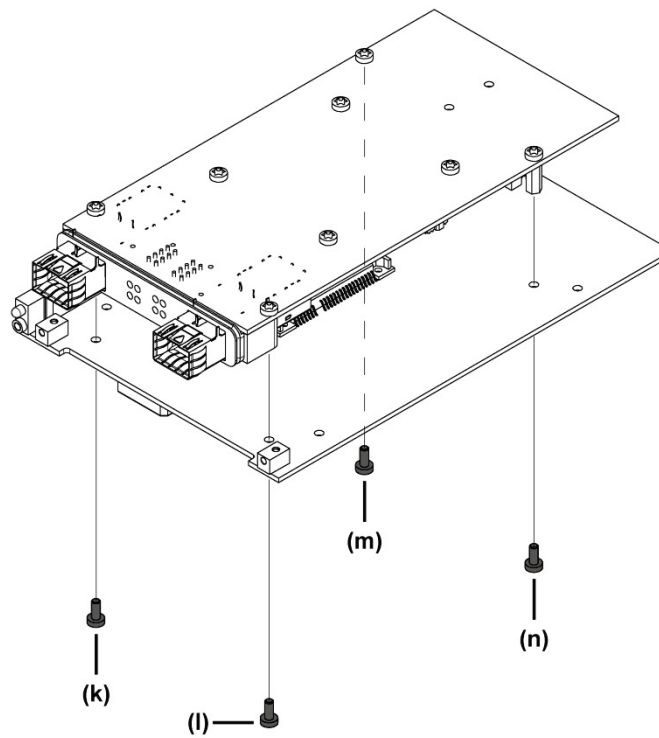


Figure 30: CP3005-SA Board with MMEXT-XMC02 Extension Module and XMC Module

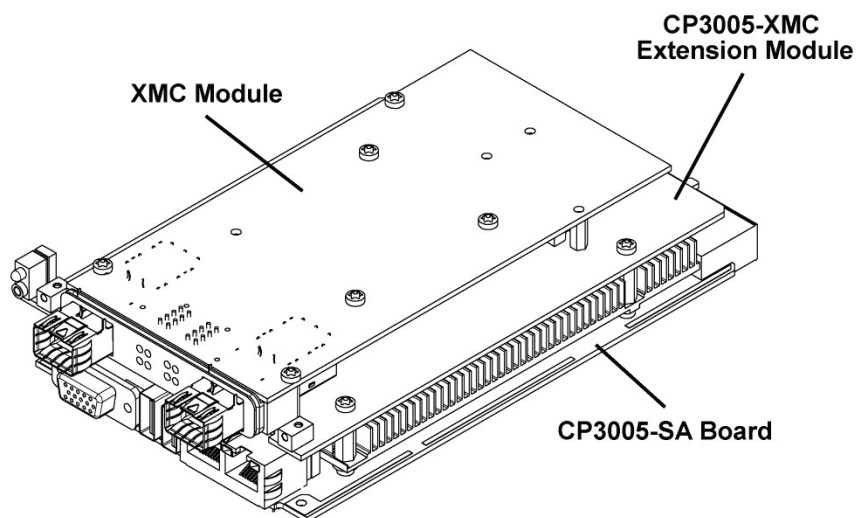
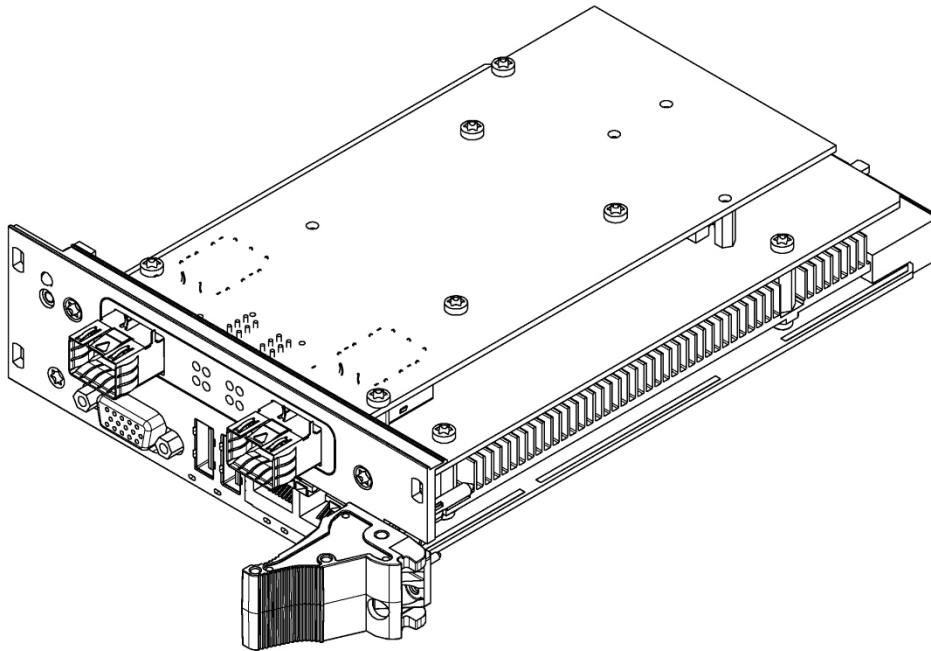


Figure 31: CP3005-SA with Front Panel, MMEXT-XMC02 Extension Module and XMC Module

1. Ensure that no power is applied to the CP3005-SA and disconnect any interfacing cables that may be connected to the board before proceeding.

NOTICE

Even though power may be removed from the system, the CP3005-SA front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source. In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins. It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting). Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

2. Remove the front panel by unscrewing the following screws that are retaining the front panel to the CP3005-SA board. Please refer to **Figure 28: Screws Securing the Front Panel and the MMEXT-XMC02 to the CP3005-SA** for the location of the above-mentioned screws.
 - ▶ (a) and (b) near the VGA connector on the front panel
 - ▶ (c) and (d) near the XMC slot on the front panel
 - ▶ (e) and (f) on the board's solder side near the front panel
3. Remove the MMEXT-XMC02 from the CP3005-SA by unscrewing the (g), (h), (i) and (j) screws shown in **Figure 28: Screws Securing the Front Panel and the MMEXT-XMC02 to the CP3005-SA**

Turn the XMC module component-side down, align its XMC connector with the MMEXT05's XMC connector, J1, and gently press down. Secure the XMC module to the MMEXT-XMC02 by inserting the four screws (k), (l), (m), and (n) supplied with the XMC module through the MMEXT05-CMC02's mounting holes into the XMC module's standoffs and tightening them. Refer to

4. **Figure 29: Screws Securing the XMC Module to the MMEXT-XMC02 Extension Module** for the location of the above-mentioned mounting holes.
5. Align the board-to-board connectors, J5 and J6, on the MMEXT-XMC02 with the board-to-board connectors, J8 and J14, on the CP3005-SA and gently press down. Please refer to **Figure 30: CP3005-SA Board with MMEXT-XMC02 Extension Module and XMC Module** for further information on this instruction.
6. Secure the MMEXT-XMC02 equipped with the XMC module to the CP3005-SA by inserting the screws (g), (h), (i) and (j) removed in step 3 into the respective mounting holes and tightening them.
7. Remove the XMC slot cover plate from the XMC bezel cutout of the CP3005-SA front panel, if mounted.
8. Attach the front panel to the board assembly and secure it with the screws (a), (b), (c), (d), (e), and (f) removed in step 2. If the XMC module is provided with a rubber seal at the bezel, ensure that the rubber seal is properly seated between the bezel and the front panel cutout when attaching the front panel. Please refer to **Figure 31: CP3005-SA with Front Panel, MMEXT-XMC02 Extension Module and XMC Module** for further information on this instruction

The 8HP CP3005-SA equipped with the MMEXT-XMC02 extension module and an XMC module is now ready for operation. For the operation of the XMC module, refer to appropriate documentation provided with the XMC module.

12.3.4. SATA M.2 Card Installation

A SATA Flash module may be connected to the CP3005-SA via the onboard connector, J12. This optionally available module must be physically installed on the CP3005-SA prior to installation of the CP3005-SA in a system. During installation it is necessary to ensure that the SATA Flash module is properly seated.

The following failures may occur:

- ▶ SATA device fail message at boot-up: may be a bad cable or lack of power going to the drive
- ▶ SATA device fail message at boot-up on Rear I/O module, caused by forced speed to 6.0 Gb/s (see Chapter 9.5.6 "SATA Interfaces")

The CP3005-SA provides a M.2 card socket on the board to install SSD cards.

NOTICE

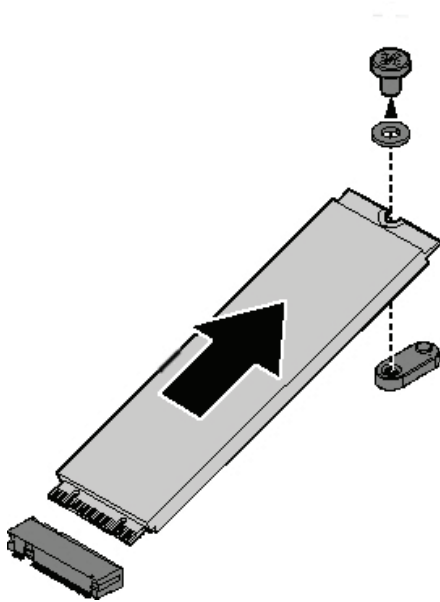
The CP3005-SA does not support removal and reinsertion of the M.2 storage card while the board is in a powered-up state. Connecting the M.2 card while the power is on, which is known as "hot plugging", may damage your system.

12.3.4.1. Removing a M.2 Card

To remove a M.2 card:

1. Power off the board, and then detach the power cord from the power supply.
2. Remove the CP card.
3. Remove the screw and washer securing the M.2 card and M.2 holder.
4. The M.2 card pops up. Grasp it by the edges and slide it out.

Figure 32: Removing a M.2 Card

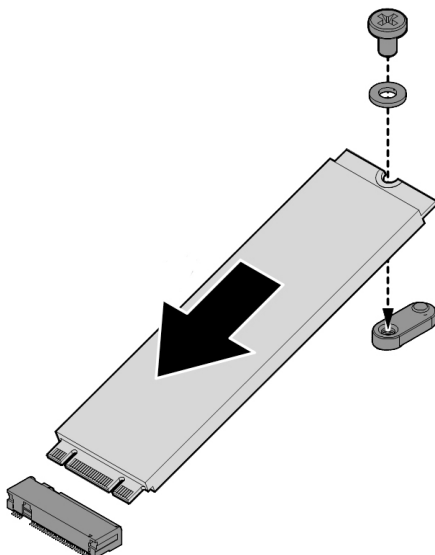


12.3.4.2. Installing a M.2 Card

To install a M.2 card:

1. Align the connector on the M.2 with the connector on the board. Make sure the slits are aligned with the protrusions on the connector.
2. Insert the M.2 card into the connector on the server board.
3. Install the washer.
4. Secure the M.2 card holder with the screw.

Figure 33: Installing a M.2 Card



12.3.5. Rear I/O Device Installation

The CP-RIO3-04 4HP/8HP and CP-RIO3-04S rear transition modules does not support hot swapping. Therefore, the system must have power removed to install or remove the CP-RIO3-04 4HP/8HP and CP-RIO3-04S rear transition modules. Before extracting the CP-RIO3-04 4HP/8HP and CP-RIO3-04S rear transition modules, ensure that all connected cables are disconnected. For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

NOTICE

VGA and Ethernet can be used either on the front panel or on the rear I/O. The COM interface can be used either on the MMEXT05 extension module or on the rear I/O. It is not possible to use any of the above-mentioned interfaces on the front or the MMEXT05 extension and on the rear I/O simultaneously. On the MMEXT05 there is a third Ethernet port, which is working all time.

12.4. Battery Replacement

The CP3005-SA RTC may be backed up using a single 3.0 V coin cell lithium battery from one of two possible points of installation:

- ▶ via MMBTA02 module on the CP3005, connected with a cable
- ▶ on the MMEXT05 extension module

Only one battery may be installed at a time. Refer to Table 1: CP3005-SA Main Specifications for battery requirements. The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

NOTICE

The battery is mounted on a battery module (MMBAT02) on the CP3005-SA board or on the MMEXT05 extension module – but never on both devices.

13/ uEFI BIOS

13.1. Starting the uEFI BIOS

The CP3005-SA is provided with a Kontron-customized, pre-installed and configured version of Aptio®V (referred to as uEFI BIOS in this manual), AMI's BIOS firmware based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the CP3005-SA.

The uEFI BIOS comes with a Setup program which provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows the accessing of various menus which provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A Setup menu will appear.

The CP3005-SA uEFI BIOS Setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the Setup screens. The following table provides information concerning the usage of these hot keys.

Table 47: Navigation

Hot Key	Description
→←	The Left and Right <Arrow> keys are used to select a major Setup screen. For example: Main Screen, Advanced Screen, Chipset Screen, etc.
↑↓	The Up and Down <Arrow> keys are used to select a Setup function or a sub-screen.
+ / -	The Plus and Minus <Arrow> keys are used to change the field value of a particular Setup function, for example, system date and time.
<F1>	The <F1> key is used to invoke the General Help window.
<F2>	The <F2> key is used to restore the previous values.
<F3>	The <F3> key is used to load the defaults for the Setup and the kboardconfig uEFI Shell command.
<F4>	The <F4> key is used to save the current settings and exit the uEFI BIOS Setup.
<K>	The <K> key is used to scroll the help area upwards.
<M>	The <M> key is used to scroll the help area downwards.
<ESC>	The <ESC> key is used to exit a menu or the uEFI BIOS Setup. Pressing the <ESC> key in a sub-menu causes the next higher menu level to be displayed. When the <ESC> key is pressed in a major Setup menu, a pop-up window will appear asking the user if he wants to exit the uEFI BIOS Setup menu without saving.
<Enter>	The <Enter> key is used to execute a command or select a menu.

13.2. Setup Menus

The Setup utility features four menus listed in the selection bar at the top of the screen:

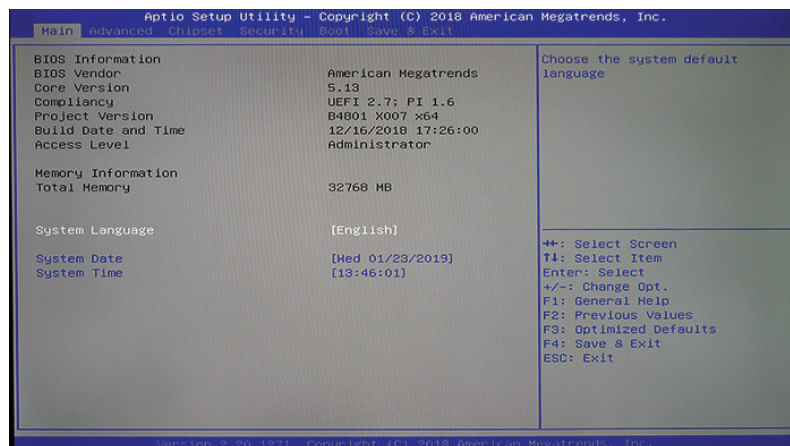
- ▶ Main
- ▶ Advanced
- ▶ Chipset
- ▶ Security
- ▶ Boot
- ▶ Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white.

Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item-Specific Help window providing an explanation of the respective function.

13.2.1. Main Setup Menu

Figure 34: Main Setup



NOTICE

In the manual is the disabled expert mode described.

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information as well as functions for setting the system time and date.

Table 48: Main Setup Menu Sub-Screens and Functions

Sub-Screen	Function	Description
BIOS Information	Project Version, Build Date and Time, etc.	Read-only field, displays information about the system BIOS. Information about the running uEFI BIOS is reflected in the display-only function "Project Version" (parameter "10.00" indicates Rev. 10).
Memory Information	Total Memory	Read-only field, displays information about the processor and the memory.
System Language	[English]	Selects the system language. Currently, only English is

Sub-Screen	Function	Description
		supported
System Date	<WD MM/DD/YYYY>	Changes the system date, select the system date using the Up and Down <Arrow> keys. Enter the new values through the keyboard or press +/- to increment/decrement values. Use "Tab" to switch between date elements. The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.
System Time	<HH:MM:SS>	Changes the system time, select the system time using the Up and Down <Arrow> keys. Enter the new values through the keyboard or press +/- to increment/decrement values. Use "Tab" to switch between time elements.

13.2.2. Advanced Setup Menu

The Advanced Setup menu provides sub-screens and functions for advanced configuration.

NOTICE

Setting items on this screen to incorrect values may cause the system to malfunction.

Figure 35: Advanced Setup

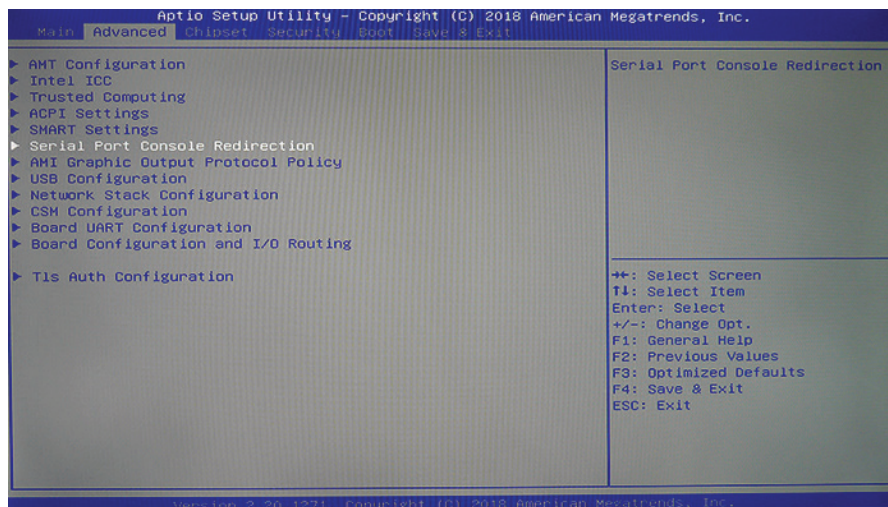


Table 49: Advanced Setup Menu Sub-Screens and Functions

Sub-Screen	Function	Description
AMT Configuration	ASF Support	Enabled/ Disabled
	USB Provisioning of AMT	Enabled/ Disabled
	CIRA Configuration	Activate Remote Assistance Process [Enabled/ Disabled] CIRA Timeout [0]
	ASF Configuration	
	Secure Erase Configuration	
	OEM Flags Settings	MEBx hotkey pressed [Enabled/ Disabled] MEBx Selection Screen [Enabled/ Disabled]

Sub-Screen	Function	Description
		Hide Unconfigure ME Confirmation Prompt [Enabled/ Disabled] MEBx OEM Debug Menu Enable [Enabled/ Disabled] Unconfigure ME [Enabled/ Disabled]
	MEBx Resolution Settings	Non-UI Mode Resolution [Auto] UI Mode Resolution [Auto] Graphice Mode Resolution [Auto]
Intel ICC	ICC/OC Watchdog Timer	[Enabled/ Disabled]
Trusted Computing	Security Device Support	[Enabled /Disabled]
	SHA-1 PCR Bank	[Enabled /Disabled]
	SHA-256 PCR Bank	[Enabled /Disabled]
	Pending Operation	[None]
	Platform Hierarchy	[Enabled /Disabled]
	Storage Hierarchy	[Enabled /Disabled]
	Endorsement Hierarchy	[Enabled /Disabled]
	TPM2.0 UEFI Spec Version	[TCG_2]
	Physical Presence Spec Version	[1.3]
	TPM 20 Interface Type	[CRB]
	Device Select	[Auto]
ACPI Settings	Enable SCPI Auto Configuration	[Enabled/ Disabled]
	Enable Hibernation	[Enabled /Disabled]
	ACPI Sleep State	[S3 Suspend to RAM]
	Lock Legacy Resources	[Enabled/ Disabled]
	S3 Video Repost	[Enabled/ Disabled]
Smart Settings	Smart Self Test	[Enabled/ Disabled]
Serial Port Console Redirection	COM0 Console Redirection	[Enabled/ Disabled]
	COM1 Console Redirection	[Enabled/ Disabled]
	Legacy Console Redirection Settings	Redirection COM Port [COM0] Resolution [80x24] Redirection after Post [Always Enable]
	Console Redirection	[Enabled/ Disabled]
AMI Graphic Output	Output Select	[EDP1]

Sub-Screen	Function	Description
Protocol Policy	Brightness Setting	255
	BIST Enable	[Enabled/Disabled]
USB Configuration	Legacy USB Support	[Enabled/Disabled]
	XHCI Hand-off	[Enabled/Disabled]
	USB Mass Storage Driver Support	[Enabled/Disabled]
	USB transfer timeout	[20 sec]
	Device reset time-out	[20 sec]
	Device powerup delay	[Auto]
Network Stack Configuration	Network Stack	[Enabled/Disabled]
CSM Configuration	CSM Support	[Enabled/Disabled]
	Gate A20 Active	[Upon Request]
	INT19 Trap Response	[Immediate]
	Boot option filter	[UEFI only]
	Network	[Do not launch]
	Storage	[UEFI]
	Video	[UEFI]
	Other PCI devices	[UEFI]
Board UART Configuration	Serial Port 1 Configuration	Serial Port [Enabled/Disabled] Change Settings [Auto]
	Serial Port 2 Configuration	Serial Port [Enabled/Disabled] Change Settings [Auto]
Board Configuration and I/O Routing	Expert Mode	[Enabled/Disabled]
	Enable automatic update	[Enabled/Disabled]
	Shell Timeout config	[5 sec]
	Com A	[Extension]
	Com B	[RS232]
	VGA Port Configuration	[Front]
	Eth A	[Front]
	Eth B	[Front]
	USB I/O	[Enabled/Disabled]
	USB Front	[Enabled/Disabled]
	USB Rear	[Enabled/Disabled]
Tls Auth Configuration	Server CA Configuration	Enroll Cert [Enroll Cert Using File/Commit Changes and Exit/Discard Changes and Exit] Delete Cert
	Client Cert Configuration	Enroll Cert [Enroll Cert Using File/Commit Changes and Exit/Discard Changes and Exit] Delete Cert

13.2.3. Chipset Menu

Figure 36: Chipset Menu

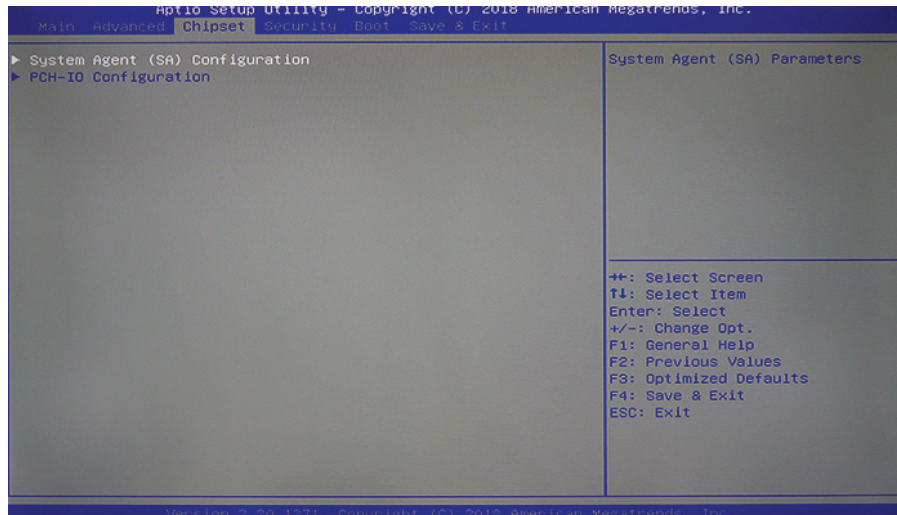


Table 50: Chipset Menu Functions

Sub-Screen	Function	Description
System Agent (SA) Configuration	Memory Configuration	Maximum Memory Frequency [Auto]
	Graphics Configuration	SkipScanning of External Gfx Card [Enabled/ Disabled] Primary Display [Auto] Select PCIE Card [Auto] External Gfx Card Primary Display Configuration Internal Graphics [Auto] GTT Size [8 MB] Aperture Size [256 MB] PSMI Support [Enabled/ Disabled] DVM T Pre-Allocated [32M] DVM T Total Gfx Mem [256M] Intel Graphics Pei Display Peim [Enabled/ Disabled] VDD Enable [Enabled /Disabled] PM Support [Enabled /Disabled] PAVP Enable [Enabled /Disabled] Cdyynmax Clamping Enable [Enabled /Disabled] Cd Clock Frequency [675 MHz] Skip CD Clock Init in S3 resume [Enabled/ Disabled] IUER Button Enable [Enabled/ Disabled] Intel Ultrabook Support [IUERSlate Enable[Enabled/ Disabled] /IUER Dock Enable[Enabled/ Disabled]]
	PEG Port 0:1:0 Configuration	Enable Root Port [Auto] Max Link Speed [Auto]

Sub-Screen	Function	Description
		PEG0 Slot Power Limit Value 75 PEG0 Slot Power Limit Scale [1.0x] PEG0 Physical Slot Number 1
	PEG Port 0:1:1	Enable Root Port [Auto] Max Link Speed [Auto] PEG1 Slot Power Limit Value 75 PEG1 Slot Power Limit Scale [1.0x] PEG1 Physical Slot Number 2
	PEG Port 0:1:2	Enable Root Port [Auto] Max Link Speed [Auto] PEG2 Slot Power Limit Value 75 PEG2 Slot Power Limit Scale [1.0x] PEG2 Physical Slot Number 3
	PEG Port 0:6:0	Enable Root Port [Auto] Max Link Speed [Auto] PEG3 Slot Power Limit Value 75 PEG3 Slot Power Limit Scale [1.0x] PEG3 Physical Slot Number 4
	PEG Port Feature Configuration	Detect Non-Compliance Device [Enabled/Disabled]
	Program PCIe ASPM after OpROM	[Enabled/Disabled]
	Program Static Phase1 Eq	[Enabled/Disabled]
	Gen3 Root Port Preset value for each lane	[Lane 0 ... Lane 15: 7]
	Gen3 Endpoint Preset value for each lane	[Lane 0 ... Lane 15: 7]
	Gen3 Endpoint Hint value for each lane	[Lane 0 ... Lane 15: 2]
	Gen3 RxCTLE Control	Bundle0 ... Bundle7: 0, PEG11 ... PEG13 [Enabled/Disabled], DMI [Enabled/Disabled] [Enabled/Disabled]
	Always Attempt SW EQ	[Auto]
	Number of Presets to test	[Auto]
	Allow PERST# GPIO Usage	[Enabled/Disabled]
	SW EQEnable VOC	[Auto]
	Jitter Dwell Time	3000
	Jitter Error Target	2
	VOC Dwell Time	10000
	VOC Error Target	2
	Generate BDAT PEG Margin	[Enabled/Disabled]

Sub-Screen	Function	Description
	Data PCIe Rx CEM Test Mode	[Enabled/ Disabled]
PCH-IO Configuration	PCI Express Configuration	
	SATA and RST Configuration	
	USB Configuration	
	Security Configuration	
	HD Audio Configuration	
	PCH LAN Controller	[Enabled/ Disabled]
	LAN Wake From DeepSx	[Enabled/ Disabled]
	Wake on LAN Enable	[Enabled/ Disabled]
	SLP_LAN# Low on DC Power	[Enabled/ Disabled]
	State after G3	[S0 State]

13.2.4. Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The CP3005-SA provides no factory-set passwords.

Figure 37: Security Setup

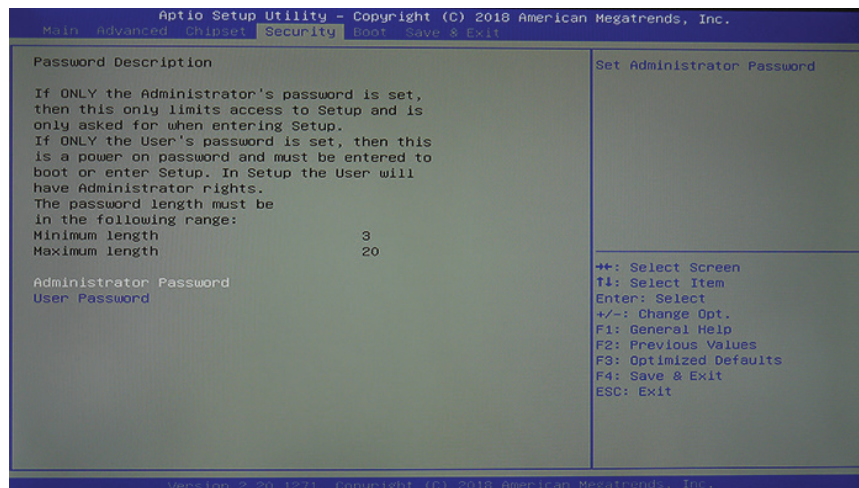


Table 51: Security Setup Menu Functions

Function	Description
Password Description	Read-only field.
Administrator Password	Sets, changes or clears the Administrator Password. To set a password, enter it twice and acknowledge by pressing Return.
User Password	Sets, changes or clears the User Password. To set a password,

Function	Description
	enter it twice and acknowledge by pressing Return.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Table 52: Modes of Security

Setting	Description
No password is set	Booting the system as well as entering the Setup is unsecured.
Only Administrator password is set	Booting the system is unsecured. For entering the Setup, the Administrator password is required.
Only User password is set	The password is required for booting the system as well as for entering the Setup menu. On every startup, the user will be asked for the password.
Both User and Administrator passwords are set	Either the User or the Administrator password is required for booting the system as well as for entering the Setup menu. If the User password is entered here, limited access to the Setup is granted. Entering the Administrator password provides full access to all Setup entries.

13.2.5. Remember the Password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords may lead to being completely locked out of the system.

If the system cannot be booted because neither the User Password nor the Administrator Password are known, refer to the section 3.1, for information about clearing the uEFI BIOS settings, or contact Kontron for further assistance.

NOTICE

The HDD User Password cannot be cleared using the above method.

13.2.6. Boot Setup Menu

The Boot Setup menu provides sub-screens and functions for boot configuration and shows the boot device priority order, which is dynamically generated.

Figure 38: Boot Setup

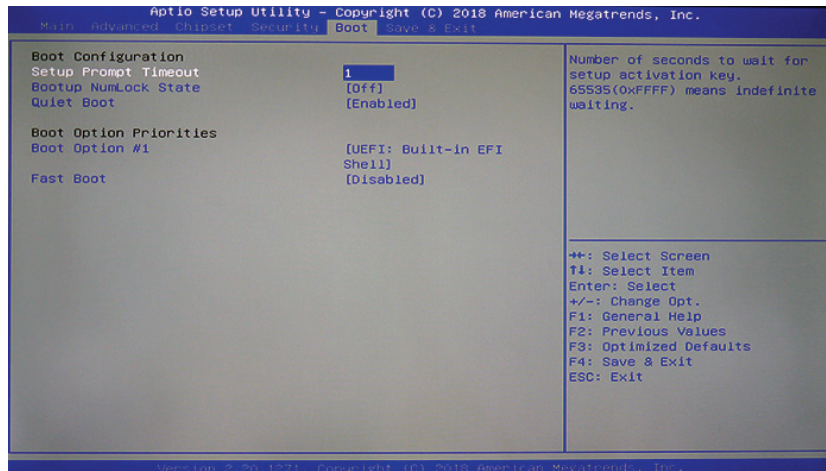


Table 53: Boot Setup Menu Sub-Screens and Functions

Sub-Screen	Function	Description
Boot Configuration	Setup Prompt Timeout	1
	Bootup NumLockState	[Off]
	Quiet Boot	[Enabled/Disabled]
Boot Option Priorities	Boot option #1..2	[UEFI: Built in EFI Shell]
	Fast Boot	[Enabled/Disabled]

13.2.7. Save & Exit Setup Menu

The Save & Exit Setup menu provides functions for handling changes made to the uEFI BIOS settings and the exiting of the Setup program.

NOTICE

The Setup will ask for confirmation prior to executing the commands.

Figure 39: Save & Exit Setup

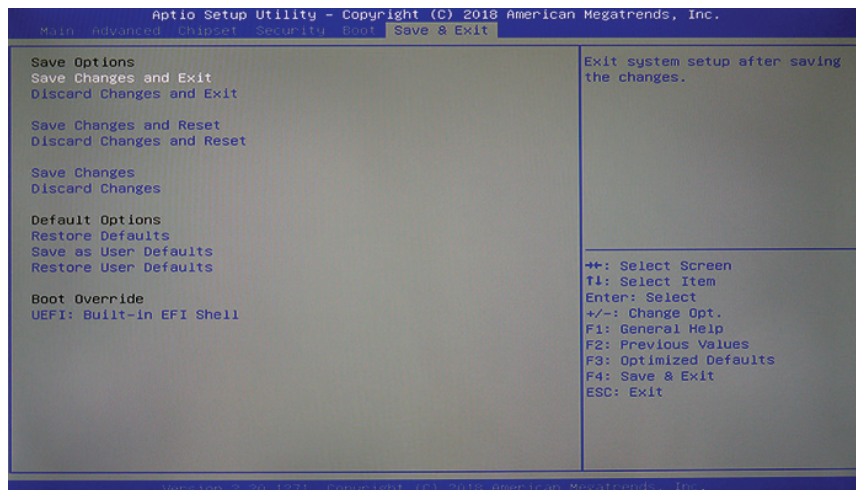


Table 54: Save & Exit Setup Menu Sub-Screens and Functions

Sub-Screen	Function	Description
Save & Exit	Save Changes and Exit	Equal to F4. Saves all changes made within the Setup to flash, then exits the uEFI BIOS Setup, and finally resets the system automatically. This function continues the boot process as long as no option was altered that requires a reboot.
	Discard Changes and Exit	Discards all changes made within the Setup, then exits the uEFI BIOS Setup. This function continues the boot process.
	Save Changes and Reset	Saves all changes made within the Setup to flash and resets the system.
	Discard Changes and Reset	Discards all changes made within the Setup and resets the system.
Save Options	Save Changes	Saves all changes made within the Setup to flash but does not reset system. This function returns to Setup.
	Discard Changes	Discards all changes made within the Setup but does not reset system. This function returns to Setup.
	Restore Defaults	Equal to F3. Restores/Loads the factory default values for all setup options.
	Save as User Defaults	Saves all current settings as user default. The current setup state can later be restored using Restore User Defaults.
	Restore User Defaults	Restores all tokens to settings previously stored by Save as User Defaults.

Sub-Screen	Function	Description
Boot Override	UEFI: Built-in EFI Shell	This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order. If booting to EFI Shell this way, an exit from the shell returns to Setup.

13.3. The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting refer to the EFI Shell User's Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (<http://sourceforge.net/projects/efi-shell/files/documents/>).

Please note that not all shell commands described in the EFI Shell Command Manual are provided by the Kontron uEFI BIOS.

13.3.1. Introduction, Basic Operation

The uEFI Shell forms an entry into the uEFI boot order and is the first boot option by default.

13.3.1.1. Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Press the ESC key within 5 seconds after a message such as the one below appears:

```

UEFI Interactive Shell v2.0
EDK II
UEFI v2.40 (American Megatrends, 0x0005000A)
Mapping table
  blk0      :Removable HardDisk - Alias hd33b0b0b fs0
              Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
...
Press the ESC key within 5 seconds to skip startup.nsh, and any other key to continue.
The output produced by the device mapping table can vary depending on the board's
configuration.
If the ESC key is pressed before the 5-second timeout has elapsed, the shell prompt is
shown:
Shell>
```

13.3.1.2. Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Invoke the exit uEFI Shell command to select the boot device in the boot menu for the OS to boot from.
2. Reset the board using the reset uEFI Shell command.

13.3.1.3. Kontron-Specific uEFI Shell Commands

The Kontron uEFI implementation provides the following additional commands related to the specific HW features of the Kontron system.

Table 55: Kontron-Specific uEFI Shell Commands

Command	Description
kboardconfig	Configures non-volatile board settings, such as: ▶ AutoUpdate: Note: If AutoUpdate is enabled, an automatic update procedure from the connected mass storage device is initiated after a reset. The update status is indicated in the log file located in the directory where the firmware images are stored. ▶ C3State ▶ C6State ▶ C7State ▶ ComA ▶ cPCISlotClockOut0..7 ▶ CpuTurbo ▶ cTDP ▶ GbeA ▶ GbeB ▶ IntelHT ▶ IntelVT ▶ PrimaryDisplay ▶ Pxe ▶ Sata2Hotplug ▶ Sata3Hotplug ▶ SataMode ▶ SataSpeed ▶ ShellTimeOut ▶ SpeedStep ▶ Vga ▶ WrProtSata ▶ WrProtSystem Note: The parameters of the kboardconfig command are not case-sensitive.
kboardinfo	Shows a summary of board-specific data and displays/checks various parameters such as the current uEFI BIOS revision, etc.
kboot	Boots a legacy OS Not to be used for uEFI BootLoaders! If the requested device is not present, boot returns to shell. This command cannot boot native uEFI-aware operating systems. But since these are bootable from shell by calling their bootloader, this is not necessary either. If a requested device is present but not bootable, uEFI continues to boot with the next bootable device in the boot order.
kbootscript	Manages the flash-stored startup script If the shell is launched by the boot process, it executes a shell script stored in the flash. If the shell script terminates, the shell will continue the boot process. However, the shell script can also contain any other boot command.
kflash	Programs and verifies the SPI boot flashes holding the uEFI BIOS code, uEFI BIOS binary files must be available from connected mass storage devices, such as USB

Command	Description
	flash drive or harddisk.
kjtag	Programs an onboard device via the JTAG interface
knvram	Manages the NVRAM to restore the system's default settings, Since all uEFI settings are stored inside the NVRAM, the default settings are loaded after invoking this command.
kpassword	Controls uEFI Setup and Shell passwords, This command is used to determine the status of both passwords (set or not set) and to set or clear the uEFI Shell and Setup passwords. Both user and superuser (Supervisor) passwords can be controlled with this command. Call without options to get current password status. Entering an empty password clears the password.
kramdisk	Creates and manages RAMdisks, This command is used to perform file operations when no real filesystem is connected to the system.
kreset	Controls the board's reset behavior, This command controls if the board shall react on a CompactPCI backplane reset if it is used in a peripheral slot. It has no effect if the board is installed in the CompactPCI system slot. The parameter of this command is volatile and set to off at the next start.
kupdate	Controls the Kontron common update tool, When using the kupdate command, the structure of the ZIP archive must not be altered. kupdate automatically starts the update procedure via kupdate -u. If a certain image is intended to be used, enter kupdate -s to select the respective image.
kwatchdog	Configures the Kontron onboard Watchdog, This command is used to enable the Kontron onboard Watchdog with reset target before OS boot. This can be used to detect if the OS fails to boot and react by reset.

NOTICE

The uEFI Shell commands are not case-sensitive. Each uEFI Shell command is provided with a detailed online help that can be invoked by entering "<cmd> <space> <-?>" in the command line. To display the uEFI Shell command list, enter <help> or <?> in the command line.

13.4. uEFI Shell Scripting

13.4.1. Startup Scripting

If the ESC key is not pressed and the timeout is run out, the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Kontron flash-stored startup script
2. If there is no Kontron flash-stored startup script present, the uEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts is present or the startup script terminates, the default boot order is continued.

13.4.2. Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor edit or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system. To copy the startup script to the flash use the **kbootscript** uEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the **kramdisk** uEFI Shell command.

13.4.3. Examples of Startup Scripts

13.4.3.1. Automatic Booting from USB Flash Drive

Automatic booting is made from a USB flash drive, if present, otherwise the boot is made from the harddrive.

```
kboot -t usb-harddrive
kboot -t harddrive
```

If neither a USB flash drive nor a harddrive is present, the boot order is continued.

13.4.3.2. Execute Shell Script on Other Harddrive

This example (**startup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disc drive (**fs0**).

```
fs0:
bootme.nsh
```

13.4.3.3. Enable Watchdog and Control PXE Boot

The uEFI Shell provides environment variables used to control the execution flow.

The following sample start-up script shows two uEFI Shell environment variables, **wdt_enable** and **pxe_first**, used to control the boot process and the Watchdog.

```
echo -off
echo "Executing sample startup.nsh..."
if %wdt_enable% == "on" then
    kwdt -t 15
    echo "Watchdog enabled"
endif
if %pxe_first% == "on" then
    echo "forced booting from network"
    kboot -t network
endif
```

To create uEFI Shell environment variables, use the **set** uEFI Shell command as shown below:

```
Shell> set wdt_enable on
Shell> set pxe_first on
Shell> set
    pxe_first : on
    wdt_enable : on
Shell> reset
```

13.4.3.4. Handling the Startup Script in the SPI Boot Flash

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the following instructions:

1. Press <ESC> during power-up to log into the uEFI Shell.
2. Create a RAM disk and set the proper working directory as shown below:


```
Shell> kramdisk -s 3 myramdisk
Shell> myramdisk:
```
3. Enter the sample start-up script mentioned above in this section using the **edit** uEFI Shell command.


```
myramdisk:\> edit boot.nsh
```
4. Save the start-up script to the SPI boot flash using the **kbootscript** uEFI Shell command.


```
myramdisk:\> kbootscript -p boot.nsh
```

5. Reset the board to execute the newly installed script using the reset uEFI Shell command.

```
myramdisk:\> reset
```
6. If a script is already installed, it can be edited using the following kbootscript uEFI Shell commands.

```
myramdisk:\> kbootscript -g boot.nsh
myramdisk:\> edit boot.nsh
```

13.5. Updating the uEFI BIOS

The CP3005-SA has two SPI boot flashes programmed with the uEFI BIOS, a standard SPI boot flash and a recovery SPI boot flash. The basic idea behind that is to always have at least one working uEFI BIOS flash available regardless if there have been any flashing errors or not.

13.5.1. Updating Procedure

The standard SPI boot flash can be updated with the latest uEFI BIOS from the ZIP archive using the kupdate -u or the kflash -p uEFI Shell command. When using the kupdate command, the directory structure of ZIP archive must not be altered. The update status is indicated in the log file located in the directory where the firmware images are stored.

13.5.2. uEFI BIOS Recovery

In case of the standard SPI boot flash being corrupted and therefore the board not starting up, the board can be booted from the recovery SPI boot flash if the DIP switch SW1, switch 2 is set to ON. For further information, refer to the section 3.1 DIP Switch Configuration.

NOTICE

The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

NOTICE

To make the standard SPI boot flash bootable again, invoke the kflash -c uEFI Shell Command. Hence, the content of the recovery SPI boot flash is copied to the standard SPI boot flash.

13.5.3. Determining the Active Flash

Sometimes it may be necessary to check which flash is active. On the AMI Aptio-based uEFI BIOS, the information is available using the kboardinfo uEFI Shell command.

Appendix A: List of Acronyms

List of Acronyms

API	Application Programming Interface
BMC	Base Management Controller
CLI	Command-Line Interface
COM	Computer-on-Module
ECC	Error Checking and Correction
FRU	Field Replaceable Unit
GPU	Graphics Processing Unit
HD/HDD	Hard Disk /Drive
HPM	PICMG Hardware Platform Management specification family
IOL	IPMI-Over-LAN
IOT	Internet of Things
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
KVM	Keyboard Video Mouse
MEI	Management Engine Interface
NCSI	Network Communications Services Interface
PCIe	PCI-Express
PECI	Platform Environment Control Interface
PICMG®	PCI Industrial Computer Manufacturers Group
RTC	Real Time Clock
SEL	System Event Log
ShMC	Shelf Management Controller
SMBus	System Management Bus
SMWI	System Monitor Web Interface
SOL	Serial Over LAN
SSH	Secure Shell
TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface
VLP	Very Low Profile



About Kontron

Kontron is a global leader in embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall. For more information, please visit: <http://www.kontron.com/>



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