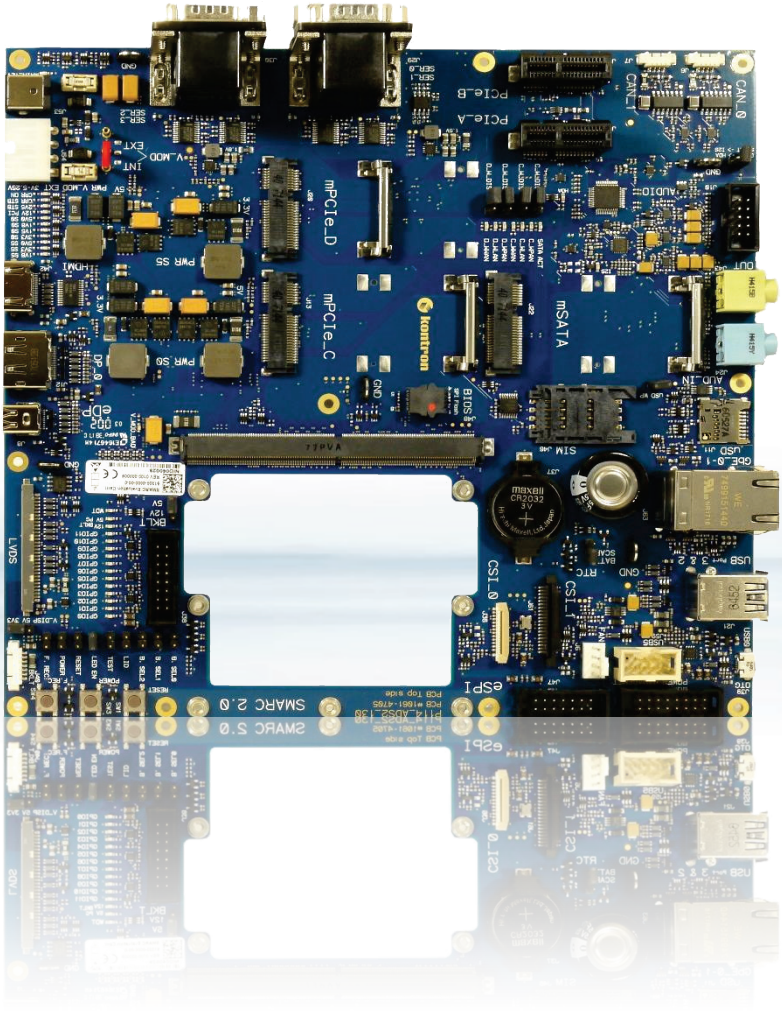
USER GUIDE



SMARC Eval-Carrier-2

Doc-ID: 1061-6432

Doc. Rev. 1.5

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SMARC EVAL-CARRIER-2 - USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	Basic draft	2017-November-30	hjs
1.1	added BIOS chapter	2017-December-20	hjs
1.2	typo Pin23 modified	2018-January-11	hjs
1.3	CSI corrected	2018-March-29	hjs
1.4	Tables 15 to 18 modified	2018-July-24	hjs
1.5	Chapter 8.29: caution note added, boot options for SEL#2, supported SPI on carrier board	2018-October-08	hjs

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Symbols

The following symbols may be used in this manual

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. Please refer also to the "High-Voltage Safety Instructions" portion below in this section.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	This symbol indicates general information about the product and the user manual. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this User Guide or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version, that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present User Guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Table of Contents

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List of Figures

1/ Introduction

This manual describes the Smart Mobility ARChitecture SMARC Eval-Carrier-2 board. This document describes the electronic, mechanical and thermal design of the SMARC evaluation carrierboard. It is designed for the testing of SMARC-sXAL (2), SMARC_SMX7 and other SMARC 2.0 modules. The board will be equipped with DP++ connector, HDMI connector, LVDS connector, two full-size or half-size mPCIe card slot (PCIe + USB 2.0), two PCIe x1 slot and full-size mSATA slot to easily use and test additional cards.

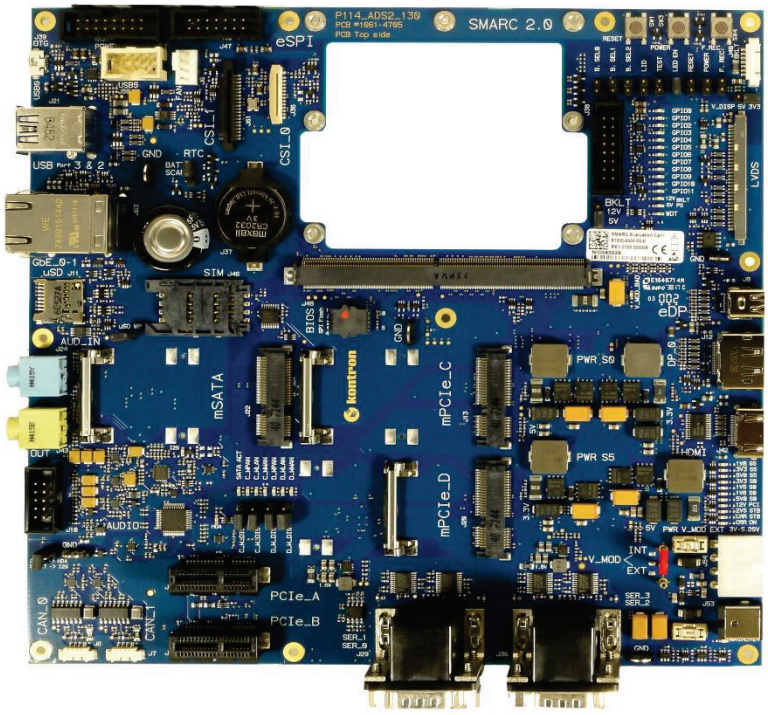
The use of this Users Guide implies a basic knowledge of PC hard- and software. This manual is focussed on describing the special features and is not intended to be a standard PC textbook. New users are recommended to study the short installation procedure stated in the following chapter before switching on the power. All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus. Latest revision of this manual, datasheet, BIOS, drivers and BSP's (Board Support Packages) can be downloaded from Kontron Web Page.

2/ Description

The SMARC Eval-Carrier-2 is designed on the latest SMARC 2.0 specification. The board will be equipped with

- DP++ connector,
- HDMI connector,
- LVDS connector,
- two full-size or half-size mPCIe card slot (PCIe + USB 2.0),
- two PCIe x1 slot,
- full-size mSATA slot,
- two USB 3.0 connectors one USB 2.0 OTG connector,
- SIM card slot,
- Battery holder and super cap
- Camera interface,
- CAN interface,
- two Ethernet connectors,
- HDA and I2S audio codec,
- one USB 2.0 on header,
- µSD connector,
- 4x COM ports.

Figure 1: Carrier board with SMARC interface



3/ Installation procedure

3.1. Packing Check List

The package includes the following basic items accompany with this manual.

- One board

If this item is damaged or missed, please contact your vendor and save all packing materials for future replacement and maintenance.

Note: The above packing list is for standard single box packing only.

3.2. Requirements IEC60950-1

Take care when designing chassis interface connectors in order to fulfil the IEC60950-1 standard.

Users of board must evaluate the end product to ensure compliance the requirements of the IEC60950-1 safety standard are met:

The motherboard must be installed in a suitable mechanical, electrical and fire enclosure.

The system in its enclosure must be evaluated for temperature and air flow considerations.

For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from or to the product shall be with Safety Extra Low Voltage (SELV) circuits only.

Wires have suitable rating to withstand the maximum available power.

The enclosure of the peripheral device fulfills the fire protecting requirements of IEC60950-1.

4/ System specifications

4.1. Component Main Data

The table below summarizes the features of the motherboard.

Table 1: Component Main Data

SMARC Eval-Carrier-2	
Form factor	Testing Hardware with 210 mm x 200 mm, max. thickness 3 mm
Memory	
EEPROM System (U78)	The EEPROM type 24LC64 on carrier board connected to SMARC I2C_PM bus.
SPI flash socket (J48)	SPI flash socket (SOIC8 – 1045-8636) with flash memory W25Q128FWSIQ
EEPROM DDC optional (U72)	The EDID EEPROM type 24C04 on carrier board connected to LVDS_I2C bus. Holding display relevant DDC information. Used by BIOS to initialize LCD. KEAPI support with module.
External I/O	
LAN	two Gbit-Ethernet ports
USB	two USB 3.0 double stack and one µUSB connector for On The Go (OTG) function: powered for host, not powered for client. The 5 V output from USB 2.0 and USB OTG is separately electronically fused to 500 mA. The 5V output from USB 3.0 is electronically fused to 1000 mA each port.
HDMI	HDMI connector from SMARC module
DP++	DP++ Display port connector from SMARC module
COM1-4	4x COM RS232, 9-pin DSUB
Camera interfaces	Two Camera Header for cameras, including power, GPIO, I2C. Recommended Power should be 3.3 V, fused with 0.75 A resettable fuse.
Audio	Line-in and line-out 3.5mm jack; Front Panel 2x5 Pin Header (2.54mm), supporting both interfaces I2S and HDA selectable by jumper. On audio header is also Microphone and Headphone output.
Internal I/O	
LVDS	30-pin LVDS dual channel from SMARC module. Configurable 3.3 V / 5V voltage levels of power for different panels via jumper.
USB 2.0 Header	2.54 mm pitch 2x10-pin USB header with one USB pair
Backlight	Backlight PWM and power. Configurable 12 V/ 5 V voltage levels of backlight power for different panels via jumper. Maximum Power is 12 W continuous. If the selected panel exceeds, the provided power by this carrier evaluation of the SMARC module with LVDS can still be done with external panel power.
eDP	eDP connector, shared with LVDS as an option via resistors. PWR Out must provide +3.3 V +/-10 % with a maximum current of 500 mA and a minimum power capability of 1.5 W.
mSATA	1x slot (full size / half size ; SATA port)
LVDS	one LVDS and one LVDS/eDP1.4
PCIe X1	two PCIe 1X slots
mPCIe	two card slots (full size / half size) - PCIe & USB; support all MC3 mPCIe cards
SIM Card	SIM Card connected to both mPCIe
µSD	microSD card socket from SMARC module

Controller Area Network (CAN)	two CAN interfaces
LEDs	SMD LEDs for storage activity, board status, device and power status (power good)
Internal Header and Jumper	
GPIO	GPIO Header 2.54 mm
eSPI header	eSPI header (2.54 mm pin header, dual row)
Power Management Header	2.54 mm pin header, dual row
Battery	1.5F Goldcap and/or CR2032 battery. Optional parallel usage supported.
Fan	4-pin fan connector, Voltage can be 5 V or 12 V (default)
Carrier Board Controllers	
I2C EEPROM	General purpose EEPROM I2C
SPI Socket	SPI socket with 64 MB Flash
HDA Codec	TSI 92HD73C HDA Codec
I2S Codec	WM8904 I2S Codec
EEPROM DDC	Holding display relevant DDC information. Used by BIOS to initialize LCD.
Carrier Board Power	
Power input	12 V input power connector, used as an alternative power for module to support wide voltage range. 12 V DC power connector for powering carrier and module 5 V. Separate input power connector for module with voltage range: 3.0 V to 5.25 V DC
LED status	
Power LEDs	Power good of carrier power lanes
CARRIER_PWR_ON	Power on
CARRIER_STB#	CARRIER_STB#
SATA_ACT#	SATA activity LED
Power rails	1.8 V; 3.3 V; 5 V
GPIO	GPIO indication LEDs
Watchdog	Watchdog indication LED

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

Table 2: Environmental Conditions

Operating	0°C to +70°C Some connectors and supercap has operating temperature only 0°C to +70°C, relative humidity (non-condensing) 10 % to 93 % at 40°C
Storage	-40°C to +85°C relative humidity (non-condensing) 10 % to 95 % at 40°C
Electromagnetic Compatibility (EMC) and Interference (EMI)	The board shall be designed to meet the following requirements: EMC Emission EN 55022 Class B, FCC CFR part 15 Class B
Shock/Vibration/ Bump	Shock & Vibration according to IEC/EN60068-2-6 and IEC/EN60068-2-27
Theoretical MTBF	not applicable
Restriction of Hazardous Substances (RoHS) II Compliance	RoHS II compliant
Safety	The board shall be designed to meet the following requirements: ▶ UL 60950, 3rd edition (US and Canada) ▶ EN 60950-1 (Europe)

5/ Jumpers and Connectors

5.1. Hardware Configuration Setting

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on the board are in the proper position. The default settings shipped from factory are marked with an asterisk (*).

In general, jumpers on the board are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here, NC stands for “Not Connect”.

5.1.1. Jumpers and Connectors

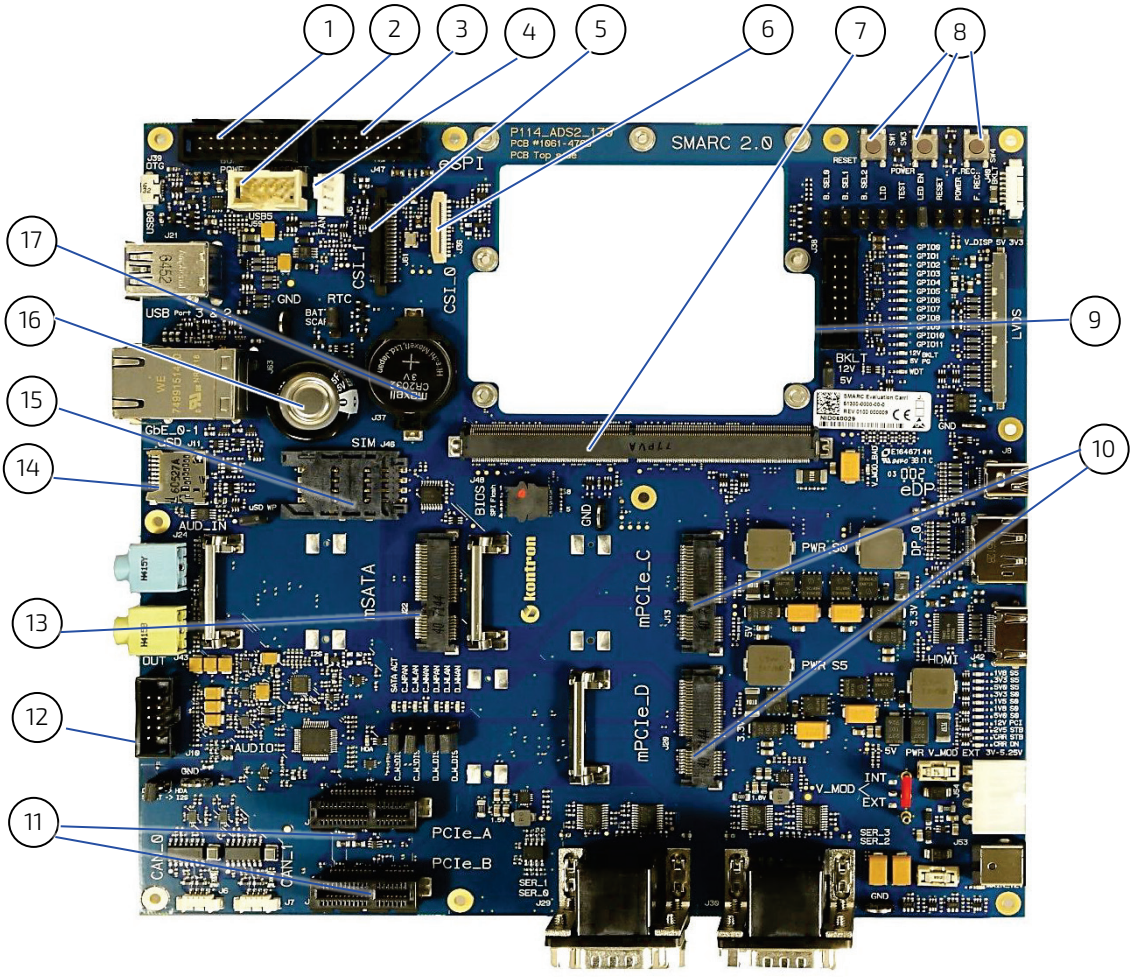
Table 3: Jumpers and Connectors

Connector	Function	Remark
High current jumper (H8 with contacts J55, J56 and J57)	Module power selection: Either internal power via J53 (5 V supply), or external via J54 (3 to 5.25 V supply). ATTENTION: J54 powers the module ONLY! Carrier still needs to be powered via 12V, through J53.	1x3-pin Jumper
5 V/3.3 V (J4)	Display voltage selection (3.3 V or 5 V)	1x3-pin Jumper
5 V/12 V (J23)	Display backlight voltage selection (5 V or 12 V)	1x3-pin Jumper
A_W_Disable_1 (J49)	Disable miniPCIe radio operation	1x2-pin Jumper
A_W_Disable_2 (J50)	Disable miniPCIe radio operation	1x2-pin Jumper
B_W_Disable_1 (J51)	Disable miniPCIe radio operation	1x2-pin Jumper
B_W_Disable_2 (J52)	Disable miniPCIe radio operation	1x2-pin Jumper
CODEK_OPTION_SW_I2S_HDA# (J31)	Audio Codec Multipexor HDA (default)/I2S Codec	1x2-pin Jumper
LEDs ENABLE (J44)	Enable/Disable status and power LEDs	1x2-pin Jumper
V_BAT_JP (J58)	Selection between Battery or Goldcap	1x3-pin Jumper
USB 2.0 (J59)	2.54 mm pitch USB header with one USB pair	2x5 pin header
SMARC (J1)	SMARC connector	1x314-connector
LVDS/eDP (J3)	LVDS dual channel. From SMARC module. Configurable 3.3 V / 5 V voltage levels of power for different panels via jumper.	
HDMI (J42)	HDMI connector from SMARC module	
DP++ (J12)	Display port connector from SMARC module	
PCIe x1 (J2)	2x PCIe 1x slot	standard
mPCIe (J13/J20)	2x card slot (full size / half size) - PCIe & USB; support all MC3 mPCIe cards	standard
mSATA (J22)	1x slot (full size / half size ; SATA port)	standard
Audio (J24 IN/J43 OUT)	Line-in and line-out 3.5mm jack; Front Panel 2x5 Pin Header (2.54mm)	2x5 header
CAN (J6/J7)	2x CAN, Molex 53261-0471 or similar	1x4 header
Power Management Header (J45)	SYS-Signals Header (2.54mm pin header)	2x8 header

Connector	Function	Remark
SD Card (J9)	SD card write protect setting	
Fan (J62)	Fan	1x4 header
GPIO (J38, U33, U34, U35)	GPIO Header 2.54mm	2x8 header

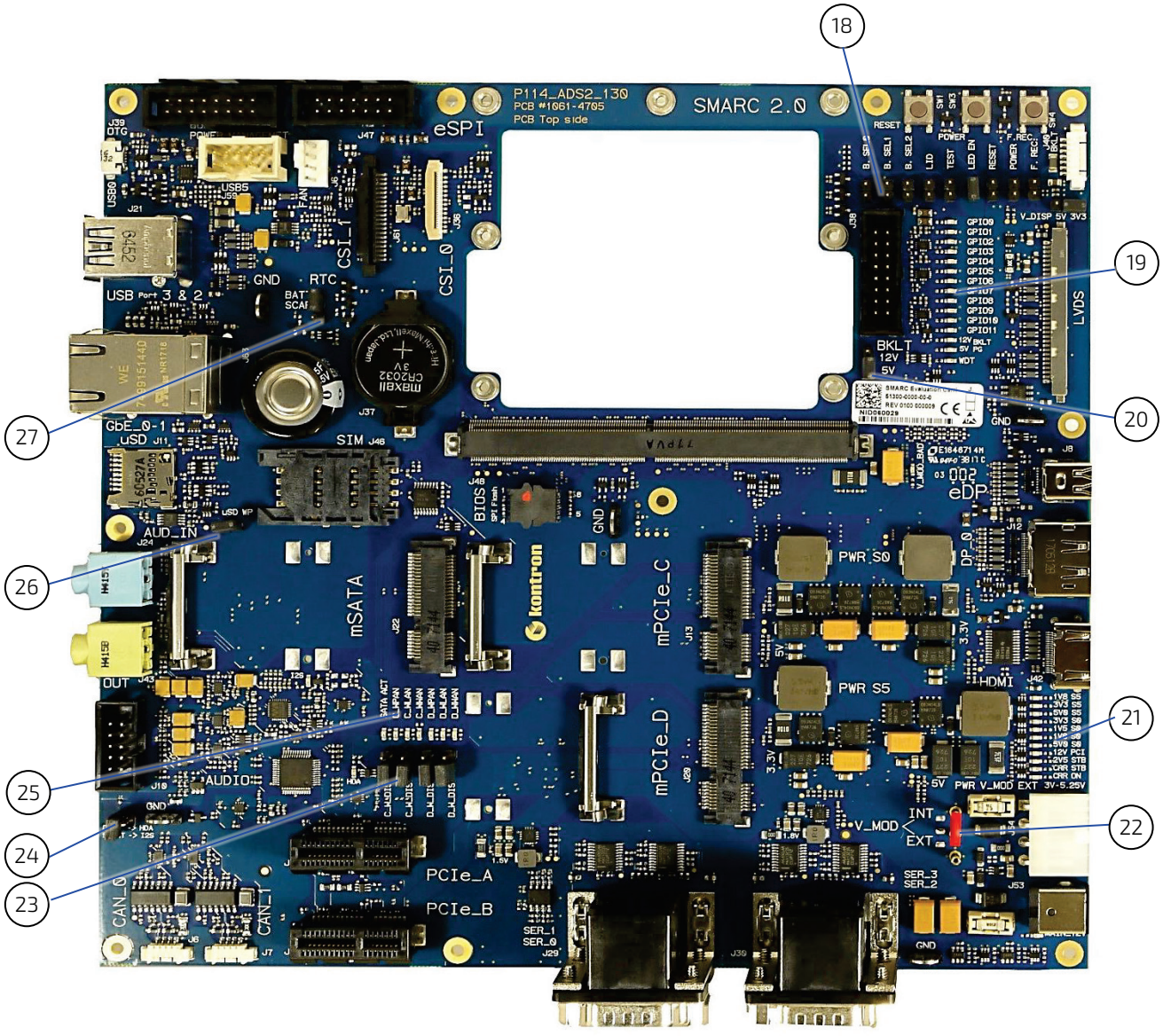
5.2. Mainboard views and I/O locations

Figure 2: Top View



1. Power Management Header
2. USB 2.0 internal
3. eSPI Header
4. Fan Connector
5. Camera Serial Interface (J61)
6. Camera Serial Interface (J36)
7. SMARC Interface
8. Button Switches
9. GPIO
10. mPCIe
11. 2x PCIe x1
12. Audio
13. mSATA
14. Micro-SD Card Connector
15. SIM Card
16. Goldcap
17. Battery

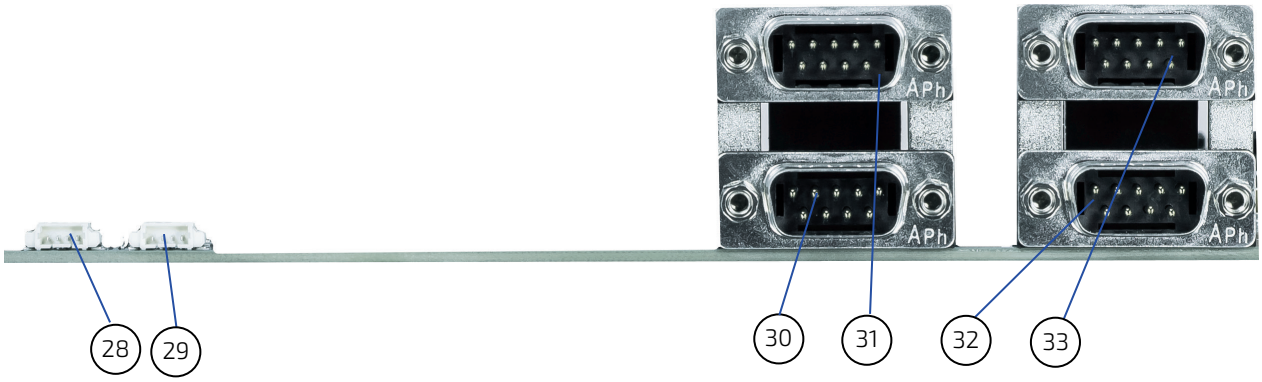
Figure 3: Top View with LEDs and Jumper



18. Jumper Boot Sel 0/1/2, LID, TEST, LED EN, RESET, POWER, F. REC, V DISP 5V 3V3
19. LEDs GPIO 0-10, 12 V/5 V BKLT, WDT
20. Jumper BKLT 12 V/5 V
21. LEDs S5, S0, PCI, 2V5 STB, CRR STB, CRR ON
22. Jumper V_MOD 5V/EXT
23. Jumper C_W_DI, D_W_DI
24. Jumper HDA/I2S
25. LEDs SATA ACT, WPAN, WLAN, WWAN
26. Jumper µSD WP
27. Jumper RTC BATT/SCAP

5.3. Front View

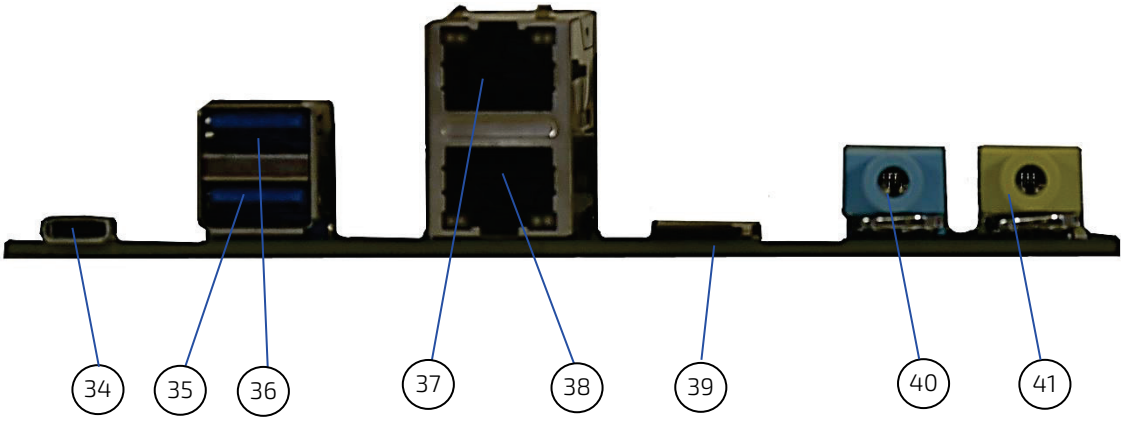
Figure 4: Front View



28. CAN Connector CAN_0
29. CAN Connector CAN_1
30. UART SER_0
31. UART SER_1
32. UART SER_2
33. UART SER_3

5.4. Front Left View

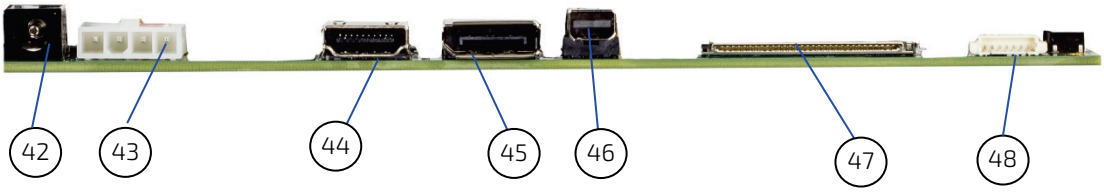
Figure 5: Front Left View



34. µUSB 2.0 OTG Connector
35. USB 3.0 Port 3
36. USB 3.0 Port 2
37. LAN GbE_1
38. LAN GbE_0
39. MicroSD Connector
40. Audio IN
41. Audio OUT

5.5. Front Right View

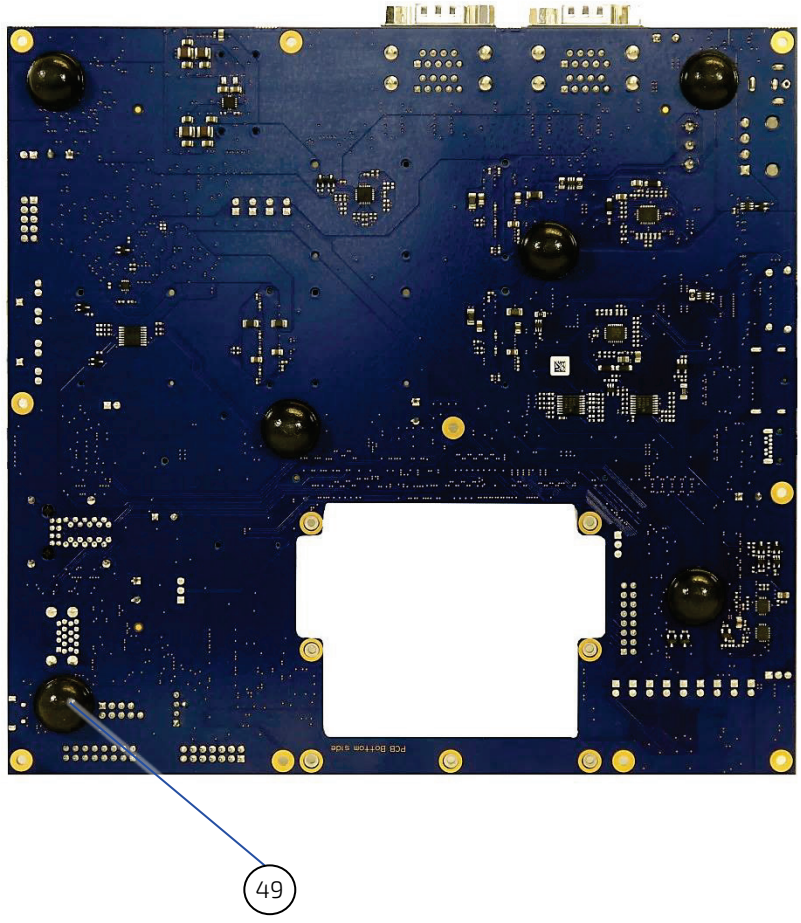
Figure 6: Front Right View



42. Power Jack: Main power connector
43. Power-in 4-pin: special power connector, for powering the module only (!) externally, with 3 to 5.25 V.
44. HDMI connector
45. DP connector
46. Mini Display Port connector
47. LVDS connector
48. Backlight connection

5.6. Rear Side

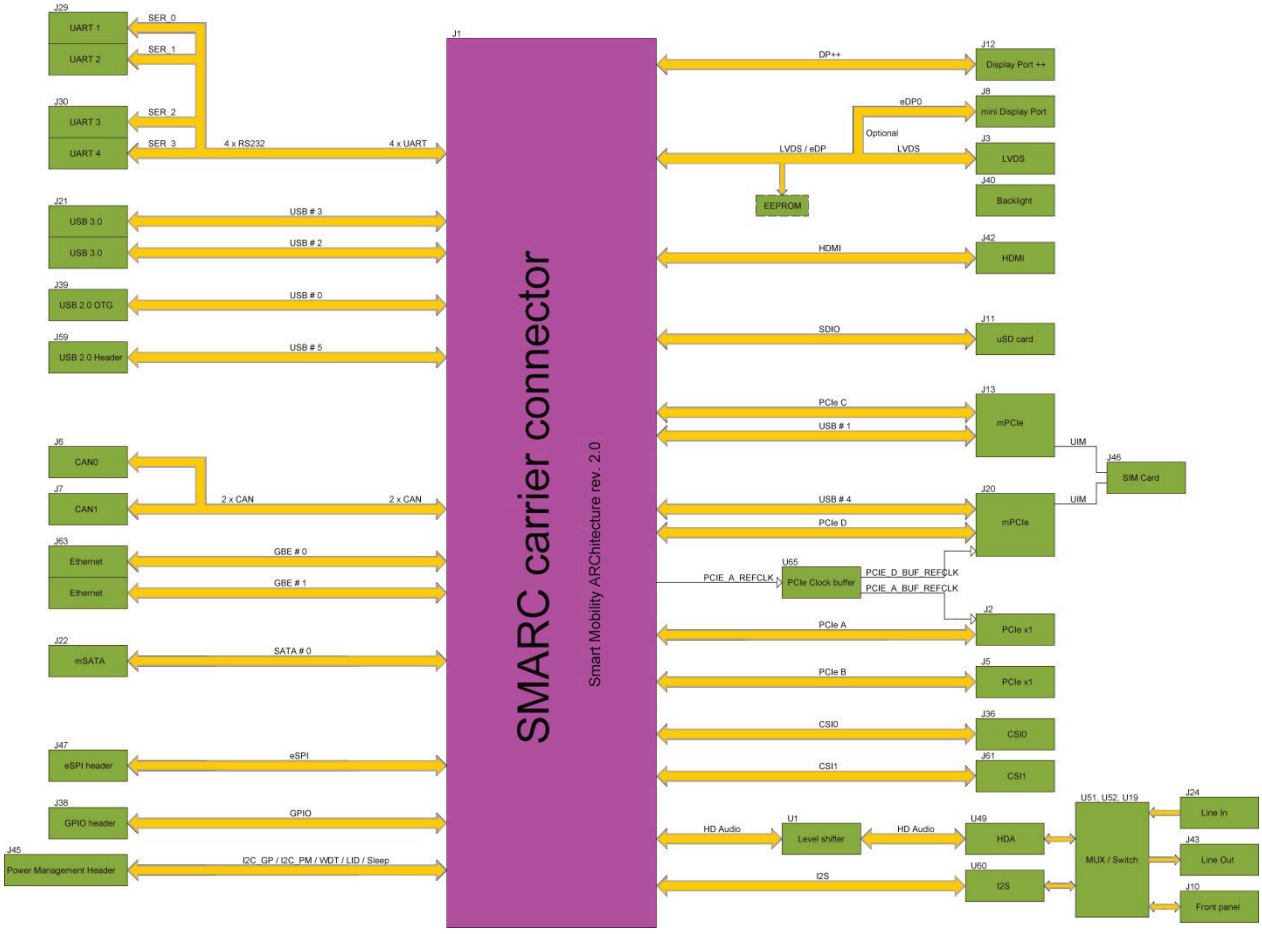
Figure 7: Rear Side from SMARC Eval-Carrier-2



49. Rubber feet 6x

6/ Block Diagram

Figure 8: Block Diagram for the SMARC Eval-Carrier-2

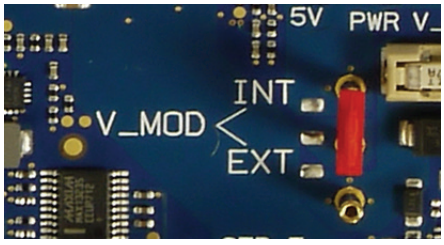


NOTICE

There are two different ways to power the carrier and module:

- Default and recommended: Power Connector J53 with 12 V, which also delivers 5 V to the module and 12 V to the board. Jumper V_MOD must be on position INT.

Figure 9: Red Jumper on position INT



- Alternative: Power Connector J53 with 12 V and Power Connector J54 with 5 V, which delivers power separately to the board (12 V) and module. Jumper V_MOD must be on position EXT.

7/ Maintenance and Status Information

7.1. LEDs

Figure 10: Power LEDs, see board position 21

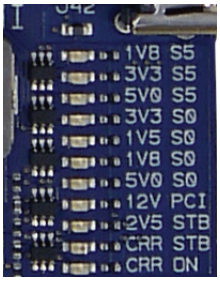


Table 4: Power LEDs

LED Color	Signal	Diode	Function
Green	V_1V8_S5	D59	Voltage V_1V8_S5 is present
Green	V_1V8_S0	D60	Voltage V_1V8_S0 is present
Green	V_1V5_S0	D61	Voltage V_1V5_S0 is present
Green	V_3V3_S5	D56	Voltage V_3V3_S5 is present
Green	V_3V3_S0	D57	Voltage V_3V3_S0 is present
Green	V_5V0_S5	D58	Voltage V_5V0_S5 is present
Green	V_5V0_S0	D38	Voltage V_5V0_S0 is present
Green	V_12V0_PCIE	D39	Voltage V_12V0_PCIE is present
Green	V_2V5_STB	D40	Voltage V_2V5_STB is present
Green	Carrier_PWR_ON	D64	Voltage Carrier_PWR_ON is present
Red	Carrier_STBY	D41	

Figure 11: GPIO and Backlight LEDs, see board position 19

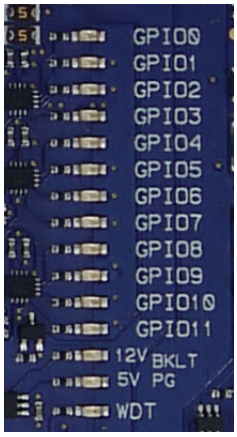


Table 5: Backlight voltage LEDs

LED Color	Signal	Diode	Function
Green	PG_BKLT_5V	D70	LED is shining when voltage is present
Green	PG_BKLT_12V0	D71	LED is shining when voltage is present

Table 6: GPIO LEDs

LED Color	Signal	Diode	Function
Blue	GPIO0/CAM0_PWR#	D8	GPIO0 level indication
Blue	GPIO1/CAM1_PWR#	D9	GPIO1 level indication
Blue	GPIO2/CAM0_RST#	D11	GPIO2 level indication
Blue	GPIO3/CAM1_RST#	D19	GPIO3 level indication
Blue	GPIO4/HDA_RST#	D24	GPIO4 level indication
Blue	GPIO5/PWM_OUT	D25	GPIO5 level indication
Blue	GPIO6/TACHIN	D26	GPIO6 level indication
Blue	GPIO7	D27	GPIO7 level indication
Blue	GPIO8	D28	GPIO8 level indication
Blue	GPIO9	D29	GPIO9 level indication
Blue	GPIO10	D30	GPIO10 level indication
Blue	GPIO11	D31	GPIO11 level indication

Table 7: Watchdog LEDs

LED Color	Signal	Diode	Function
Red	WDT	D6	Watchdog indication from module

Figure 12: GPIO and Backlight LEDs, see board position 25

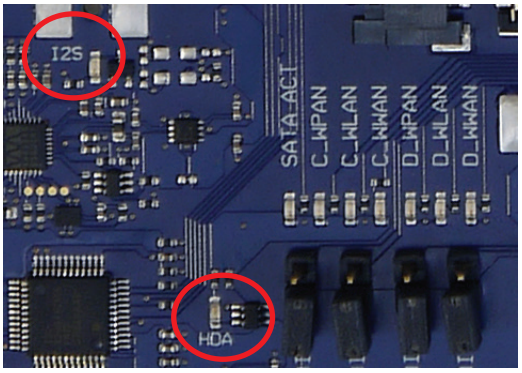


Table 8: Audio selection LEDs

LED Color	Signal	Diode	Function
Yellow	CODEK_OPTION_SW_I2S_HDA#	D44	I2S Codec is active; J31 is closed
Yellow	CODEK_OPTION_SW_I2S_HDA#	D45	HDA Codec is active; J31 is open

Table 9: SATA Activity LEDs

LED Color	Signal	Diode	Function
Red	SATA_ACT	D3	Indicate SATA activity

Table 10: mPCIe slot A LEDs

LED Color	Signal	Diode	Function
Yellow	MPCIEA_WPAN#	D35	WPAN Activity
Yellow	MPCIEA_WLAN#	D34	WLAN Activity
Yellow	MPCIEA_WWAN#	D33	WWAN Activity

Table 11: mPCIe slot B LEDs

LED Color	Signal	Diode	Function
Yellow	MPCIEB_WPAN#	D43	WPAN Activity
Yellow	MPCIEB_WLAN#	D42	WLAN Activity
Yellow	MPCIEB_WWAN#	D36	WWAN Activity

8/ Pin Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.
The connector definitions follow the following notation:

Table 12: Connector Definitions

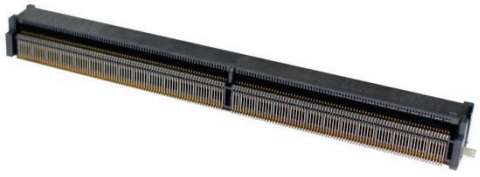
Column Name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AI: Analog Input AO: Analog Output I: Input, TTL compatible if nothing else stated IO: Input / Output, TTL compatible if nothing else stated IOT: Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible IOD: Input / Output, CMOS level Schmitt-triggered (Open drain output) NC: Not Connected O: Output, TTL compatible OC: Output, open-collector or open-drain, TTL compatible OT: Output with tri-state capability, TTL compatible LVDS: Low Voltage Differential Signal PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal
Designation	Type and number of item described

8.1. SMARC Connector (J1)

The SMARC connector has different pins on both sides:

- Top side: 74 pins are on the left side, 82 pins on the right side
- Bottom side: 75 pins are on the left side, 83 pins on the right side

Figure 13: 314-pin SMARC Connector for SMARC-Interface



P-Pin	Signal	S-Pin	Signal
P1	SMB_ALERT_1V8#	S1	CSI1_TX+ / I2C_CAM1_CK
P2	GND	S2	CSI1_TX- / I2C_CAM1_DAT
P3	CSI1_CK+	S3	GND
P4	CSI1_CK-	S4	RSVD
P5	GBE1_SDP	S5	CSI0_TX- / I2C_CAM0_CK
P6	GBE0_SDP	S6	CAM_MCK
P7	CSI1_RX0+	S7	CSI0_TX+ / I2C_CAM0_DAT
P8	CSI1_RX0-	S8	CSI0_CK+
P9	GND	S9	CSI0_CK-
P10	CSI1_RX1+	S10	GND
P11	CSI1_RX1-	S11	CSI0_RX0+
P12	GND	S12	CSI0_RX0-
P13	CSI1_RX2+	S13	GND
P14	CSI1_RX2-	S14	CSI0_RX1+
P15	GND	S15	CSI0_RX1-
P16	CSI1_RX3+	S16	GND
P17	CSI1_RX3-	S17	GBE1_MDI0+
P18	GND	S18	GBE1_MDI0-
P19	GBE0_MDI3-	S19	GBE1_LINK100#
P20	GBE0_MDI3+	S20	GBE1_MDI1+
P21	GBE0_LINK100#	S21	GBE1_MDI1-
P22	GBE0_LINK1000#	S22	GBE1_LINK1000#
P23	GBE0_MDI2-	S23	GBE1_MDI2+
P24	GBE0_MDI2+	S24	GBE1_MDI2-
P25	GBE0_LINK_ACT#	S25	GND
P26	GBE0_MDI1-	S26	GBE1_MDI3+
P27	GBE0_MDI1+	S27	GBE1_MDI3-
P28	GBE0_CTREF	S28	GBE1_CTREF
P29	GBE0_MDI0-	S29	PCIE_D_TX+

P-Pin	Signal	S-Pin	Signal
P30	GBE0_MDI0+	S30	PCIE_D_TX-
P31	SPI0_CS1#	S31	GBE1_LINK_ACT#
P32	GND	S32	PCIE_D_RX+
P33	SDIO_WP	S33	PCIE_D_RX-
P34	SDIO_CMD	S34	GND
P35	SDIO_CD#	S35	USB4+
P36	SDIO_CK	S36	USB4-
P37	SDIO_PWR_EN	S37	USB3_VBUS_DET
P38	GND	S38	AUDIO_MCK
P39	SDIO_D0	S39	I2S0_LRCK
P40	SDIO_D1	S40	I2S0_SDOUT
P41	SDIO_D2	S41	I2S0_SDIN
P42	SDIO_D3	S42	I2S0_CK
P43	SPI0_CS0#	S43	ESPI_ALERT0#
P44	SPI0_CK	S44	ESPI_ALERT1#
P45	SPI0_DIN	S45	RSVD
P46	SPI0_DO	S46	RSVD
P47	GND	S47	GND
P48	SATA_TX+	S48	I2C_GP_CK
P49	SATA_TX-	S49	I2C_GP_DAT
P50	GND	S50	HDA_SYNC / I2S2_LRCK
P51	SATA_RX+	S51	HDA_SDO / I2S2_SDOUT
P52	SATA_RX-	S52	HDA_SDI / I2S2_SDIN
P53	GND	S53	HDA_CK / I2S2_CK
P54	ESPI_CS0#	S54	SATA_ACT#
P55	ESPI_CS1#	S55	USB5_EN_OC#
P56	ESPI_CK	S56	ESPI_IO_2
P57	ESPI_IO_1	S57	ESPI_IO_3
P58	ESPI_IO_0	S58	ESPI_RESET#
P59	GND	S59	USB5+
P60	USB0+	S60	USB5-
P61	USB0-	S61	GND
P62	USB0_EN_OC#	S62	USB3_SSTX+
P63	USB0_VBUS_DET	S63	USB3_SSTX-
P64	USB0_OTG_ID	S64	GND
P65	USB1+	S65	USB3_SSRX+
P66	USB1-	S66	USB3_SSRX-
P67	USB1_EN_OC#	S67	GND
P68	GND	S68	USB3+
P69	USB2+	S69	USB3-
P70	USB2-	S70	GND
P71	USB2_EN_OC#	S71	USB2_SSTX+

P-Pin	Signal	S-Pin	Signal
P72	RSVD	S72	USB2_SSTX-
P73	RSVD	S73	GND
P74	USB3_EN_OC#	S74	USB2_SSRX+
	Key	S75	USB2_SSRX-
P75	PCIE_A_RST#		***Key***
P76	USB4_EN_OC#	S76	PCIE_B_RST#
P77	RSVD	S77	PCIE_C_RST#
P78	RSVD	S78	PCIE_C_RX+
P79	GND	S79	PCIE_C_RX-
P80	PCIE_C_REFCK+	S80	GND
P81	PCIE_C_REFCK-	S81	PCIE_C_TX+
P82	GND	S82	PCIE_C_TX-
P83	PCIE_A_REFCK+	S83	GND
P84	PCIE_A_REFCK-	S84	PCIE_B_REFCK+
P85	GND	S85	PCIE_B_REFCK-
P86	PCIE_A_RX+	S86	GND
P87	PCIE_A_RX-	S87	PCIE_B_RX+
P88	GND	S88	PCIE_B_RX-
P89	PCIE_A_TX+	S89	GND
P90	PCIE_A_TX-	S90	PCIE_B_TX+
P91	GND	S91	PCIE_B_TX-
P92	HDMI_D2+ / DP1_LANE0+	S92	GND
P93	HDMI_D2- / DP1_LANE0-	S93	DP0_LANE0+
P94	GND	S94	DP0_LANE0-
P95	HDMI_D1+ / DP1_LANE1+	S95	DP0_AUX_SEL
P96	HDMI_D1- / DP1_LANE1-	S96	DP0_LANE1+
P97	GND	S97	DP0_LANE1-
P98	HDMI_D0+ / DP1_LANE2+	S98	DP0_HPD
P99	HDMI_D0- / DP1_LANE2-	S99	DP0_LANE2+
P100	GND	S100	DP0_LANE2-
P101	HDMI_CK+ / DP1_LANE3+	S101	GND
P102	HDMI_CK- / DP1_LANE3-	S102	DP0_LANE3+
P103	GND	S103	DP0_LANE3-
P104	HDMI_HPD / DP1_HPD	S104	USB3_OTG_ID
P105	HDMI_CTRL_CK / DP1_AUX+	S105	DP0_AUX+
P106	HDMI_CTRL_DAT / DP1_AUX-	S106	DP0_AUX-

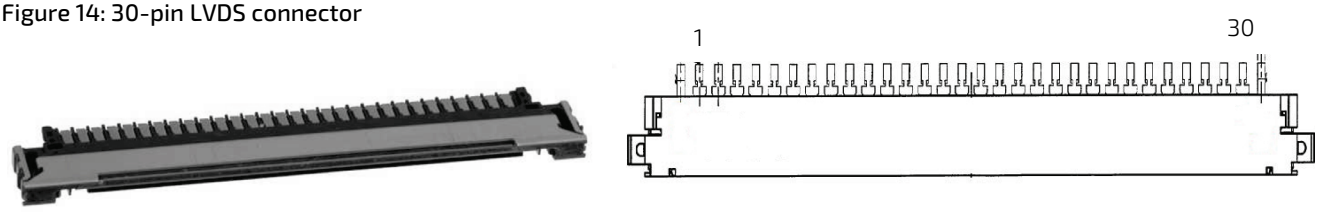
P-Pin	Signal	S-Pin	Signal
P107	DP1_AUX_SEL	S107	LCD1_BKLT_EN
P108	GPIO0 / CAM0_PWR#	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+
P109	GPIO1 / CAM1_PWR#	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-
P110	GPIO2 / CAM0_RST#	S110	GND
P111	GPIO3 / CAM1_RST#	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+
P112	GPIO4 / HDA_RST#	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-
P113	GPIO5 / PWM_OUT	S113	eDP1_HPD
P114	GPIO6 / TACHIN	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+
P115	GPIO7	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-
P116	GPIO8	S116	LCD1_VDD_EN
P117	GPIO9	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+
P118	GPIO10	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-
P119	GPIO11	S119	GND
P120	GND	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+
P121	I2C_PM_CK	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-
P122	I2C_PM_DAT	S122	LCD1_BKLT_PWM
P123	BOOT_SEL0#	S123	RSVD
P124	BOOT_SEL1#	S124	GND
P125	BOOT_SEL2#	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+
P126	RESET_OUT#	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-
P127	RESET_IN#	S127	LCD0_BKLT_EN
P128	POWER_BTN#	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+
P129	SER0_TX	S129	LVDS0_1- /

P-Pin	Signal	S-Pin	Signal
			eDP0_TX1- / DSI0_D1-
P130	SER0_RX	S130	GND
P131	SER0_RTS#	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+
P132	SER0_CTS#	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-
P133	GND	S133	LCD0_VDD_EN
P134	SER1_TX	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+
P135	SER1_RX	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-
P136	SER2_TX	S136	GND
P137	SER2_RX	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+
P138	SER2_RTS#	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-
P139	SER2_CTS#	S139	I2C_LCD_CK
P140	SER3_TX	S140	I2C_LCD_DAT
P141	SER3_RX	S141	LCD0_BKLT_PWM
P142	GND	S142	RSVD
P143	CAN0_TX	S143	GND
P144	CAN0_RX	S144	eDP0_HPD
P145	CAN1_TX	S145	WDT_TIME_OUT#
P146	CAN1_RX	S146	PCIE_WAKE#
P147	VDD_IN	S147	VDD_RTC
P148	VDD_IN	S148	LID#
P149	VDD_IN	S149	SLEEP#
P150	VDD_IN	S150	VIN_PWR_BAD#
P151	VDD_IN	S151	CHARGING#
P152	VDD_IN	S152	CHARGER_PRSNT#
P153	VDD_IN	S153	CARRIER_STBY#
P154	VDD_IN	S154	CARRIER_PWR_ON
P155	VDD_IN	S155	FORCE_RECOV#
P156	VDD_IN	S156	BATLOW#
		S157	TEST#

8.2. LVDS Connector (J3)

This connector provides data and power connection between Carrier Board and Display. This 30-pin lockable connector contains the LVDS output signals and the power to the LVDS display.

Figure 14: 30-pin LVDS connector



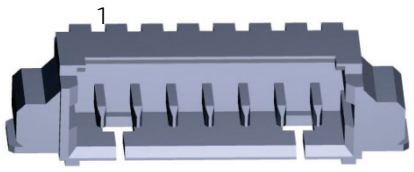
Pin	Signal	Description
1	LVDS_A_DATA[0]-	LVDS odd channel 0, minus signal
2	LVDS_A_DATA[0]+	LVDS odd channel 0, plus signal
3	LVDS_A_DATA[1]-	LVDS odd channel 1, minus signal
4	LVDS_A_DATA[1]+	LVDS odd channel 1, plus signal
5	LVDS_A_DATA[2]-	LVDS odd channel 2, minus signal
6	LVDS_A_DATA[2]+	LVDS odd channel 2, plus signal
7	GND	Ground
8	LVDS_A_CLK-	LVDS odd channel clock, minus signal
9	LVDS_A_CLK+	LVDS odd channel clock, plus signal
10	LVDS_A_DATA[3]-	LVDS odd channel 3, minus signal
11	LVDS_A_DATA[3]+	LVDS odd channel 3, plus signal
12	LVDS_B_DATA[0]-	LVDS even channel 0, minus signal
13	LVDS_B_DATA[0]+	LVDS even channel 0, plus signal
14	GND	Ground
15	LVDS_B_DATA[1]-	LVDS even channel 1, minus signal
16	LVDS_B_DATA[1]+	LVDS even channel 1, plus signal
17	GND	Ground
18	LVDS_B_DATA[2]-	LVDS even channel 2, minus signal
19	LVDS_B_DATA[2]+	LVDS even channel 2, plus signal
20	LVDS_B_CLK-	LVDS even channel clock,

Pin	Signal	Description
		minus signal
21	LVDS_B_CLK+	LVDS even channel clock plus signal
22	LVDS_B_DATA[3]-	LVDS even channel 3, minus signal
23	LVDS_B_DATA[3]+	LVDS even channel 3, plus signal
24	GND	Ground
25	FP_STRAP_1	Flat panel strapping pin 1
26	FP_STRAP_2	Flat panel strapping pin 2
27	FP_STRAP_3	Flat panel strapping pin 3
28	V_TFT	Flat panel power supply (3V3 or 5V)
29	V_TFT	Flat panel power supply (3V3 or 5V)
30	V_TFT	Flat panel power supply (3V3 or 5V)

In schematic are pin 1 and pin 32 shields and are not included in the table above.

8.3. Backlight Connector (J40)

Figure 15: 7-pin Backlight Connector

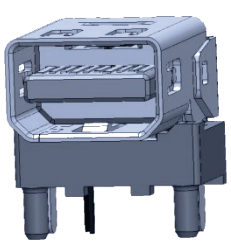


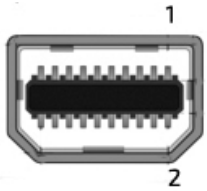
Pin	Signal	Type
1	NC	
2	Backlight Brightness 5V or 3.3V (jumper selection J4) PWM (0% - 100%)	Out (27.4 Ohm series resistor)
3	GND	Ground
4	V_BKLT - 12V or 5.0V (jumper selection J23)	Power
5	V_BKLT - 12V or 5.0V (max. 12W continuous, inrush limited with U54 or U55)"	Power
6	GND	Ground
7	Backlight enable (0 V: off; 5 V or 3 V3: on - jumper selection J4)	Out (27.4 Ohm series resistor)

8.4. eDP connector (embedded Display Port) (J8)

The connector provides eDP signals from SMARC board as an option on LVDS pins.

Figure 16: 20-pin eDP connector





Pin	Signal	Description
1	GND	Ground
2	In	Hot plug Detect
3	Out	ML_Lane 0 (p)
4	Config	CONFIG 1 *(See note 1)*
5	Out	ML_Lane 0 (n)
6	Config	CONFIG 2 *(See note 1)*
7	GND	Ground
8	GND	Ground
9	Out	ML_Lane 1 (p)
10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)
12	Out	ML_Lane 3 (n)
13	GND	Ground
14	GND	Ground
15	Out	ML_Lane 2 (p)
16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)
18	I/O	AUX_CH (n)
19	GND	Ground
20	PWR	DP_Power *(See note 2)*

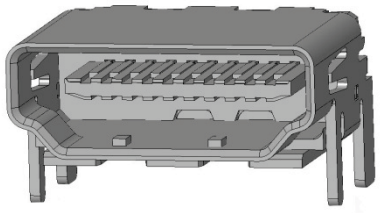
Note 1: Pins 4 and 6 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.

Note 2: Pin 20, PWR Out, must provide +3.3V+/-10% with a maximum current of 500mA and a minimum power capability of 1.5 watts.

Note3: Connection is according to DP specification v 1.2

8.5. HDMI connector (J42)

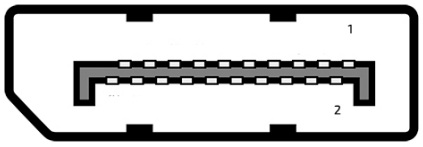
Figure 17: 19-pin HDMI connector



Pin	Signal
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved / Utility
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

8.6. DP connector (J12)

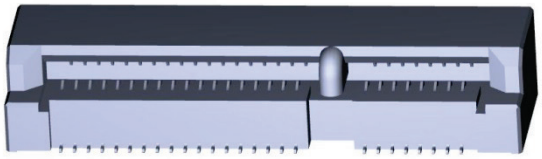
Figure 18: 20-pin DP connector

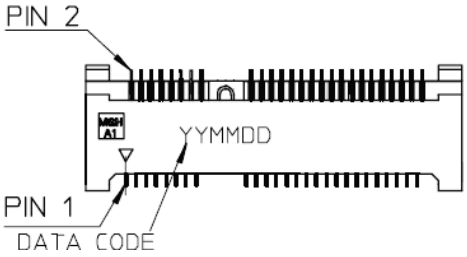


Pin	Signal	Pin	Signal
1	ML LANE 0+	2	GND (ML LANE 0)
3	ML LANE 0-	4	ML LANE 1+
5	GND (ML LANE 1)	6	ML LANE 1-
7	ML LANE 2+	8	GND (ML LANE 2)
9	ML LANE 2-	10	ML LANE 3+
11	GND (ML LANE 3)	12	ML LANE 3-
13	AUX_SEL#	14	Pull-down to GND
15	AUX CH+	16	GND (AUX CH)
17	AUX CH-	18	Hot plug
19	GND (GND_DDC)	20	+3.3V (DDC EEPROM power) Max 500mA

8.7. Mini PCIe Card socket 1 (J13)

Figure 19: 52-pin Mini PCIe Card



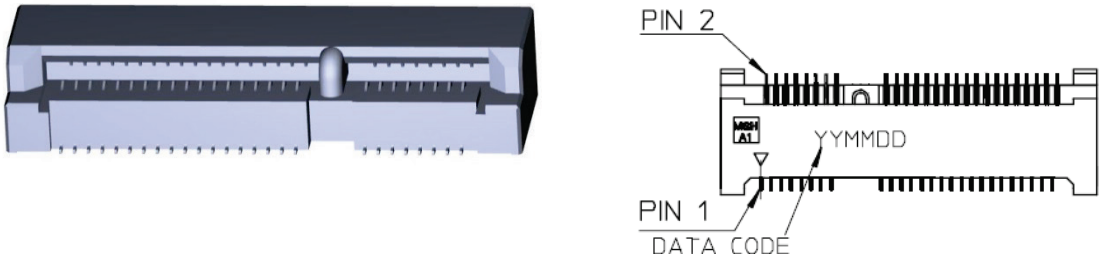


Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3V_S5
3	N.C.	4	GND
5	N.C.	6	+1.5V_S0
7	CLKREQ#	8	UIM-PWR
9	GND	10	UIM-DATA
11	PCIe_REFCLK-	12	UIM-CLK

Pin	Signal	Pin	Signal
13	PCIe_REFCLK+	14	UIM-RST
15	GND	16	UIM-VPP
17	UIM-C8	18	GND
19	UIM-C4	20	W_DISABLE#
21	GND	22	PLTRST#
23	PCIe_RX-	24	+3.3V_S5
25	PCIe_RX+	26	GND
27	GND	28	+1.5V_S0
29	GND	30	PU 3.3V(S5) (Optional: SMB_CLK)
31	PCIe_TX-	32	PU 3.3V(S5) (Optional: SMB_DAT)
33	PCIe_TX+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3V_S5	40	GND
41	+3.3V_S5	42	PU 3.3V(S0)
43	GND	44	PU 3.3V(S0)
45	N.C.	46	PU 3.3V(S0)
47	N.C.	48	+1.5V_S0
49	N.C.	50	GND
51	N.C.	52	+3.3V_S5

8.8. Mini PCIe Card socket 2 (J20)

Figure 20: 52-pin Mini PCIe Card



Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3V_S5
3	N.C.	4	GND
5	N.C.	6	+1.5V_S0
7	CLKREQ#	8	UIM-PWR
9	GND	10	UIM-DATA

Pin	Signal	Pin	Signal
11	PCIe_REFCLK-	12	UIM-CLK
13	PCIe_REFCLK+	14	UIM-RST
15	GND	16	UIM-VPP
17	UIM-C8	18	GND
19	UIM-C4	20	W_DISABLE#
21	GND	22	PLTRST#
23	PCIe_RX-	24	+3.3V_S5
25	PCIe_RX+	26	GND
27	GND	28	+1.5V_S0
29	GND	30	PU 3.3V(S5) (Optional: SMB_CLK)
31	PCIe_TX-	32	PU 3.3V(S5) (Optional: SMB_DAT)
33	PCIe_TX+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3V_S5	40	GND
41	+3.3V_S5	42	PU 3.3V(S0)
43	GND	44	PU 3.3V(S0)
45	N.C.	46	PU 3.3V(S0)
47	N.C.	48	+1.5V_S0
49	N.C.	50	GND
51	N.C.	52	+3.3V_S5

8.9. SIM card socket (J46)

Figure 21: 8-pin SIM card socket

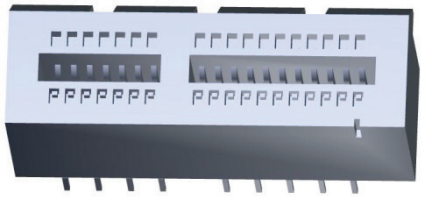
Pin	Signal
1	UIM_PWR
2	UIM_RST
3	UIM_CLK
4	UIM_C4
5	GND
6	UIM_VPP / NC
7	UIM_DATA
8	UIM_C8

NOTICE

Never use two mPCIe cards in both slots using UIM interface at the same time. SIM Card is directly shared between both slots.

8.10. PCIe x1 connector 1 (J2)

Figure 22: 52-pin PCIe x1 connector

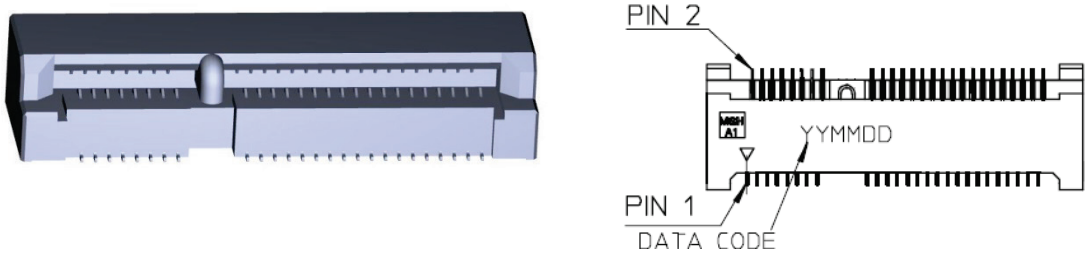


Pin	Signal	Pin	Signal
A1	PRSNT1#	B1	V_12V0_S0

Pin	Signal	Pin	Signal
A2	V_12V0_S0	B2	V_12V0_S0
A3	V_12V0_S0	B3	V_12V0_S0
A4	GND	B4	GND
A5	JTAG2_TCK	B5	SMCLK
A6	JTAG3_TDI	B6	SMDAT
A7	JTAG4_TDO	B7	GND
A8	JTAG5_TMS	B8	V_3V3_S0
A9	V_3V3_S0	B9	JTAG1_TRST#
A10	V_3V3_S0	B10	V_3V3_AUX
A11	PERST#	B11	WAKE#
A12	GND	B12	RSVD – N.C.
A13	REFCLK+	B13	GND
A14	REFCLK-	B14	PET0+
A15	GND	B15	PET0-
A16	PER0+	B16	GND
A17	PER0-	B17	PRSNT2#
A18	GND	B18	GND

8.11. Mini SATA Card Socket (J22)

Figure 23: 52-pin SATA Card Socket



Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3V_S5
3	N.C.	4	GND
5	N.C.	6	+1.5V_S0
7	N.C.	8	UIM-PWR
9	GND	10	UIM-DATA
11	N.C	12	UIM-CLK
13	N.C	14	UIM-RST
15	GND	16	UIM-VPP
17	N.C.	18	GND
19	N.C.	20	W_DISABLE#
21	GND	22	PLTRST#

Pin	Signal	Pin	Signal
23	SATA_RX+	24	+3.3V_S5
25	SATA_RX-	26	GND
27	GND	28	+1.5V_S0
29	GND	30	PU 3.3V(S5) (Optional: SMB_CLK)
31	SATA_TX-	32	PU 3.3V(S5) (Optional: SMB_DAT)
33	SATA_TX+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3V_S5	40	GND
41	+3.3V_S5	42	PU 3.3V(S0)
43	GND	44	PU 3.3V(S0)
45	N.C.	46	PU 3.3V(S0)
47	N.C.	48	+1.5V_S0
49	N.C.	50	GND
51	PU 3.3V(S5)	52	+3.3V_S5

8.12. Audio Connector Line In (J24/J43)

Figure 24: Audio Jacks

Pin Assignment J43 (Line Out, green, Figure 24 left)

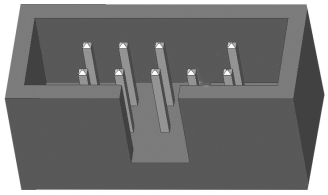
Pin	Signal
1	Audio GND
2	Line Out Left
3	Line Out Sense
4	Audio GND
5	Line Out Right

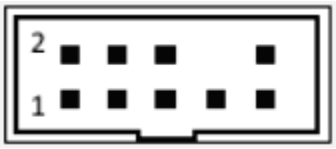
Pin Assignment J24 (Line In, blue, Figure 24 right)

Pin	Signal
1	Audio GND
2	Line In Left
3	Line In Sense
4	Audio GND
5	Line In Right

8.13. Audio Connector (J10)

Figure 25: 9-pin Audio Connector Header

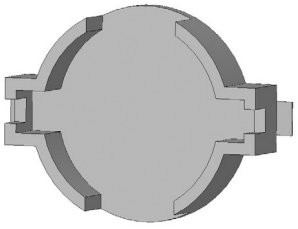




Pin	Signal	Pin	Signal
1	MIC_L	2	AGND
3	MIC_R	4	PRESENCE#
5	HEADPHONE_R	6	MIC_JD
7	SENSE	8	-
9	HEADPHONE _L	10	LINE_JD

8.14. RTC battery holder (J37)

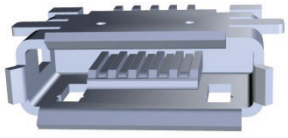
Figure 26: RTC battery holder



Pin	Signal
Positive (+)	V_BAT_INT
Negative (-)	GND

8.15. µUSB 2.0 OTG connector (J39)

Figure 27: µUSB 2.0 OTG connector



Pin	Signal
1	+5 V USB output (500 mA max.)
2	USB Data -
3	USB Data +
4	ID
5	Ground

8.16. J21 – USB Connections

Figure 28: USB 2.0 / 3.0 socket

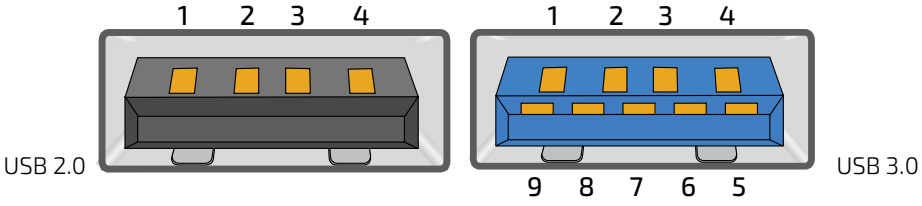


Table 13: Pin Assignment

Pin	Type	Signal	Note
1	PWR	5 V / SB 5 V	USB2.0 / 3.0
2	IO	USB 3-	USB2.0 / 3.0
3	IO	USB 3+	USB2.0 / 3.0
4	PWR	GND	USB2.0 / 3.0
5	IO	RX 2-	USB3.0
6	IO	RX 2+	USB3.0
7	PWR	GND	USB3.0
8	IO	TX 2-	USB3.0
9	IO	TX 2+	USB3.0

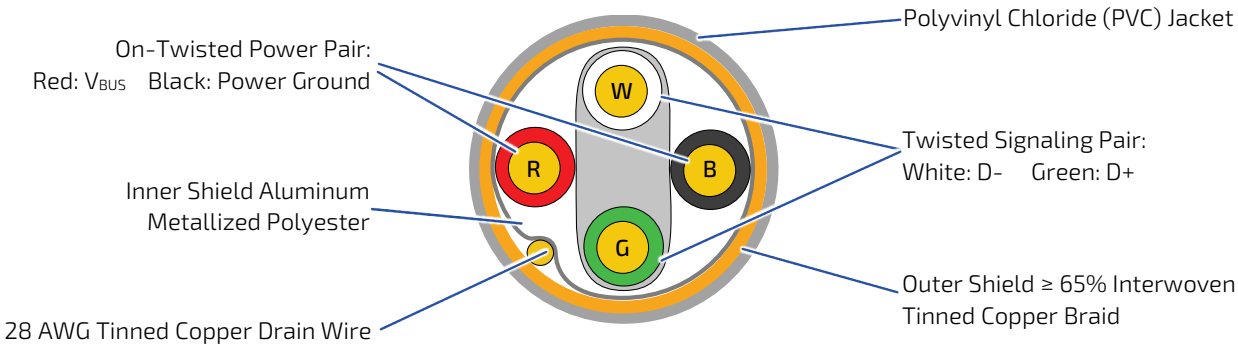
Table 14: Signal Description

Signal	Description
USBn+ USBn-	Differential pair works as serial differential receive/transmit data lines.

Signal	Description
RXn+ RXn- TXn+ TXn-	(n= 0,1,2,3)
5 V / SB5 V	5 V supply for external devices. SB5 V is supplied during power-down to allow wakeup on USB device activity. Power is maximum 1 A for each USB 3.0 port (protected with 1 A load switch for each port).

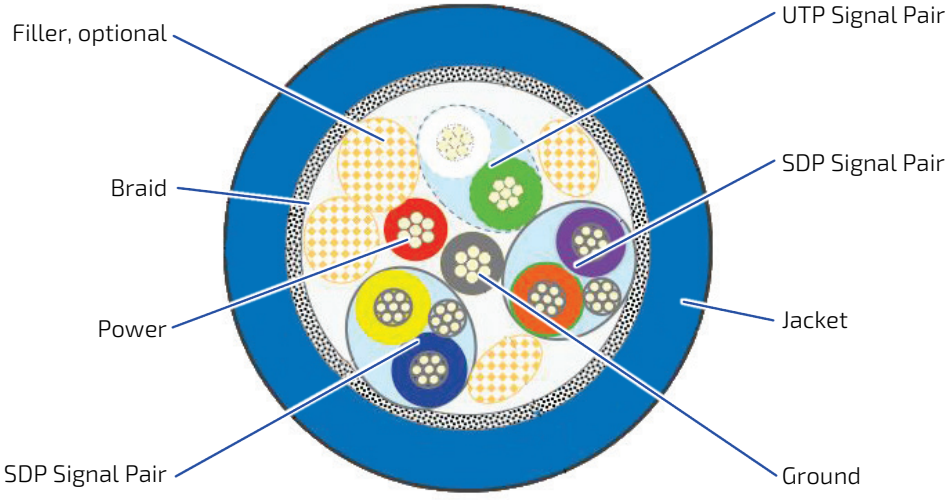
For HiSpeed rates it is required to use a USB cable, which is specified in USB2.0 standard:

Figure 29: USB 2.0 High Speed Cable



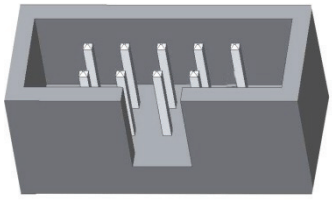
For SuperSpeed rates it is required to use a USB cable, which is specified in USB3.0 standard:

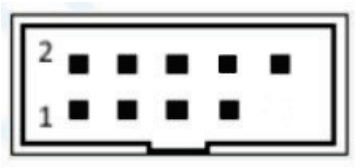
Figure 30: USB 3.0 High Speed Cable



8.17. USB 2.0 Header (J59)

Figure 31: 9-pin USB Header





Pin	Signal	Pin	Signal
1	+5 V USB output (500 mA max.)	2	N.C.
3	USB Data -	4	N.C.
5	USB Data +	6	N.C.
7	Ground	8	N.C.
9		10	N.C.

8.18. Double USB 3.0 Connector (J21)

This connector provides two USB 3.0 connections (downstream). The 5 V output is electronically fused to 1000 mA each port.

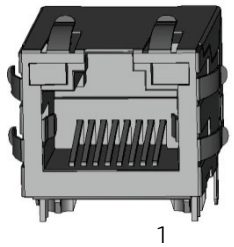
Figure 32: Double USB 3.0 Connector

Pin	Signal	Remark
1	VBUS +5V (900mA max.)	Low, Full & High Speed (USB 2.0) contact pins Bottom con.
2	USB Data -	
3	USB Data +	
4	GND	
5	USB SSRX-	Super Speed (USB3.0) contact pins Bottom con.
6	USB SSRX+	
7	GND	
8	USB SSTX-	
9	USB SSTX+	
10	VBUS +5V (900mA max.)	Low, Full & High Speed (USB 2.0) contact pins Top con.
11	USB Data -	
12	USB Data +	
13	GND	
14	USB SSRX-	Super Speed (USB3.0) contact pins Top con.
15	USB SSRX+	
16	GND	
17	USB SSTX-	
18	USB SSTX+	
Shield	Shield	

8.19. LAN Connector (J36 and J41)

This connector provides an isolated Ethernet 1000Base-T port, which is connected to an on-board LAN Controller. The galvanic isolated transformers (1500 V_{rms}, Voltage Regulator Module (VRM)) are integrated in the LAN connectors.

Figure 33: LAN Connector



1

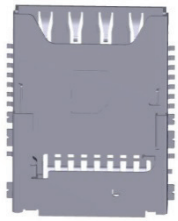
Pin	Signal	Pin	Signal
1	MDI0+	2	MDI0-
3	MDI1+	4	MDI1-
5	CTREF	6	CTREF
7	MDI2+	8	MDI2-
9	MDI3+	10	MDI3-
11	Green (A) / Yellow (C)	12	Green (C) / Yellow (A)
13	Green (A) / Yellow (C)	14	Green (C) / Yellow (A)

Left LED State	Link Activity State
Off	Link not active
Green (constant on)	Link active
Green (flashing)	Link active plus activity

Right LED State	Link Speed
Off	10 Base-T
Green (constant on)	100 Base-T
Green (flashing)	1000 Base-T

8.20. Micro-µSD Card Connector (J11)

Figure 34: Micro-µSD Card Connector



Pin	Signal
1	SD_DAT[2]
2	CD / SD_DAT[3]
3	CMD
4	VDD
5	SD_CLK
6	GND / VSS
7	SD_DAT[0]
8	SD_DAT[1]
9	CD_DETECT
10	CD_GND
11	SH_GND
12	SH_GND
13	SH_GND
14	SH_GND

8.21. UART-SER Connector (J29/J30)

This standard double D-SUB 9-pin connector contains the SER0 and SER1 signals.

Figure 35: Double D-SUB 9-pin Connector

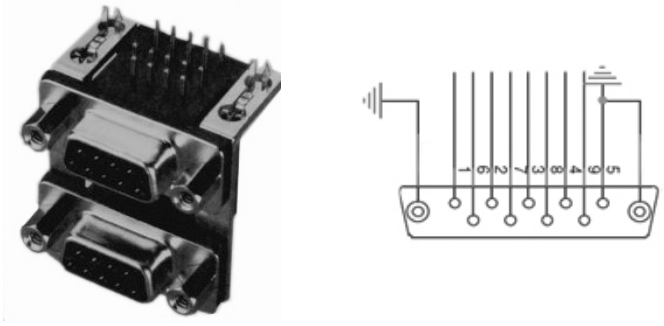


Table 15: Bottom SER0/UART0

Pin	Signal	Direction
1	N.C.	
2	RXD (Receive Data)	In
3	TXD (Transmit Data)	Out
4	N.C.	
5	GND	
6	N.C.	
7	RTS# Request to Send)	Out
8	CTS# (Clear to Send)	In
9	N.C.	

Table 16: Top SER1/UART1

Pin	Signal	Direction
1	N.C.	
2	RXD (Receive Data)	In
3	TXD (Transmit Data)	Out
4	N.C.	
5	GND	
6	N.C.	
7	N.C.	
8	N.C.	
9	N.C.	

Table 17: Bottom SER2/UART2

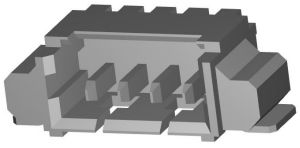
Pin	Signal	Direction
1	N.C.	
2	RXD (Receive Data)	In
3	TXD (Transmit Data)	Out
4	N.C.	
5	GND	
6	N.C.	
7	RTS# Request to Send)	Out
8	CTS# (Clear to Send)	In
9	N.C.	

Table 18: Top SER3/UART3

Pin	Signal	Direction
1	N.C.	
2	RXD (Receive Data)	In
3	TXD (Transmit Data)	Out
4	N.C.	
5	GND	
6	N.C.	
7	N.C.	
8	N.C.	
9	N.C.	

8.22. CAN Connector (J6/J7)

Figure 36: CAN_0/CAN_1 Connector



1

Pin	Signal
1	CAN0_L
2	CAN0_H
3	V_5V0
4	GND

8.23. Camera Serial Interface (CSI0) Connector (J36)

Figure 37: 15-pin Camera CSI Connector

Pin	Signal
1	NC
2	NC
3	CSI0_RX0-
4	NC
5	CSI0_RX0+
6	NC
7	CSI0_CLK-
8	CSI0_PCLK
9	CSI0_CLK+
10	GND
11	CSI0_RX1+
12	CSI0_XCLK_1V8
13	CSI0_RX1+
14	V_1V8_S0_CSIO
15	V_1V5_S0_CSIO
16	CSIO_HREF
17	CSIO_PWDN_1V8_C
18	CSIO_VSYNC
19	RESET_CSIO_1V8_C
20	CSIO_I2C_CLK_1V8_C
21	V_2V8_DAT_1V8_C
22	CSIO_I2C_DAT_1V8_C
23	AGND_CSI
24	NC

Pin 14: 1.8 V with resettable fuse 0.75 A

Pin15: 1.5 V with resettable fuse 0.75 A

Pin 21: 2.8 V from LDO regulator with over current protection. Maximum 100 mA not fused.

8.24. Camera Serial Interface (CSI1) Connector (J61)

Figure 38: 20-pin Camera CSI Connector

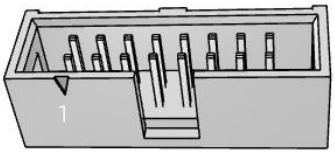
1

Pin	Signal
1	GND
2	CSI1_RX0-
3	CSI1_RX0+
4	GND
5	CSI1_RX1-
6	CSI1_RX1+
7	GND
8	CSI1_RX2-
9	CSI1_RX2+
10	GND
11	CSI1_RX3-
12	CSI1_RX3+
13	GND
14	CSI1_CLK-
15	CSI1_CLK+
16	GND
17	CSI1_CAM_CLK_1V8
18	CSI1_I2C_CLK_3V3
19	CSI1_I2C_DAT_3V3
20	V_3V3_S0_CSI1

Pin 20 with 3.3 V and 0.75 A resettable fuse

8.25. GPIO Header (J38)

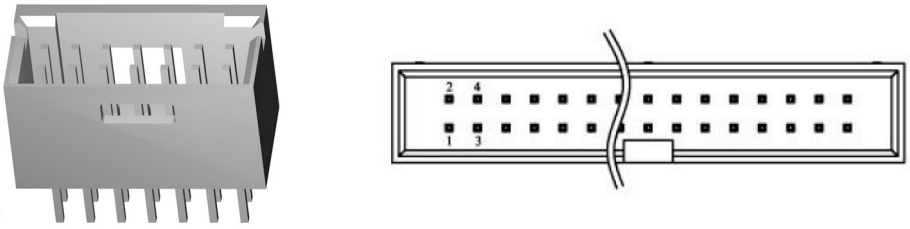
Figure 39: 2x8-pin GPIO Header



Pin	Signal	Pin	Signal
1	VCC 1.8V	2	VCC 3.3V
3	GPIO_0	4	GPIO_1
5	GPIO_2	6	GPIO_3
7	GPIO_4	8	GPIO_5
9	GPIO_6	10	GPIO_7
11	GPIO_8	12	GPIO_9
13	GPIO_10	14	GPIO_11
15	GND	16	GND

8.26. Enhanced Serial Peripheral Interface Bus (eSPI) Connector (J47)

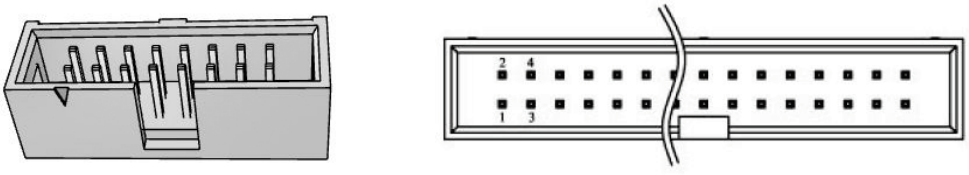
Figure 40: 2x7-pin eSPI Connector



Pin	Signal	Pin	Signal
1	VCC 1.8V	2	VCC 3.3V
3	ESPI_CS0	4	ESPI_CS1
5	ESPI_IO0	6	ESPI_IO1
7	ESPI_IO2	8	ESPI_IO3
9	ESPI_RESET#	10	ESPI_ALERT0
11	ESPI_ALERT1	12	ESPI_CK
13	GND	14	GND

8.27. Power Management Header (J45)

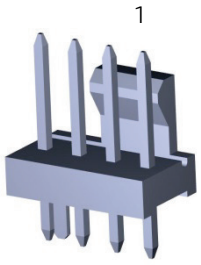
Figure 41: 2x8-pin Power Management Header



Pin	Signal	Pin	Signal
1	VCC 1.8V	2	VCC 3.3V
3	VIN_PWR_BAD#	4	CARRIER_PWR_ON#
5	CARRIER_STB#	6	SLEEP#
7	LID#	8	PWR_BTN
9	RESET_OUT#	10	RESET_IN#
11	BATLOW#	12	I2C_PM_DAT
13	I2C_PM_CK	14	SMB_ALERT_1V8#
15	GND	16	GND

8.28. Fan Connector (J62)

Figure 42: 4-pin Fan Connector



Pin	Signal	Description
1	GND	
2	V_S0_FAN	12 V by default. Can optionally be changed to 5 V, via removing FB69 and populating FB68.
3	FAN_TACH_J	FAN-Tacho signal
4	FAN_PWMOUT_J	PWM output for FAN control

8.29. Power-In Connector (J53)

Figure 43: Power-In Connector

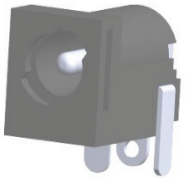


Table 44: Power-In Connector

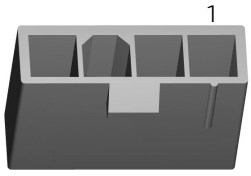
Pin	Signal	Description
1	V_12V0_IN_CON	Main power input for either both module and carrier (default), or for carrier only, when J54 is used.
2	GND	

⚠CAUTION

The board can be supplied via the AC/DC adapter plugged into the power jack. Such adapters have usually no connection to protective earth. Consequently, the potential of the conductive parts on the board may drift. If a human touches such a part, this may lead to an electric shock. The board must be grounded separately, if the unit is supplied via power jack.

8.30. Module Power-In Connector (J54)

Figure 45: Module Power-In Connector



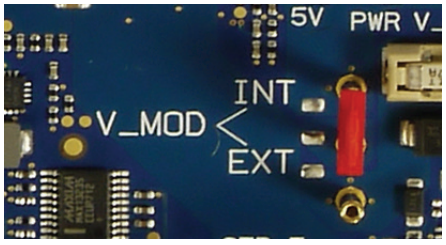
Pin	Signal	Description
1	V_MODULE	Module Power from 3.0 V to 5.25 V is independent from Carrier power.
2	GND	
3	N.C.	Not connected
4	GND	

NOTICE

There are two different ways to power the carrier and module:

- Default and recommended: Power Connector J53 with 12 V, which also delivers 5 V to the module and 12 V to the board. Jumper V_MOD must be on position INT.

Figure 46: Red Jumper on position INT



- Alternative: Power Connector J53 with 12 V and Power Connector J54 with 5 V, which delivers power separately to the board (12 V) and module. Jumper V_MOD must be on position EXT.

8.31. Button Switch

Figure 47: Button Switch

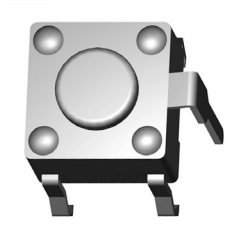


Table 19: Power Button (SW3, J26)

Pin	Signal
1	POWER_BTN#
2	POWER_BTN#
3	GND
4	GND
5	SHIELD

Table 20: Reset Button (SW1, J25)

Pin	Signal
1	RESET_IN#
2	RESET_IN#
3	GND
4	GND
5	SHIELD

Table 21: Force Recovery Button (SW4, J27)

Pin	Signal
1	FORCE_RECOV#
2	FORCE_RECOV#
3	GND
4	GND
5	SHIELD

8.32. Boot Selection Jumpers (J28, J32, J33) and other Jumpers

There are three Jumpers for Boot Select according to the SMARC 2.0 specification.

Figure 48: Jumpers for Boot Select

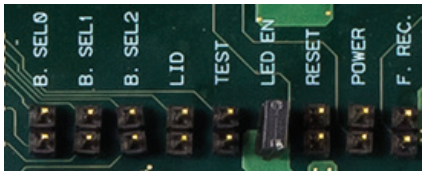


Table 22: Boot Selection Jumpers

	Carrier Connection			Boot Source
	BOOT_SEL2# (J33)	BOOT_SEL1# (J32)	BOOT_SEL0# (J28)	
1	GND	GND	GND	Carrier SATA
2	GND	GND	Float	Carrier SD Card
3	GND	Float	GND	Carrier eSPI (ESPI_CS0#)
4	GND	Float	Float	Carrier SPI (SPI0_CS0#)
5	Float	GND	GND	Module device (NAND, NOR) – vendor specific
6	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
7	Float	Float	GND	Module eMMC Flash

Boot options for the SMARC-sXAL (BOOT_SEL2#):

Only boot from module BIOS or carrier BIOS are supported, no other boot options are supported.

- To boot from module, remove shunt jumper on J33 (BOOT_SEL2#) of SMARC-Eval-Carrier-2.
- To boot from carrier, place shunt jumper on J33 (BOOT_SEL2#) of SMARC-Eval-Carrier-2.

Table 23: Display Power Select Jumper (J4)

Jumper Position	Function description
1-2	LVDS panel power (V_5V0_3V3_S0 pins 28-30) is 5.0V
2-3 (Default)	LVDS panel power (V_5V0_3V3_S0 pins 28-30) is 3.3V

Table 24: Backlight Power Select Jumper (J23)

Jumper Position	Function description
1-2	Backlight power (V_BKLT) is 5.0V
2-3 (Default)	Backlight power (V_BKLT) is 12V

Table 25: LID Jumper (J34)

Jumper Position	Function description
Open (Default)	LID Inactive
Close	LID Active

Table 26: TEST Jumper (J35)

Jumper Position	Function description
Open (Default)	TEST# not active
Close	TEST# active

Table 27: LEDs Enable Jumper (J44)

Jumper Position	Function description
Open (Default)	LEDs not active
Close	LEDs active

Table 28: RESET Jumper (J25)

Jumper Position	Function description
Open (Default)	Reset Signal Inactive
Close	Reset Signal Active

Table 29: Power Jumper (J26)

Jumper Position	Function description
Open (Default)	Power Signal Inactive
Close	Power Signal Active

Table 30: Force Recovery Jumper (J27)

Jumper Position	Function description
Open (Default)	Regular boot
Close	Force Recovery

Figure 49: Module Power Select Jumper (J55, J56, J57)

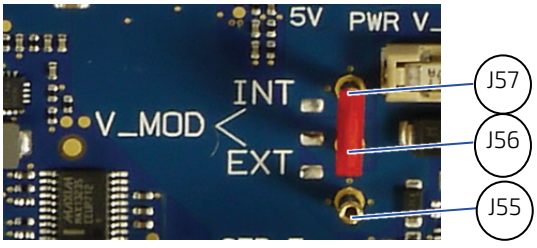


Table 31: Module Power Select Jumper (J55, J56, J57)

Jumper Position	Function description
J56 - J57 (Default)	SMARC module powered from carrier by 5 V power
J56 – J55	SMARC module powered from external connector J54

Table 32: Audio Channel Jumper for I2S or HDA (J31)

Jumper Position	Function description
Open (Default)	HDA Codec Active
Close	I2S Codec Active

NOTICE Jumper J31 should not be changed when power is present.

Table 33: mPCIe-1WLAN Disable Jumper (J49, J50)

Jumper Position	Function description
Open (Default)	WLAN in mPCIe slot J13 active
Close	WLAN in mPCIe slot J13 inactive

Table 34: mPCIe-1WLAN Disable Jumper (J51, J52)

Jumper Position	Function description
Open (Default)	WLAN in mPCIe slot J13 active
Close	WLAN in mPCIe slot J13 inactive

Figure 50: RTC Jumper (J58)

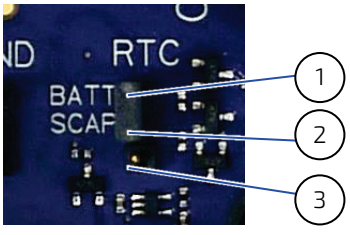


Table 35: RTC Jumper (J58)

Jumper Position	Function description
1-2 (Default)	Module RTC is powered from battery (J37)
2-3	Module RTC is powered from super cap (C364)

List of Acronyms

ATA	Advanced Technology Attachment
COM	Serial Communication Port
DP	DisplayPort
EC	Embedded Controller
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electro Static Discharge
Flash	Non-Volatile Memory
FPGA	Field Programmable Gate Array
Gold Flash Plating	Very thin gold plating (e.g. on contacts)
I/O	Input / Output
I2C	Inter IC bus (IIC or I2C)
JTAG	Joint Test Action Group, is a debug and programming port
LED	Light Emitting Diode
NC	Not connected
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer (IC)
PU	Pull-up
RS-232	Recommended Standard 232
RTC	Real Time Clock
SATA	Serial ATA
SMARC	Smart Mobility ARChitecture
SPI	Serial Peripheral Interface
SSD	Solid State Drive
TTL	Transistor-Transistor-Logic
UART	Universal Asynchronous Receiver and Transmitter
USB	Universal Serial Bus
VGA	Video Graphics Array: analog graphic output
VHDL	Very high speed integrated circuit Hardware Description Language
VRM	Voltage Regulator Module

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With a significant percentage of employees in research and development, Kontron creates many of the standards that drive the world's embedded computing platforms; bringing to life numerous technologies and applications that touch millions of lives. The result is an accelerated time-to-market, reduced total-cost-of-ownership, product longevity and the best possible overall application with leading-edge, highest reliability embedded technology.

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