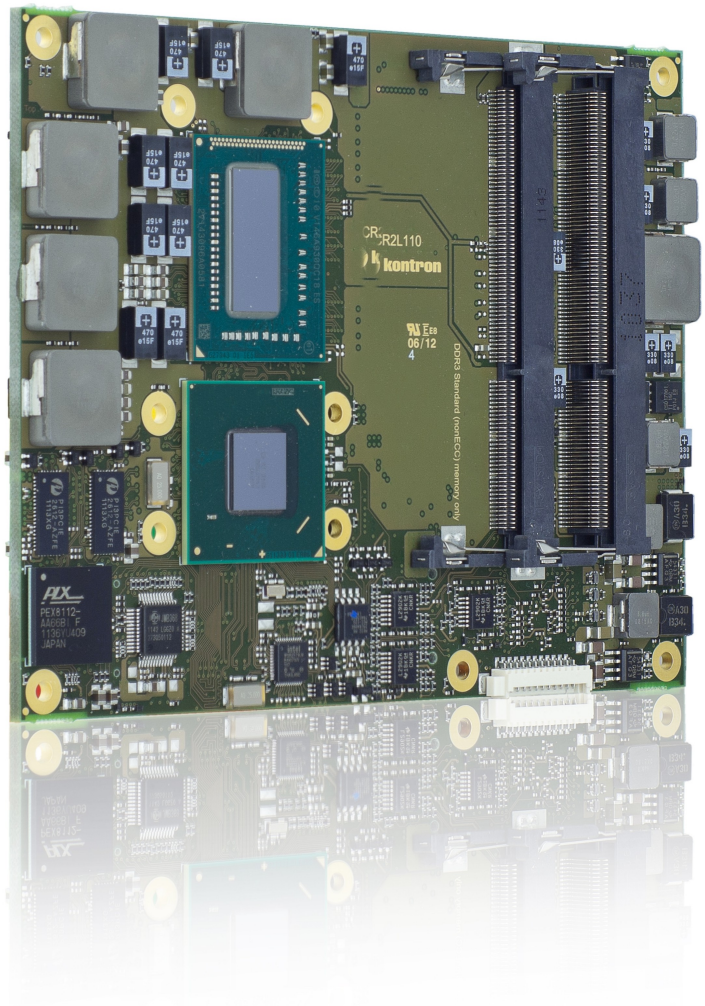
» Kontron User's Guide «



COMe-bIP2

Document Revision 140

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1 User Information

1.1 About This Document

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For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

1.3 Trademarks

The following lists the trademarks of components used in this board.

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1.4 Standards

Kontron Europe GmbH is certified to ISO 9000 standards.

1.5 Warranty

For this Kontron Europe GmbH product warranty for defects in material and workmanship exists as long as the warranty period, beginning with the date of shipment, lasts. During the warranty period, Kontron Europe GmbH will decide on its discretion if defective products are to be repaired or replaced.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

Warranty does not apply for defects arising/resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, as well as the operation outside of the product´s environmental specifications and improper installation and maintenance.

Kontron Europe GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Europe GmbH that are caused by a faulty Kontron Europe GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Europe GmbH and/or its subsidiaries are available for technical support. We are committed to make our product easy to use and will help you use our products in your systems.

Please consult our Website at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications, Board Support Packages, DemoImages, 3D drawings and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 Product Description

Kontron's Computer-on-Module for COM Express® basic with 3rd Generation of Intel® Core(TM) Series. With support for Pin-out Type 2 and Type 6, Kontron's module covers both the need for latest interface technology and the need to extend life-time for existing baseboard designs.

The 3rd Intel® Core Generation increases efficiency and performance per watt ratio which is a result of the innovative 22nm 3-D Tri-Gate.

With USB 3.0, SATA 6Gb/s and PCI Express Gen 3, COMe-bIP6 offers incredible data transfer. Additionally, note the outstanding visual computing performance with up to 3 independent displays and support for DirectX® 11 and OCL 1.1.

2.2 Naming clarification

COM Express® defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component.

» COMe-bXX# modules are Kontron's COM Express® modules in basic form factor (125mm x 95mm)

» COMe-cXX# modules are Kontron's COM Express® modules in compact form factor (95mm x 95mm)

» COMe-mXX# modules are Kontron's COM Express® modules in mini form factor (55mm x 84mm)

The product names for Kontron COM Express® Computer-on-Modules consist of a short form of the industry standard (**COMe-**), the form factor (**b**=basic, **c**=compact, **m**=mini), the capital letters for the CPU and Chipset Codenames (**XX**) and the pin-out type (**#**) followed by the CPU Name.

2.3 Understanding COM Express® Functionality

All Kontron COM Express® basic and compact modules contain two 220pin connectors; each of it has two rows called Row A & B on primary connector and Row C & D on secondary connector. COM Express® Computer-on-modules feature the following maximum amount of interfaces according to the PICMG module Pin-out type:

Feature	Pin-Out Type 1	Pin-Out Type 10	Pin-Out Type 2	Pin-Out Type 6
HD Audio	1x	1x	1x	1x
Gbit Ethernet	1x	1x	1x	1x
Serial ATA	4x	4x	4x	4x
Parallel ATA	-	-	1x	-
PCI	-	-	1x	-
PCI Express x1	6x	6x	6x	8x
PCI Express x16 (PEG)	-	-	1x	1x
USB Client	1x	1x	-	-
USB 2.0	8x	8x	8x	8x
USB 3.0	-	2x	-	4x
VGA	1x	-	1x	1x
LVDS	Dual Channel	Single Channel	Dual Channel	Dual Channel
DP++ (SDVO/DP/HDMI/DVI)	1x optional	1x	3x shared with PEG	3x
LPC	1x	1x	1x	1x
External SMB	1x	1x	1x	1x
External I2C	1x	1x	1x	1x
GPIO	8x	8x	8x	8x
SDIO shared w/GPIO	1x optional	1x optional	-	1x optional
UART (2-wire COM)	-	2x	-	2x
FAN PWM out	-	1x	-	1x

2.4 COM Express® Documentation

This product manual serves as one of three principal references for a COM Express® design. It documents the specifications and features of COMe-bIP2. Additional references are available at your Kontron Support or at PICMG®:

» The COM Express® Specification defines the COM Express® module form factor, pin-out, and signals. This document is available at the PICMG® website by filling out the order form.

» The COM Express® Design Guide by PICMG® serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules.

Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COM Express® Benefits

COM Express® modules are very compact, highly integrated computers. All Kontron COM Express® modules feature a standardized form factor and a standardized connector layout which carry a specified set of signals. Each COM is based on the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A single baseboard design can use a range of COM Express® modules with different sizes and pin-outs. This flexibility can differentiate products at various price/performance points, or when designing future proof systems that have a built-in upgrade path. The modularity of a COM Express® solution also ensures against obsolescence when computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

3 Product Specification

3.1 Module definition

The COM Express® basic sized Computer-on-Module COMe-bIP2 (CCR2) follows pin-out Type 2 and is compatible to PICMG specification COM.0 Rev 2.0. The COMe-bIP2 based on latest Chief River platform is available in different variants to cover the demand of different performance, price and power:

Commercial grade modules (0°C to 60°C operating)

Product Number	Product Name	Processor	PCH	Memory	Graphics	PEG	TPM
38020-0000-23-4	COMe-bIP2 i7-3615QE	Intel® Core™ i7-3615QE	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-21-4	COMe-bIP2 i7-3612QE	Intel® Core™ i7-3612QE	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-25-2	COMe-bIP2 i7-3555LE	Intel® Core™ i7-3555LE	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-17-2	COMe-bIP2 i7-3517UE	Intel® Core™ i7-3517UE	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-27-2	COMe-bIP2 i5-3610ME	Intel® Core™ i5-3610ME	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-24-2	COMe-bIP2 i3-3120ME	Intel® Core™ i3-3120ME	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-16-2	COMe-bIP2 i3-3217UE	Intel® Core™ i3-3217UE	QM77	2xDDR3-1600	HD4000	YES	Infineon SLB9635TT
38020-0000-22-1	COMe-bIP2 1020E	Intel® Celeron® 1020E	HM76	2xDDR3-1600	HD	YES	Infineon SLB9635TT
38020-0000-14-1	COMe-bIP2 1047UE	Intel® Celeron® 1047UE	HM76	2xDDR3-1600	HD	YES	Infineon SLB9635TT
38020-0000-15-0	COMe-bIP2 927UE	Intel® Celeron® 927UE	HM76	2xDDR3-1600	HD	YES	Infineon SLB9635TT

Extended temperature grade modules (E1, -25°C to 75°C operating)

Product Number	Product Name	Processor	PCH	Memory	Graphics	TPM
38020-0000-21-4EXT	COMe-bIP2 i7-3612QE E1	Intel® Core™ i7-3612QE	QM77	2xDDR3-1600	HD4000	-
38020-0000-25-2EXT	COMe-bIP2 i7-3555LE E1	Intel® Core™ i7-3555LE	QM77	2xDDR3-1600	HD4000	-

The COMe-bIP2 is available for extended temperature range. General capability was tested for following options:

» CPU: all

» Memory: E2 memory only 97015-xxxx-16-2

» TPM: Atmel AT97SC3204-U2A1A-10 optional

» VCC: 12V only, no support for Wide-Range Input

Industrial temperature grade modules (XT, -40°C to 85°C operating)

Modules for E2 temperature range are available project based only, please contact your local sales or support for further details.

Product Number	Product Name	Processor	PCH	TPM
38020-0000-CC-X	COMe-bIP2	All	QM77 or HM76	Atmel AT97SC3204

The COMe-bIP2 is available for industrial temperature range by screening. General capability was tested for following options:

» CPU: all

» Memory: E2 memory only 97015-xxxx-16-2

» TPM: Atmel AT97SC3204-U2A1A-10 optional

» VCC: 12V only, no support for Wide-Range Input

3.2 Functional Specification

Processor

The 22nm Intel® 3rd Gen Core™ i7/i5/i3/Celeron® embedded (Ivy Bridge) CPU family with 31x24mm package size (FCBGA1023 socket) supports:

- » Intel® Turbo Boost Technology 2.0
- » Intel® 64
- » Intel® Virtualization Technology (VT-x)
- » Intel® Virtualization Technology for Directed I/O (VT-d)
- » AES New Instructions (AES-NI)
- » Intel® Hyper-Threading Technology
- » Enhanced Intel SpeedStep® Technology
- » Idle States (C-States)
- » Intel® Smart Cache
- » Thermal Monitoring Technologies
- » Intel® Fast Memory Access
- » Intel® Flex Memory Access
- » Integrated Intel® HD Graphics with Dynamic Frequency
- » Configurable Thermal Design Power (cTDP)

Optional available (with customized BIOS):

- » Intel® vPRO™ Technology including:
- » Intel® Active Management Technology (AMT)
- » Intel® Trusted Execution Technology (TXT)

The integrated Intel® HD Graphics 4000 supports:

- » GraphicsTechnology GT1 with 6 Execution Units
- » GraphicsTechnology GT2 with 16 Execution Units
- » Intel® Quick Sync Video
- » Intel® InTru™ 3D Technology
- » Intel® Wireless Display
- » Intel® Flexible Display Interface (Intel® FDI)
- » Intel® Clear Video HD Technology
- » 3 simultaneous/independent displays in Windows 7 & Linux
- » Hybrid Multi Monitor
- » Video Decode for AVC/H.264/VC-1/MPEG-2
- » Video Encode for AVC/H.264/MPEG-2
- » Blu-ray Playback

The integrated Intel® HD2500 Graphics supports:

- » GraphicsTechnology GT1 with 6 Execution Units
- » Dual Display
- » Video Decode for AVC/H.264/VC-1/MPEG-2
- » Video Encode for AVC/H.264/MPEG-2
- » Blu-ray Playback

Intel®	Core™	Core™	Core™	Core™	Core™	Core™	Core™	Celeron®	Celeron®	Celeron®
-	i7-3615QE	i7-3612QE	i7-3555LE	i7-3517UE	i5-3610ME	i3-3120ME	i3-3217UE	1020E	1047UE	927UE
# of Cores	4	4	2	2	2	2	2	2	2	1
# of Threads	8	8	4	4	4	4	4	2	2	1
TDP Core frequency (HFM)	**2300MHz**	**2100MHz**	**2500MHz**	**1700MHz**	**2700MHz**	**2400MHz**	**1600MHz**	**2200MHz**	**1400MHz**	**1500MHz**
Max Turbo Frequency	3300MHz	3100MHz	3200MHz	2800MHz	3300MHz	-	-	-	-	-
LFM/LPM Frequency	1200MHz	1200MHz	800MHz	800MHz	800MHz	800MHz	800MHz	1200MHz	800MHz	800MHz
Bus/Core Ratio	12-23	12-21	8-25	8-17	8-27	8-24	8-16	12-22	8-14	8-15
Nominal TDP	45W	35W	25W	17W	35W	35W	17W	35W	17W	17W
Power Limit 2 (PL2 max)	60W	44W	44W	24W	44W	-	-	-	-	-
cTDP-Down	-	-	-	14W (800MHz)	-	-	14W (800MHz)	-	-	-
cTDP-Up	-	-	-	25W (2.2GHz)	-	-	17W (1.6GHz)	-	-	-
Lithography	22nm	22nm	22nm	22nm	22nm	22nm	22nm	22nm	22nm	22nm
C-States	C0-C6	C0-C6	C0-C6	C0-C6	C0-C6	C0-C6	C0-C6	C0-C3	C0-C3	C0-C3
Smart Cache	6MB	6MB	4MB	4MB	3MB	3MB	3MB	2MB	2MB	1MB
Min Memory Type	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066	DDR3-1066
Max Memory Type	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600	DDR3-1600
Max Memory Size	16GB	16GB	16GB	16GB	16GB	16GB	16GB	16GB	16GB	16GB
# of Memory Channels	2	2	2	2	2	2	2	2	2	2
Graphics Model	HD4000	HD4000	HD4000	HD4000	HD4000	HD4000	HD4000	HD	HD	HD
GFX Base Frequency	650MHz	650MHz	550MHz	350MHz	650MHz	650MHz	350MHz	650MHz	350MHz	350MHz
GFX Max Dynamic Frequ.	1000MHz	1000MHz	1000MHz	1000MHz	1100MHz	900MHz	900MHz	1000MHz	900MHz	900MHz
GFX Technology	GT2 16EU	GT2 16EU	GT2 16EU	GT2 16EU	GT2 16EU	GT2 16EU	GT2 16EU	GT1 6EU	GT1 6EU	GT1 6EU
Quick Sync Video	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	-	-
InTru™ 3D	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	-	-
Wireless Display	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	-	-
Clear Video HD	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	-	-
vPRO™ (optional)	Yes	Yes	Yes	Yes	Yes	-	-	-	-	-
TXT (optional)	Yes	Yes	Yes	Yes	Yes	-	-	-	-	-
AES-NI	Yes	Yes	Yes	Yes	Yes	-	-	-	-	-
VT-x	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VT-d	Yes	Yes	Yes	Yes	Yes	-	-	-	-	-
PCI Express Graphics	Gen 3.0	Gen 3.0	Gen 3.0	Gen 3.0	Gen 3.0	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0	Gen 2.0

- The Driver Default PL2 is 1.25 x cTDP
- Due to onboard PCIe switches to share PEG and DDI the PEG interface on COM Express® only allows up to Gen 2.0 speed even if the CPU supports Gen 3.0

Memory

Sockets	2x DDR3 SO-DIMM
Memory Type	DDR3-1333/1600
Maximum Size	2x8GB
Technology	Dual Channel

Chipset

The 65nm Intel® 7-Series Platform Controller Hub Panther Point supports:

» PCI Express Revision 2.0

» PCI Express Configurations x1, x2, x4

» Intel® Virtualization Technology for Directed I/O (VT-d)

» Intel® Trusted Execution Technology (TXT)

» Intel® vPro Technology (optional)

» Intel® Active Management Technology 8.0 (optional)

» Intel® Anti-Theft Technology

» Intel® Rapid Storage Technology

» Intel® Smart Response Technology

PCH comparison

Feature	QM77	HM76
TDP	4.1W	4.1W
Rapid Storage	YES	YES
USB 3.0	YES	YES
Wireless Display	YES	YES
3 Displays	YES	YES
VT-d	YES	NO
vPRO	YES	NO
AMT 8.0	YES	NO
TXT	YES	NO
SATA RAID	YES	NO

The Intel® vPro Technology including Trusted Execution Technology (TXT) and Active Management Technology (AMT) is not supported by default on COMe-bIP2. Please contact your local sales or support for custom BIOS variants supporting vPro.

Graphics Core

The integrated Intel® GMA HD4000 (Gen7) supports:

Graphics Core Render Clock	GT1 /GT2; Base clock: 350/650 MHz; GT Turbo: up to 1000 MHz
Execution Units / Pixel Pipelines	GT2: 16EU / GT1: 6EU
Max Graphics Memory	1720MB
GFX Memory Bandwidth (GB/s)	17.1
GFX Memory Technology	DVMT
API (DirectX/OpenGL)	11 / 3.0 + OCL1.1
Shader Model	5.0
Hardware accelerated Video	MPEG2, VC-1, AVC, Blu-ray (+3D)
Independent/Simultaneous Displays	3
Display Port	DP 1.1a / eDP
HDCP support	HDCP 1.4

Monitor output

CRT max Resolution	2048x1536
TV out:	-

LVDS

LVDS Bits/Pixel	1x18/24, 2x18/24
LVDS Bits/Pixel with dithering	-
LVDS max Resolution:	1920x1200
PWM Backlight Control:	YES
Supported Panel Data:	JILI2/JILI3/EDID/DID

Display Interfaces

Discrete Graphics	1x PEG 2.0
Digital Display Interface DDI1	DP++/SDVOB
Digital Display Interface DDI2	DP++
Digital Display Interface DDI3	DP++/eDP
Maximum Resolution on DDI	2560x1600

PEG Configuration

The x16 PCI Express Graphics Port (PEG) is compatible to standard PCI Express devices like Ethernet or RAID controllers. The COMe-bIP2 supports following PEG Port configuration when used as PCI Express Interface:

» 1×16

» 1×8

» 1×4

» 1×2

» 1×1

The internal PCI Express controller can be re-configured to support up to 3 PCIe ports. The following port configurations are available via hardware strap options (customized article):

» 2×8 (lanes #0-7 + #8-15)

» 1×8 + 2×4 (lanes #0-7 + #8-11 + #12-15)

Storage

onboard SSD	-
SD Card support	-
IDE Interface	JMB368 PCIe2PATA
Serial-ATA	2x SATA 6Gb/s, 2x SATA 3Gb/s
SATA AHCI	NCQ, HotPlug, Staggered Spinup, eSATA, PortMultiplier
SATA RAID	0, 1, 5, 10, MATRIX (QM77 only)

If SATA AHCI or RAID is disabled in setup, the SATA Interface only supports 3Gb/s transfer rate and Staggered Spin-Up. To configure a RAID enable RAID support in BIOS Chipset/SATA settings, connect at least two hard drives and enter the RAID Option ROM by pressing 'CTRL'+'I'

Connectivity

USB 2.0	8x USB 2.0
USB 3.0	-
USB Client	-
PCI	PEX8112 PCIe2PCI
PCI External Masters	4
PCI Express	5x PCIe x1 Gen2
Max PCI Express	6x PCIe without PCIe2PATA Bridge
PCI Express x2/x4 configuration	YES (Softstrap option)
Ethernet	10/100/1000 Mbit
Ethernet controller	Intel® 82579LM (Lewisville)

Due to internal chipset configuration the Panther Point only supports up to 4 USB Hubs

PCI Express Configuration

The COMe-bIP2 only supports x1 PCIexpress lane configuration by default. Following x2/x4 configurations are possible via Management Engine Softstrap Options:

PCIe	Port #0	Port #1	Port #2	Port #3	Port #4	Port #5*	Port #6*	Port #7*
Configuration0	x1	x1	x1	x1	x1	x1	x1	x1
Configuration1	x2		x1	x1	x1	x1	x1	x1
Configuration2	x2		x2		x1	x1	x1	x1
Configuration3	x2		x2		x2		x1	x1
Configuration4	x2		x2		x2		x2	
Configuration5	x4				x1	x1	x1	x1
Configuration6	x4				x2		x1	x1
Configuration7	x4				x2		x2	
Configuration8	x4				x4			

- *PCIe Ports #5 to #7 are only available without PCIe2PATA Bridge, PCIe2PCI Bridge and without Ethernet Controller
- Configuration0 (default) and Configuration5 (modified FlashDescriptor) are provided in BIOS download package available on EMD Customer Section

Ethernet

The Intel® 82579LM (Lewisville) ethernet supports:

» Jumbo Frames

» MACsec IEEE 802.1 AE

» Time Sync Protocol Indicator

» WOL (Wake On LAN)

» PXE (Preboot eXecution Environment)

Misc Interfaces and Features

Supported BIOS Size/Type	8MB SPI
Audio	HD Audio + DisplayPort dual stream
Onboard Hardware Monitor	Nuvoton NCT7802Y
Trusted Platform Module	Infineon TPM 1.2 SLB9635TT
Miscellaneous	-

Kontron Features

External I2C Bus	Fast I2C, MultiMaster capable
M.A.R.S. support	YES
Embedded API	KEAPI1 / KEAPI2
Custom BIOS Settings / Flash Backup	YES
Watchdog support	Dual Staged

Additional features

» All solid capacitors (POSCAP). No tantalum capacitors used.

» Optimized RTC Battery monitoring to secure highest longevity

» Real fast I2C with transfer rates up to 40kB/s.

» Discharge logic on all onboard voltages for highest reliability

Power Features

Singly Supply Support	YES
Supply Voltage	8.5V - 20V
ACPI	ACPI 4.0
S-States	S0, S3, S4, S5
S5 Eco Mode	YES
Misc Power Management	cTDP @ 17W i3/i7

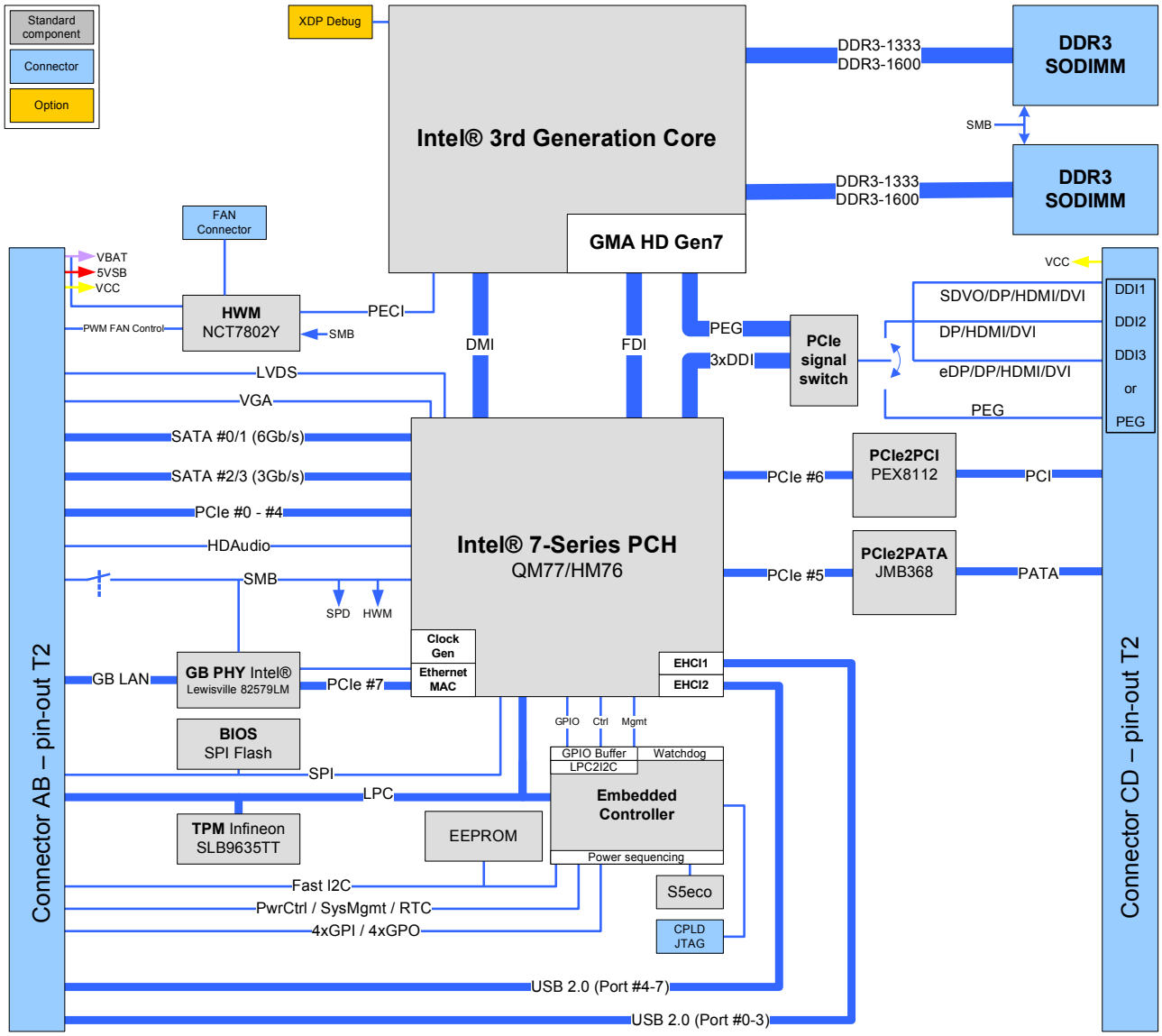
Power Consumption and Performance

Full Load Power Consumption	10 - 58W
Kontron Performance Index	18289 - 76117
Kontron Performance/Watt	1319 - 2740

*Measured Values. Please note the maximum Power Consumption with activated Turbo Mode in chapter Turbo 2.0

Detailed Power Consumption measurements in all states and benchmarks for CPU, Graphics and Memory performance are available in Application Note KEMAP054 at EMD Customer Section.

3.3 Block Diagram



3.4 Accessories

Product specific accessories

Product Number	Heatspreader and Cooling Solutions	Comment
38013-0000-99-0	HSP COMe-bSC/IP thread	For CPUs up to 25W TDP and commercial temperature grade usage
38013-0000-99-1	HSP COMe-bSC/IP through	For CPUs up to 25W TDP and commercial temperature grade usage
38013-0000-99-2	HSP COMe-bSC/IP heatpipe thread	For all CPUs and temperature grades
38013-0000-99-3	HSP COMe-bSC/IP heatpipe through	For all CPUs and temperature grades
38013-0000-99-0C05	HSK COMe-bSC/IP active setscrew thread	For all CPUs and commercial temperature grade usage
38013-0000-99-1C05	HSK COMe-bSC/IP active setscrew through hole	For all CPUs and commercial temperature grade usage
38013-0000-99-0C06	HSK COMe-bSC/IP passive setscrew thread	For all CPUs and commercial temperature grade usage
38013-0000-99-1C06	HSK COMe-bSC/IP passive setscrew through hole	For all CPUs and commercial temperature grade usage

General accessories

Part Number	COMe pin-out Type 2 compatible accessories	Project Code	Comment
38102-0000-00-1	COM Express® Reference Carrier Type 2	ADAE	mITX Carrier with 8mm COMe connector
38104-0000-00-0	COM Express® Eval Carrier Type 2	Niles Canyon	ATX Carrier with 5mm COMe connector (EOL)
38104-0000-00-1	COM Express® Eval Carrier Type 2	Topanga Canyon	ATX Carrier with 5mm COMe connector
96006-0000-00-7	ADA-Type2-DP3	DVOD	(sandwich) Adapter Card for 3x DisplayPort
38019-0000-00-0	ADA-COMe-Height-dual	EERC	Height Adapter
36100-0000-00-S	COMe Ref. Starterkit T2	ADAE	Starterkit with COMe Reference Carrier T2
Part Number	**Mounting**	**Comment**	
38017-0000-00-5	COMe Mount KIT 5mm 1set	Mounting Kit for 1 module including screws for 5mm connectors	
38017-0100-00-5	COMe Mount KIT 5mm 100sets	Mounting Kit for 100 modules including screws for 5mm connectors	
38017-0000-00-0	COMe Mount KIT 8mm 1set	Mounting Kit for 1 module including screws for 8mm connectors	
38017-0100-00-0	COMe Mount Kit 8mm 100sets	Mounting Kit for 100 modules including screws for 8mm connectors	
Part Number	**Display Adapter**	**Comment**	
9-5000-0352	ADA-LVDS-DVI 18bit	LVDS to DVI converter	
9-5000-0353	ADA-LVDS-DVI 24bit	LVDS to DVI converter	
96006-0000-00-8	ADA-DP-LVDS	DP to LVDS adapter	
96082-0000-00-0	KAB-ADAPT-DP-DVI	DP to DVI adapter cable	
96083-0000-00-0	KAB-ADAPT-DP-VGA	DP to VGA adapter cable	
96084-0000-00-0	KAB-ADAPT-DP-HDMI	DP to HDMI adapter cable	
Part Number	**Cables**	**Comment**	
96079-0000-00-0	KAB-HSP 200mm	Cable adapter to connect FAN to module (COMe basic/compact)	
96079-0000-00-2	KAB-HSP 40mm	Cable adapter to connect FAN to module (COMe basic/compact)	
Part Number	**Miscellaneous**	**Comment**	
18029-0000-00-0	MARS Smart Battery Kit	Starterkit Kontron Mobile Application platform for Rechargeable Systems	
Part Number	**DDR3 SODIMM, commercial temperature grade**		
97015-1024-16-0	DDR3-1600 SODIMM 1GB		
97015-2048-16-0	DDR3-1600 SODIMM 2GB		
97015-4096-16-0	DDR3-1600 SODIMM 4GB		
97015-8192-16-0	DDR3-1600 SODIMM 8GB		
Part Number	**DDR3 SODIMM, industrial temperature grade**		
97015-1024-16-2	DDR3-1600 SODIMM 1GB E2		
97015-2048-16-2	DDR3-1600 SODIMM 2GB E2		
97015-4096-16-2	DDR3-1600 SODIMM 4GB E2		
97015-8192-16-2	DDR3-1600 SODIMM 8GB E2		

3.5 Electrical Specification

3.5.1 Supply Voltage

Following supply voltage is specified at the COM Express® connector:

VCC:	8.5V - 20V
Standby:	5V DC +/- 5%
RTC:	2.5V - 3.47V

- 5V Standby voltage is not mandatory for operation.
- Extended Temperature (E1) variants are validated for 12V supply only

3.5.2 Power Supply Rise Time

» The input voltages shall rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

3.5.3 Supply Voltage Ripple

» Maximum 100 mV peak to peak 0 – 20 MHz

3.5.4 Power Consumption

The maximum Power Consumption of the different COMe-bIP2 variants is 10 - 58W (100% CPU load on all cores; 90°C CPU temperature). Further information with detailed measurements are available in Application Note KEMAP054 available on EMD Customer Section. Information there is available after registration.

3.5.5 ATX Mode

By connecting an ATX power supply with VCC and 5VSB, PWR_OK is set to low level and VCC is off. Press the Power Button to enable the ATX PSU setting PWR_OK to high level and powering on VCC. The ATX PSU is controlled by the PS_ON# signal which is generated by SUS_S3# via inversion. VCC can be 8.5V - 20V in ATX Mode. On Computer-on-Modules supporting a wide range input down to 4.75V the input voltage shall always be higher than 5V Standby (VCC > 5VSB).

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 → S0	PWRBTN Event	low → high	5V	high → low	0 V→ VCC
S0	high	high	5V	low	VCC

3.5.6 Single Supply Mode

In single supply mode (or automatic power on after power loss) without 5V Standby the module will start automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3V). PS_ON# is not used in this mode and VCC can be 8.5V - 20V.

To power on the module from S5 state press the power button or reconnect VCC. Suspend/Standby States are not supported in Single Supply Mode.

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	x	x	x	0
G3 → S0	high	open / high	x	connecting VCC
S5	high	open / high	x	VCC
S5 → S0	PWRBTN Event	open / high	x	reconnecting VCC

Signals marked with “x” are not important for the specific power state. There is no difference if connected or open.

All ground pins have to be tied to the ground plane of the carrier board.

3.6 Power Control

Power Supply

The COMe-bIP2 supports a power input from 8.5V - 20V. The supply voltage is applied through the VCC pins (VCC) of the module connector.

Power Button (PWRBTN#)

The power button (Pin B12) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4s, typical 400ms) at low level (Power Button Event).

Pressing the power button for at least 4seconds will turn off power to the module (Power Button Override).

Power Good (PWR_OK)

The COMe-bIP2 provides an external input for a power-good signal (Pin B24). The implementation of this subsystem complies with the COM Express® Specification. PWR_OK is internally pulled up to 3.3V and must be high level to power on the module.

Reset Button (SYS_RESET#)

The reset button (Pin B49) is available through the module connector described in the pinout list. The module will stay in reset as long as SYS_RESET# is grounded. If available, the BIOS setting for “Reset Behavior” must be set to “Power Cycle”.

Modules with Intel® Chipset and active Management Engine do not allow to hold the module in Reset out of S0 for a long time. At about 10s holding the reset button the ME will reboot the module automatically

SM-Bus Alert (SMB_ALERT#)

With an external battery manager present and SMB_ALERT# (Pin B15) connected the module always powers on even if BIOS switch “After Power Fail” is set to “Stay Off”.

3.7 Environmental Specification

3.7.1 Temperature Specification

Kontron defines following temperature grades for Computer-on-Modules in general. Please see chapter 'Product Specification' for available temperature grades for the COMe-bIP2

Temperature Specification	Operating	Non-operating	Validated Input Voltage
Commercial grade	0°C to +60°C	-30°C to +85°C	VCC: 8.5V - 20V
Extended Temperature (E1)	-25°C to +75°C	-30°C to +85°C	VCC: 12V
Industrial grade by **Screening** (XT)	-40°C to +85°C	-40°C to +85°C	VCC: 12V
Industrial grade by **Design** (E2)	-40°C to +85°C	-40°C to +85°C	VCC: 8.5V - 20V

Operating with Kontron heatspreader plate assembly

The operating temperature defines two requirements:

» the maximum ambient temperature with ambient being the air surrounding the module.

» the maximum measurable temperature on any spot on the heatspreader's surface

Test specification:

Temperature Grade	Validation requirements
Commercial grade	at 60°C HSP temperature the CPU @ 100% load needs to run at nominal frequency
Extended Temperature (E1)	at 75°C HSP temperature the CPU @ 75% load is allowed to start speedstepping for thermal protection
Industrial grade by **Screening** (XT)	at 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection
Industrial grade by **Design** (E2)	at 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection

Operating without Kontron heatspreader plate assembly

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

3.7.2 Humidity

» 93% relative Humidity at 40°C, non-condensing (according to IEC 60068-2-78)

3.8 Standards and Certifications

RoHS II

The **COMe-bIP2** is compliant to the directive 2011/65/EU on the Restriction of the use of certain Hazardous Substances (RoHS II) in electrical and electronic equipment

Component Recognition UL 60950-1

The **COM Express® basic** form factor Computer-on-Modules are Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements.

UL Listings:

» NWGQ2.E304278

» NWGQ8.E304278

WEEE Directive

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

Conformal Coating

Conformal Coating is available for Kontron Computer-on-Modules and for validated SO-DIMM memory modules. Please contact your local sales or support for further details.

Shock & Vibration

The **COM Express® basic** form factor Computer-on-Modules successfully passed shock and vibration tests according to

» IEC/EN 60068-2-6 (Non operating Vibration, sinusoidal, 10Hz-4000Hz, +/-0.15mm, 2g)

» IEC/EN 60068-2-27 (Non operating Shock Test, half-sinusoidal, 11ms, 15g)

EMC

Validated in Kontron reference housing for EMC the **COMe-bIP2** follows the requirements for electromagnetic compatibility standards

» EN55022

3.9 MTBF

The following MTBF (Mean Time Before Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The calculation method used is "Telcordia Issue 2 Method 1 Case 3" in a ground benign, controlled environment (GB,GC). This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned in.

Other environmental stresses (extreme altitude, vibration, salt water exposure, etc) lower MTBF values.

System MTBF (hours): 205482 @ 40°C (w/PCB)

Fans usually shipped with Kontron Europe GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

3.10 Mechanical Specification

Dimension

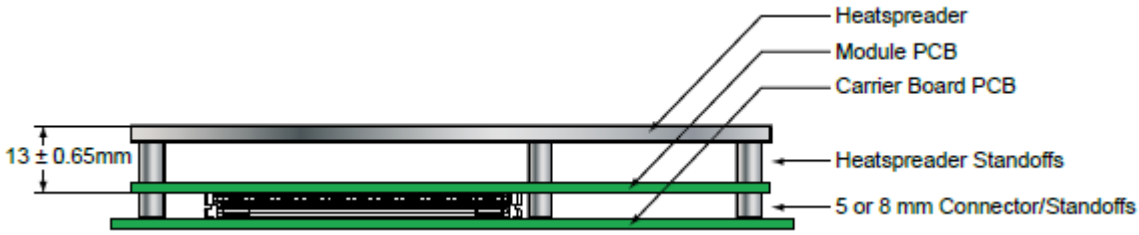
» 95.0 mm x 125.0 mm

» Height approx. 12mm (0.4”)

CAD drawings are available at EMD CustomerSection

Height

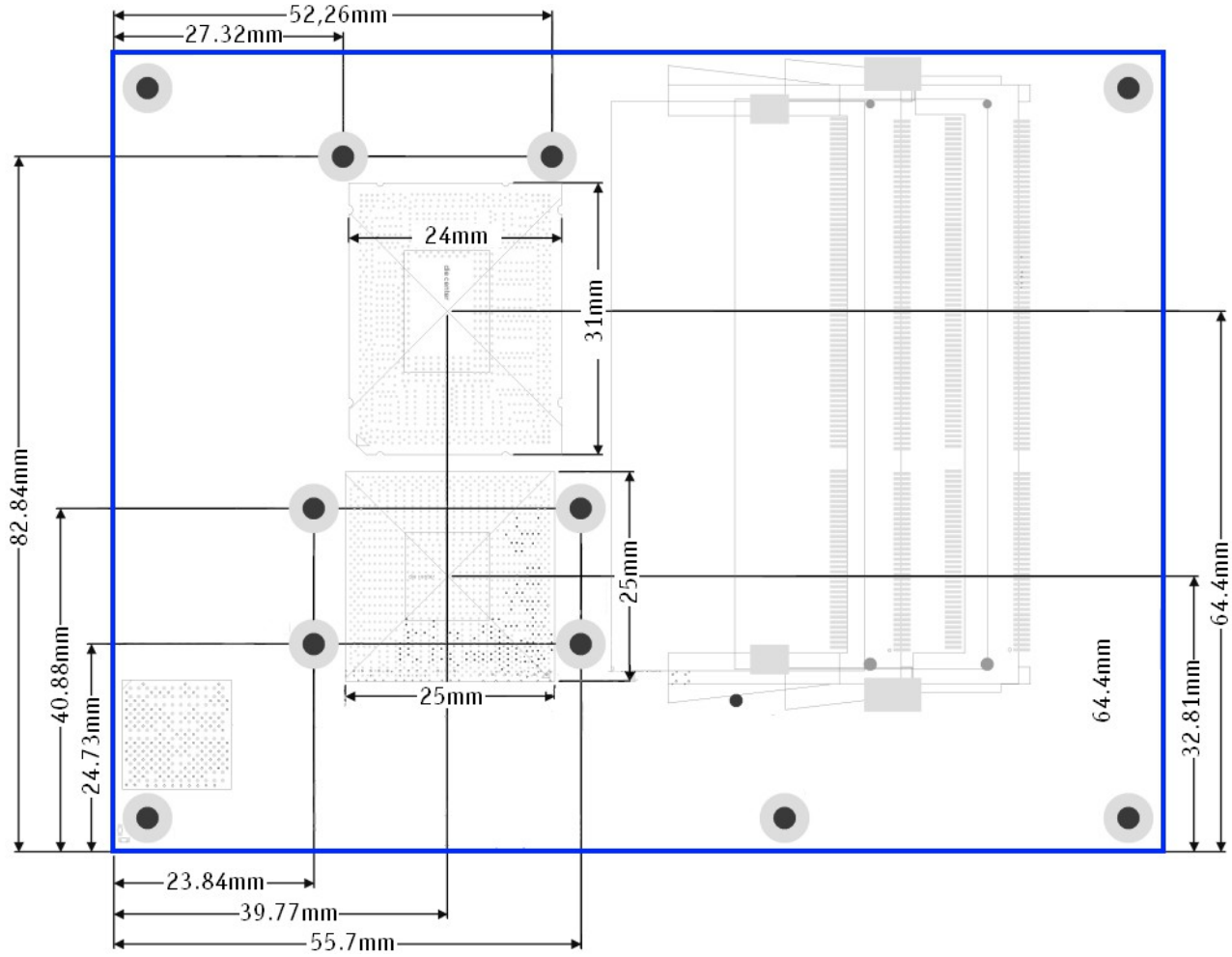
The COM Express® specification defines a module height of 13mm from module PCB bottom to heatspreader top:



Cooling solutions provided from Kontron Europe GmbH for basic sized Computer-on-Modules are 27mm in height from module bottom to Heatsink top.

Universal Cooling solutions to be mounted on the HSP (36099-0000-00-x) are 14.3mm in height for an overall height of 27.3mm from module bottom to Heatsink top.

3.11 Module Dimensions



3.12 Thermal Management, Heatspreader and Cooling Solutions

A heatspreader plate assembly is available from Kontron Europe GmbH for the COMe-bIP2. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express®-standard thermal interface to use with a heat sink or external cooling devices.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any spot of the heatspreader's surface according the module specifications:

- 60°C for commercial grade modules
- 75°C for extended temperature grade modules (E1)
- 85°C for industrial temperature grade modules (E2/XT)

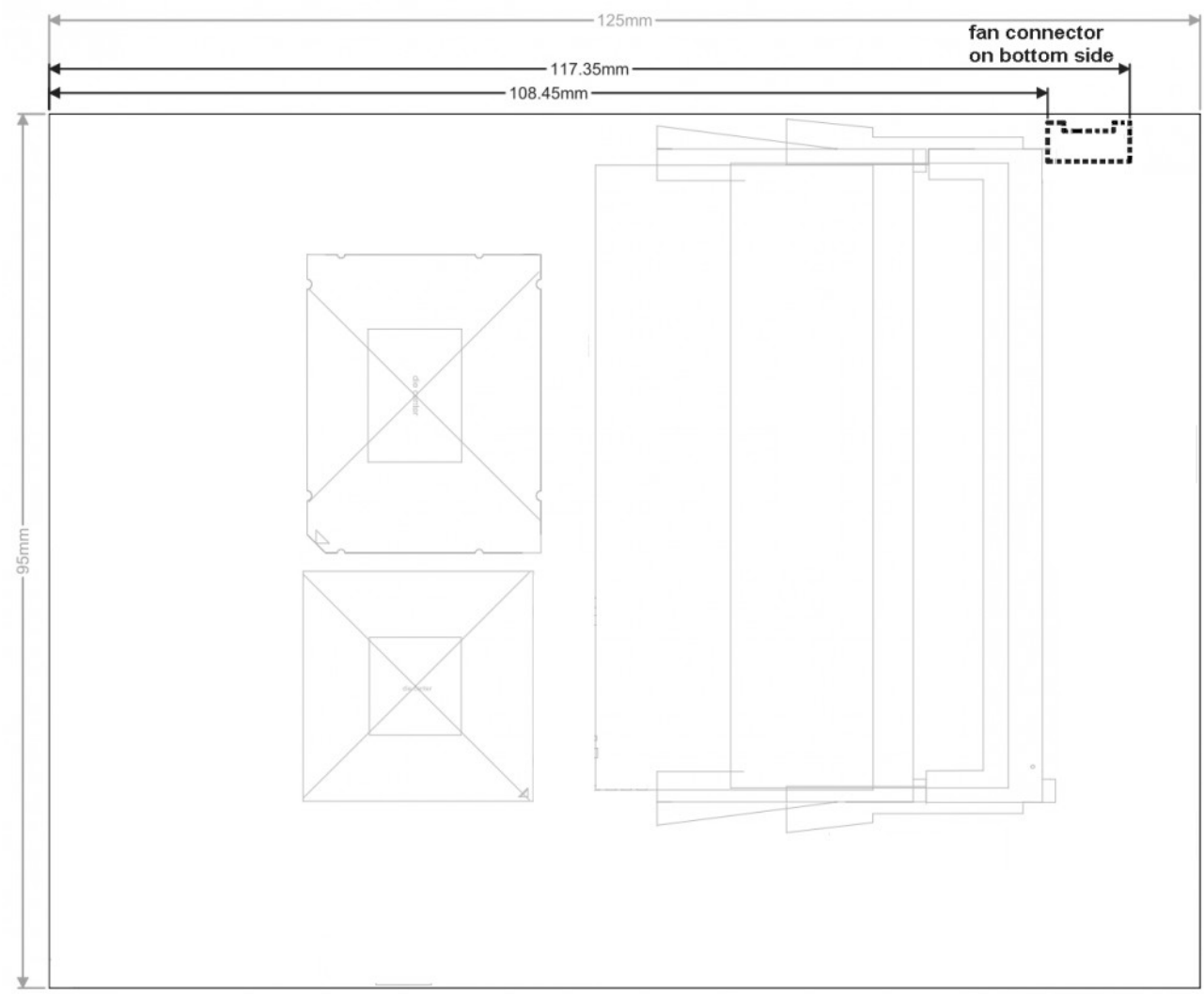
The aluminum slugs and thermal pads or the heat-pipe on the underside of the heatspreader assembly implement thermal interfaces between the heatspreader plate and the major heat-generating components on the COMe-bIP2. About 80 percent of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution.

You can use many thermal-management solutions with the heatspreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Active or passive cooling solutions provided from Kontron Europe GmbH for the COMe-bIP2 are usually designed to cover the power and thermal dissipation for a commercial grade temperature range used in a housing with proper air flow.

Documentation and CAD drawings of COMe-bIP2 heatspreader and cooling solutions are provided at http://emdcustomersection.kontron.com.

3.13 Onboard Fan Connector

Location of the FAN Connector



Specification of the FAN Connector:

» Part number (Molex) J8: 53261-0371, Mates with: 51021-0300, Crimp terminals: 50079-8100

Pin assignment

» Pin1: Tacho, Pin2: VCC, Pin3: GND

Electrical characteristic

Module Input Voltage	8.5 - 13V	>13V
FAN Output Voltage	8.5 - 13V	13V
Max. FAN Output Current	350mA	150mA

To connect a standard FAN with 3pin connector to the module please use adaptor cable KAB-HSP 200mm (96079-0000-00-0) or KAB-HSP 40mm (96079-0000-00-2)

Please check the FAN specifications when using the onboard FAN connector at input voltages above 13V according the output current limitation

4 Features and Interfaces

4.1 S5 Eco Mode

Kontron's new high-efficient power-off state S5 Eco enables lowest power-consumption in soft-off state – less than 1 mA compared to the regular S5 state this means a reduction by at least factor 200!

In the "normal" S5 mode the board is supplied by 5V_Stb and needs usually up to 300mA just to stay off. This mode allows to be switched on by power button, RTC event and WakeOnLan, even when it is not necessary. The new S5 Eco mode reduces the current enormous.

The S5 Eco Mode can be enabled in BIOS Setup, when the BIOS supports this feature.

Following prerequisites and consequences occur when S5 Eco Mode is enabled

» The power button must be pressed at least for 200ms to switch on.

» Wake via Power button only.

» "Power On After Power Fail"/"State after G3": only "stay off" is possible

4.2 LPC

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus bridge located in the CPU or chipset. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide maintained by PICMG. Please refer to the official PICMG documentation for additional information.

The LPC bus does not support DMA (Direct Memory Access) and a clock buffer is required when more than one device is used on LPC. This leads to limitations for ISA bus and SIO (standard I/O´s like Floppy or LPT interfaces) implementations.

All Kontron COM Express® Computer-on-Modules imply BIOS support for following external baseboard LPC Super I/O controller features for the **Winbond/Nuvoton 5V 83627HF/G and 3.3V 83627DHG-P**:

83627HF/G	Phoenix BIOS	AMI CORE8	AMI / Phoenix EFI
PS/2	YES	YES	YES
COM1/COM2	YES	YES	YES
LPT	YES	YES	YES
HWM	YES	YES	NO
Floppy	NO	NO	NO
GPIO	NO	NO	NO
83627DHG-P	**Phoenix BIOS**	**AMI CORE8**	**AMI / Phoenix EFI**
PS/2	YES	YES	YES
COM1/COM2	YES	YES	YES
LPT	YES	YES	YES
HWM	NO	NO	NO
Floppy	NO	NO	NO
GPIO	NO	NO	NO

Features marked as not supported do not exclude OS support (e.g. HWM can be accessed via SMB). For any other LPC Super I/O additional BIOS implementations are necessary. Please contact your local sales or support for further details.

4.3 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. Sometimes SPI is called a “four wire” serial bus, contrasting with three, two, and one wire serial buses.

The SPI interface can only be used with a SPI flash device to boot from external BIOS on the baseboard.

4.4 SPI boot

The COMe-bIP2 supports boot from an external SPI Flash. It can be configured by pin A34 (BIOS_DIS#0) and pin B88 (BIOS_DIS1#) in following configuration:

BIOS_DIS0#	BIOS_DIS1#	Function
open	open	Boot on-module BIOS
GND	open	Boot baseboard LPC FWH
open	GND	Baseboard SPI = Boot Device 1, on-module SPI = Boot Device 2
GND	GND	Baseboard SPI = Boot Device 2, on-module SPI = Boot Device 1

By default only SPI Boot Device 1 is used in configuration 3 & 4. Both SPI Boot Devices are used by splitting the BIOS with modified descriptor table in customized versions only

Recommended SPI boot flash types for 8-SOIC package

Size	Manufacturer	Part Number	Device ID
16Mbit	Atmel	AT26DF161	0x1F4600
16Mbit	Atmel	AT26DF161A	0x1F4601
16Mbit	Atmel	AT25DF161	0x1F4602
16Mbit	Atmel	AT25DQ161	0x1F8600
16Mbit	Macronix	MX25L1605A(D)(36E)(06E)	0xC22015
16Mbit	Macronix	MX25L1635D	0xC22415
16Mbit	SST/Microchip	SST25VF016B	0xBF2541
16Mbit	Winbond	W25X16BV	0xEF3015
16Mbit	Winbond	W25Q16BV(CV)	0xEF4015
Size	**Manufacturer**	**Part Number**	**Device ID**
32Mbit	Atmel	AT25/26DF321	0x1F4700
32Mbit	Atmel	AT25DF321A	0x1F4701
32Mbit	Macronix	MX25L3205A(D)(06E)	0xC22016
32Mbit	Macronix	MX25L3225D(35D)(36D)	0xC25E16
32Mbit	SST/Microchip	SST25VF032B	0XBF254A
32Mbit	Winbond	W25X32BV	0xEF3016
32Mbit	Winbond	W25Q32BV,	0xEF4016
Size	**Manufacturer**	**Part Number**	**Device ID**
64Mbit	Atmel	AT25DF641(A)	0x1F4800
64Mbit	Atmel	AT25DQ641	0x1F8800
64Mbit	Macronix	MX25L6405D(45E)(36E)(06E)(73E)	0xC22017
64Mbit	Macronix	MX25L6455E	0xC22617
64Mbit	Macronix	MX25U6435F	0xC22537
64Mbit	SST/Microchip	SST25VF064C	0xBF254B
64Mbit	Winbond	W25X64BV	0xEF3017
64Mbit	Winbond	W25Q64BV(CV)(FV)	0xEF4017
64Mbit	Winbond	W25Q64DW	0XEF6017
64Mbit	Winbond	W25Q64FW	0XEF6017

Using an external SPI flash

To program an external SPI flash follow these steps:

» Connect a SPI flash with correct size (similar to BIOS ROM file size) to the module SPI interface

» Open pin A34 and B88 to boot from the module BIOS

» Boot the module to DOS/EFI-Shell with access to the BIOS image and Firmware Update Utility provided on EMD Customer Section

» Connect pin B88 (BIOS_DIS1#) to ground to enable the external SPI flash

» Execute Flash.bat/Flash.efi to program the complete BIOS image to the external SPI flash

» reboot

Your module will now boot from the external SPI flash when BIOS_DIS1# is grounded.

External SPI flash on Modules with Intel® ME

If booting from the external (baseboard mounted) SPI flash then exchanging the COM Express® module for another one of the same type will cause the Intel® Management Engine to fail during next start. This is by design of the ME because it bounds itself to the very module it has been flashed to. In the case of an external SPI flash this is the module present at flash time.

To avoid this issue please make sure to conduct a complete flash of the external SPI flash device after changing the COMexpress module for another one. If disconnecting and reconnecting the same module again this step is not necessary.

4.5 M.A.R.S.

The Smart Battery implementation for Kontron Computer-on-Modules called **M**obile **A**pplication for **R**echargeable **S**ystems is a BIOS extension for external Smart Battery Manager or Charger. It includes support for SMBus charger/selector (e.g. Linear Technology LTC1760 Dual Smart Battery System Manager) and provides ACPI compatibility to report battery information to the Operating System.

Reserved SM-Bus addresses for Smart Battery Solutions on the carrier:

8-bit Address	7-bit Address	Device
12h	0x09	SMART_CHARGER
14h	0x0A	SMART_SELECTOR
16h	0x0B	SMART_BATTERY

4.6 Fast I2C

The COMe-bIP2 supports a CPLD implemented LPC to I2C bridge using the WISHBONE I2C Master Core provided from opencores.org. The I2C Interface supports transfer rates up to 40kB/s and can be configured in Setup

Specification for external I2C:

» Speed up to 400kHz

» Compatible to Philips I2C bus standard

» Multi-Master capable

» Clock stretching support and wait state generation

» Interrupt or bit-polling driven byte-by-byte data-transfers

» Arbitration lost interrupt with automatic transfer cancellation

» Start/Stop signal generation/detection

» Bus busy detection

» 7bit and 10bit addressing

4.7 GPIO - General Purpose Input and Output

The COMe-bIP2 offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32/K-Station. Please refer to the JIDA32/K-Station manual in the driver download packet on our customer section.

4.8 Dual Staged Watchdog Timer

Basics

A watchdog timer (or computer operating properly (COP) timer) is a computer hardware or software timer that triggers a system reset or other corrective action if the main program, due to some fault condition, such as a hang, neglects to regularly service the watchdog (writing a “service pulse” to it, also referred to as “kicking the dog”, “petting the dog”, “feeding the watchdog” or “triggering the watchdog”). The intention is to bring the system back from the nonresponsive state into normal operation.

The COMe-bIP2 offers a watchdog which works with two stages that can be programmed independently and used one by one.

Time-out events

Reset	A reset will restart the module and starts POST and operating system new.
NMI	A non-maskable interrupt (NMI) is a computer processor interrupt that cannot be ignored by standard interrupt masking techniques in the system. It is typically used to signal attention for non-recoverable hardware errors.
SCI	A system control interrupt (SCI) is a OS-visible interrupt to be handled by the OS using AML code
Delay	Might be necessary when an operating system must be started and the time for the first trigger pulse must extended. (Only available in the first stage)
WDT Signal only	This setting triggers the WDT Pin on baseboard connector (COM Express® Pin B27) only
Cascade:	Does nothing, but enables the 2nd stage after the entered time-out.

WDT Signal

B27 on COM Express® Connector offers a signal that can be asserted when a watchdog timer has not been triggered within time. It can be configured to any of the 2 stages. Deassertion of the signal is automatically done after reset. If deassertion during runtime is necessary please ask your Kontron technical support for further help.

4.9 Intel® Fast Flash Standby™ / Rapid Start Technology™

The target of Intel® Fast Flash Standby™ (iFFS) (also known as Intel® Rapid Start Technology™ iRST) is to get a wake-up time from S4 compareable to S3. Normally S4 is caused by OS which stores it's information to the hard disk and does then a normal shutdown. S4 resume takes quite long as the system does a normal BIOS POST and OS restores it's information from the hard disk.

IFFS does it in a different way. The Operating System initiates an S3 and stores it's information in memory. After that BIOS copies this OS information from DRAM to SSD and does a sleep state similar to S4 with nearly zero power. If system is resumed by power button, BIOS restores memory content from SSD to the DRAM and does an S3 resume which is much faster.

Requirements

» SATA Solid State Disk in AHCI mode

» Free disk space on the SSD with at least the DRAM size

» Operating System with disk partition tool to allocate the hibernation partition (e.g. Windows 7/8)

» BIOS supporting iFFS feature

How to setup once the operating system is installed

» Prepare a free disk space on your onboard or external SSD with at least the size of DRAM

» Open *cmd.exe* in Administrator Mode and type *diskpart.exe* to open the Windows disk partition tool

» DISKPART> list disk

» DISKPART> select disk X (X is disk number where you want to create the store partition. Refer to results from “list disk” for exact disk number)

» DISKPART> create partition primary

» DISKPART> detail disk

» DISKPART> select Volume X (X is Volume of your store partition. Refer to results from “detail disk” for exact volume number)

» DISKPART> set id=84 override (ID 84 marks the partition as hibernate partition)

» DISKPART> exit

» Now there should be a Hibernate Partition visible in your disk management

» Reboot and enable iFFS in BIOS

Usage

» Activate Lid / move system to Sleep/Standby (→S3)

» After configured period of time in Setup the system powers on automatically and information in DRAM moves to non-volatile memory (Default is *'immediately'*)

» System switches off again to iFFS (→comparable to S4, Power Supply can now be disconnected)

» When System is powered on, information moved back to DRAM (No display output during copy process)

» System resumes same as Sleep/Standby S3

Note

» Depending on the platform iFFS enabled may disable the hibernate function in Windows automatically

Benefits

» System transitions from S3 to S4 automatically

» Up to 6x battery life compared to Standby

» Resume time reduced up to 75%

Measured resume times from Power-on to Win7 Log-on Screen on COMe-mCT10:

» 2.5" SATA II HDD 5400rpm: Hibernate: 22s, iFFs on onboard NANDrive: 17s

» 2.5" SATA III SSD: Hibernate: 18s, iFFS on SSD: 10s

4.10 Speedstep Technology

The Intel® processors offer the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It enables you to adapt high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

By deactivating the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

4.11 C-States

New generation platforms include power saving features like SuperLFM, EIST (P-States) or C-States in O/S idle mode.

Activated C-States are able to dramatically decrease power consumption in idle mode by reducing the Core Voltage or switching of parts of the CPU Core, the Core Clocks or the CPU Cache.

Following C-States are defined:

C-State	Description	Function
C0	Operating	CPU fully turned on
C1	Halt State	Stops CPU main internal clocks via software
C1E	Enhanced Halt	Similar to C1, additionally reduces CPU voltage
C2	Stop Grant	Stops CPU internal and external clocks via hardware
C2E	Extended Stop Grant	Similar to C2, additionally reduces CPU voltage
C3	Deep Sleep	Stops all CPU internal and external clocks
C3E	Extended Stop Grant	Similar to C3, additionally reduces CPU voltage
C4	Deeper Sleep	Reduces CPU voltage
C4E	Enhanced Deeper Sleep	Reduces CPU voltage even more and turns off the memory cache
C6	Deep Power Down	Reduces the CPU internal voltage to any value, including 0V
C7	Deep Power Down	Similar to C6, additionally LLC (LastLevelCache) is switched off

C-States are usually enabled by default for low power consumption, but active C-States my influence performance sensitive applications or real-time systems.

» Active C6-State may influence data transfer on external Serial Ports

» Active C7-State may cause lower CPU and Graphics performance

It's recommended to disable C-States / Enhanced C-States in BIOS Setup if any problems occur.

4.12 Hyper Threading

Hyper Threading (officially termed Hyper Threading Technology or HTT) is an Intel®-proprietary technology used to improve parallelization of computations performed on PC´s. Hyper-Threading works by duplicating certain sections of the processor—those that store the architectural state but not duplicating the main execution resources. This allows a Hyper-Threading equipped processor to pretend to be two “logical” processors to the host operating system, allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always relies on the Operating System.

4.13 Dynamic FSB Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency by half to further decrease the minimum processor operating frequency from the Enhanced Intel SpeedStep Technology performance states and achieve the Super Low Frequency Mode (Super LFM). This feature is supported at FSB frequencies of 1066 MHz, 800 MHz and 667 MHz and does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and GMCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. Both the processor and GMCH maintain a virtual BCLK signal (VBCLK) that is aligned to the external BCLK but at half the frequency.

After a downward shift, it would appear externally as if the bus is running with a 133-MHz base clock in all aspects, except that the actual external BCLK remains at 266 MHz. See Figure 3 for details. The transition into Super LFM, a “down-shift,” is done following a handshake between the processor and GMCH. A similar handshake is used to indicate an “up-shift,” a change back to normal operating mode. Please ensure this feature is enabled and supported in the BIOS.

4.14 VID-x

The processor implements the VID-x feature for improved control of core voltage levels when the processor enters a reduced power consumption state. VID-x applies only when the processor is in the Intel Dynamic Acceleration Technology performance state and one or more cores are in low-power state (i.e., CC3/CC4/CC6). VID-x provides the ability for the processor to request core voltage level reductions greater than one VID tick. The amount of VID tick reduction is fixed and only occurs while the processor is in Intel Dynamic Acceleration Technology mode. This improved voltage regulator efficiency during periods of reduced power consumption allows for leakage current reduction which results in platform power savings and extended battery life.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw an Instantaneous current (ICC_CORE_INST) for a short duration of tINST; however, the average ICC current will be lesser than or equal to ICCDES current specification.

4.15 Intel® Turbo Boost Technology and AVX

For applications that are particularly power-hungry, the new processors provide enhanced Intel® Turbo Boost technology. This automatically shifts processor cores and processor graphics resources to accelerate performance, tailoring a workload to give users an immediate performance boost for their applications whenever needed. Another innovation is the enhancement to the 256-bit instruction set, known as Intel® Advanced Vector Extensions (AVX). AVX delivers improved performance, rich functionality and the ability to manage, rearrange and sort data in a better way. The new instruction set accelerates floating-point intensive applications such as “number crunchers” or digital processing of images, videos and audio data.

Intel® Turbo Boost Technology 2.0

Intel has optimized Intel® Turbo Boost Technology to provide even more performance when needed on the latest-generation Intel® microarchitecture. Intel® Turbo Boost Technology 2.0 automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits. Intel Turbo Boost Technology 2.0 is activated when the Operating System (OS) requests the highest processor performance state (P0).

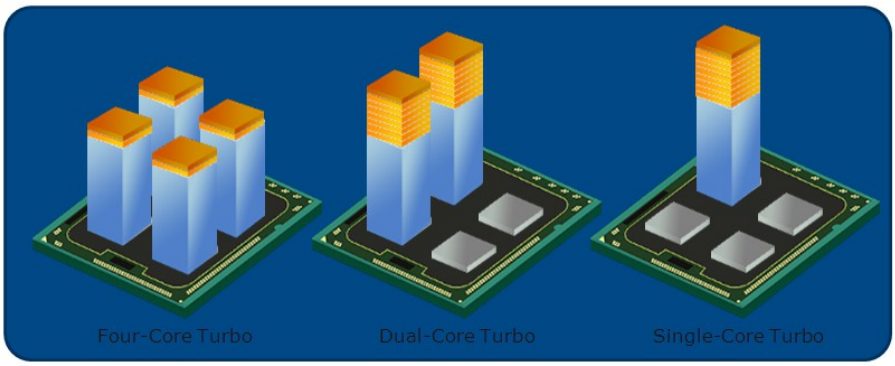
The maximum frequency of Intel Turbo Boost Technology 2.0 is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology 2.0 state depends on the workload and operating environment. Any of the following can set the upper limit of Intel Turbo Boost Technology 2.0 on a given workload:

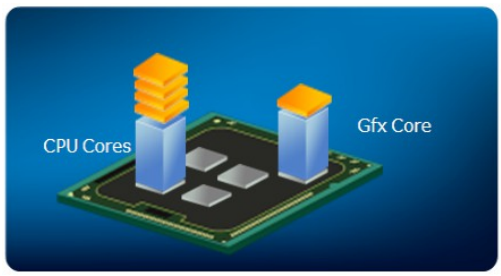
» Number of active cores

» Estimated current consumption

» Estimated power consumption

» Processor temperature

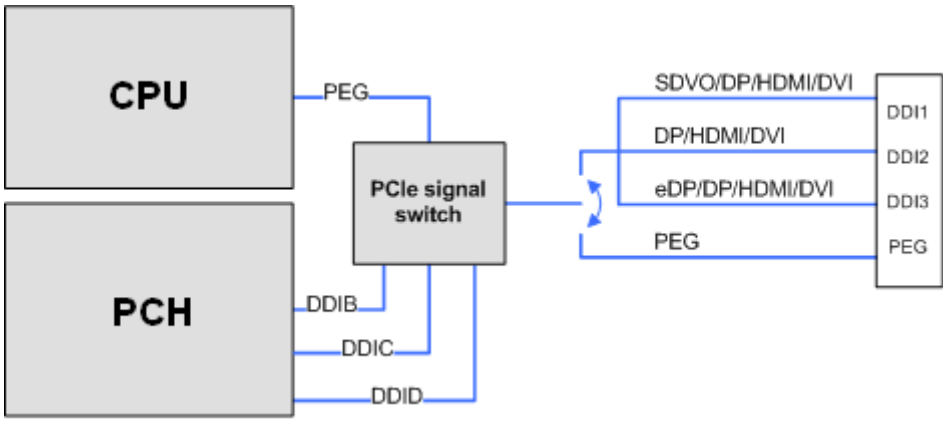




When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Intel Turbo Boost Technology 2.0 has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency. Note: Intel Turbo Boost Technology 2.0 allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

4.16 Shared Graphics Interfaces

On COM Express® pin-out Type 2 based Computer-on-Modules the PCI Express Graphics interface is usually multiplexed with several digital display interfaces like SDVO, DisplayPort, HDMI or TMDS if supported by the chipset. The new generation Chief River platform no longer shares it's interfaces. For full backwards compatibility the COMe-bIP2 includes multi-staged PCIexpress 2.0 switches to provide a shared graphics output on PEG Interface similar to former platforms. It offers full functionality like auto detection for external Graphics or SDVO devices.



PEG Interface pin-outs

COM Express		x16 PCI Express		SDVO		HDMI & DVI		Display Port	
Pin	Name	Pin	Name	Pin name	Description	Pin name	description	pin name	description
D52	PEG_TX[0]+	B14	HSOp(0)	SDVOB_RED_P	Digital Video B red	TMDS_B_DATA2_P	HDMI Port B Data2	DPB_LANE0_P	DisplayPort B Lane0 output
D53	PEG_TX[0]-	B15	HSOn(0)	SDVOB_RED_N	output differential pair	TMDS_B_DATA2_N	output differential pair	DPB_LANE0_N	differential pair
D55	PEG_TX[1]+	B19	HSOp(1)	SDVOB_GRN_P	Digital Video B green	TMDS_B_DATA1_P	HDMI Port B Data1	DPB_LANE1_P	DisplayPort B Lane1 output
D56	PEG_TX[1]-	B20	HSOn(1)	SDVOB_GRN_N	output differential pair	TMDS_B_DATA1_N	output differential pair	DPB_LANE1_N	differential pair
D58	PEG_TX[2]+	B23	HSOp(2)	SDVOB_BLU_P	Digital Video B blue	TMDS_B_DATA0_P	HDMI Port B Data0	DPB_LANE2_P	DisplayPort B Lane2 output
D59	PEG_TX[2]-	B24	HSOn(2)	SDVOB_BLU_N	output differential pair	TMDS_B_DATA0_N	output differential pair	DPB_LANE2_N	differential pair
D61	PEG_TX[3]+	B27	HSOp(3)	SDVOB_CK_P	Digital Video B clock	TMDS_B_CLK_P	HDMI Port B Clock output	DPB_LANE3_P	DisplayPort B Lane3 output
D62	PEG_TX[3]-	B28	HSOn(3)	SDVOB_CK_N	differential pair	TMDS_B_CLK_N	differential pair	DPB_LANE3_N	differential pair
D65	PEG_TX[4]+	B33	HSOp(4)	-	-	TMDS_C_DATA2_P	HDMI Port C Data2 output	DPC_LANE0_P	DisplayPort C Lane0 output
D66	PEG_TX[4]-	B34	HSOn(4)	-	-	TMDS_C_DATA2_N	differential pair	DPC_LANE0_N	differential pair
D68	PEG_TX[5]+	B37	HSOp(5)	-	-	TMDS_C_DATA1_P	HDMI Port C Data1 output	DPC_LANE1_P	DisplayPort C Lane1 output
D69	PEG_TX[5]-	B38	HSOn(5)	-	-	TMDS_C_DATA1_N	differential pair	DPC_LANE1_N	differential pair
D71	PEG_TX[6]+	B41	HSOp(6)	-	-	TMDS_C_DATA0_P	HDMI Port C Data0 output	DPC_LANE2_P	DisplayPort C Lane2 output
D72	PEG_TX[6]-	B42	HSOn(6)	-	-	TMDS_C_DATA0_N	differential pair	DPC_LANE2_N	differential pair
D74	PEG_TX[7]+	B45	HSOp(7)	-	-	TMDS_C_CLK_P	HDMI Port C Clock output	DPC_LANE3_P	DisplayPort C Lane3 output
D75	PEG_TX[7]-	B46	HSOn(7)	-	-	TMDS_C_CLK_N	differential pair	DPC_LANE3_N	differential pair
D78	PEG_TX[8]+	B50	HSOp(8)	-	-	TMDS_D_DATA2_P	HDMI Port D Data2 output	DPD_LANE0_P	DisplayPort D Lane0 output
D79	PEG_TX[8]-	B51	HSOn(8)	-	-	TMDS_D_DATA2_N	differential pair	DPD_LANE0_N	differential pair
D81	PEG_TX[9]+	B54	HSOp(9)	-	-	TMDS_D_DATA1_P	HDMI Port D Data1 output	DPD_LANE1_P	DisplayPort D Lane1 output
D82	PEG_TX[9]-	B55	HSOn(9)	-	-	TMDS_D_DATA1_N	differential pair	DPD_LANE1_N	differential pair
D85	PEG_TX[10]+	B58	HSOp(10)	-	-	TMDS_D_DATA0_P	HDMI Port D Data0 output	DPD_LANE2_P	DisplayPort D Lane2 output
D86	PEG_TX[10]-	B59	HSOn(10)	-	-	TMDS_D_DATA0_N	differential pair	DPD_LANE2_N	differential pair
D88	PEG_TX[11]+	B62	HSOp(11)	-	-	TMDS_D_CLK_P	HDMI Port D Clock output	DPD_LANE3_P	DisplayPort D Lane3 output
D89	PEG_TX[11]-	B63	HSOn(11)	-	-	TMDS_D_CLK_N	differential pair	DPD_LANE3_N	-
D91	PEG_TX[12]+	B66	HSOp(12)	-	-	-	-	-	-
D91	PEG_TX[12]-	B67	HSOn(12)	-	-	-	-	-	-
D94	PEG_TX[13]+	B70	HSOp(13)	-	-	-	-	-	-

D95	PEG_TX[13]-	B71	HSOn(13)	-	-	-	-	-	-
D98	PEG_TX[14]+	B74	HSOp(14)	-	-	-	-	-	-
D99	PEG_TX[14]-	B75	HSOn(14)	-	-	-	-	-	-
D101	PEG_TX[15]+	B78	HSOp(15)	-	-	-	-	-	-
D102	PEG_TX[15]-	B79	HSOn(15)	-	-	-	-	-	-
C52	PEG_RX[0]+	A16	HSIp(0)	SDVO_TVCLKIN_P	Digital Video TVOUT sync	-	-	-	-
C53	PEG_RX[0]-	A17	HSIn(0)	SDVO_TVCLKIN_N	clock input differential	-	-	-	-
C55	PEG_RX[1]+	A21	HSIp(1)	SDVO_INT_P	Digital Video B interrupt	-	-	-	-
C56	PEG_RX[1]-	A22	HSIn(1)	SDVO_INT_N	differential pair	-	-	-	-
C58	PEG_RX[2]+	A25	HSIp(2)	SDVO_STALL_P	Digital Video Field Stall	-	-	DPB_AUX_P	DisplayPort B Aux output
C59	PEG_RX[2]-	A26	HSIn(2)	SDVO_STALL_N	differential pair	-	-	DPB_AUX_N	differential pair
C61	PEG_RX[3]+	A29	HSIp(3)	-	-	TMDS_B_HPD#	-	DPB_HPD#	DisplayPort B Hotplug detect
C62	PEG_RX[3]-	A30	HSIn(3)	-	-	-	-	-	-
C65	PEG_RX[4]+	A35	HSIp(4)	-	-	-	-	-	-
C66	PEG_RX[4]-	A36	HSIn(4)	-	-	-	-	-	-
C65	PEG_RX[5]+	A39	HSIp(5)	-	-	-	-	-	-
C66	PEG_RX[5]-	A40	HSIn(5)	-	-	-	-	-	-
C71	PEG_RX[6]+	A43	HSIp(6)	-	-	-	-	DPC_AUX_P	DisplayPort C Aux input
C72	PEG_RX[6]-	A44	HSIn(6)	-	-	-	-	DPC_AUX_N	differential pair
C74	PEG_RX[7]+	A47	HSIp(7)	-	-	TMDS_C_HPD#	-	DPC_HPD#	DisplayPort C Hotplug detect
C74	PEG_RX[7]-	A48	HSIn(7)	-	-	-	-	-	-
C78	PEG_RX[8]+	A52	HSIp(8)	-	-	-	-	-	-
C79	PEG_RX[8]-	A53	HSIn(8)	-	-	-	-	-	-
C81	PEG_RX[9]+	A56	HSIp(9)	-	-	-	-	-	-
C82	PEG_RX[9]-	A57	HSIn(9)	-	-	-	-	-	-
C85	PEG_RX[10]+	A60	HSIp(10)	-	-	-	-	DPD_AUX_P	DisplayPort D Aux input
C86	PEG_RX[10]-	A61	HSIn(10)	-	-	-	-	DPD_AUX_N	differential pair
C88	PEG_RX[11]+	A64	HSIp(11)	-	-	TMDS_D_HPD#	-	DPD_HPD#	DisplayPort D Hotplug detect
C89	PEG_RX[11]-	A65	HSIn(11)	-	-	-	-	-	-
C91	PEG_RX[12]+	A68	HSIp(12)	-	-	-	-	-	-
C92	PEG_RX[12]-	A69	HSIn(12)	-	-	-	-	-	-
C94	PEG_RX[13]+	A72	HSIp(13)	-	-	-	-	-	-
C95	PEG_RX[13]-	A73	HSIn(13)	-	-	-	-	-	-
C98	PEG_RX[14]+	A76	HSIp(14)	-	-	-	-	-	-
C99	PEG_RX[14]-	A77	HSIn(14)	-	-	-	-	-	-
C101	PEG_RX[15]+	A80	HSIp(15)	-	-	-	-	-	-
C102	PEG_RX[15]-	A81	HSIn(15)	-	-	-	-	-	-
D73	SDVO_CLK	B17	PRSNT2#	SDVO_CTRL_CLK	SDVO I2C clock line	DDPB_CTRLCLK	HDMI port B Control Clock	-	-
C73	SDVO_DATA	B31	PRSNT2#1	SDVO_CTRL_DATA	SDVO I2C data line	DDPB_CTRLDATA	HDMI port B Control Data	DDPB_CTRLDATA	only used as boot strap
D63	RSVD	-	-	-	-	DDPC_CTRLCLK	HDMI port C Control Clock	-	-
D64	RSVD	-	-	-	-	DDPC_CTRLDATA	HDMI port C Control Data	DDPC_CTRLDATA	only used as boot strap
C97	RSVD	-	-	-	-	DDPD_CTRLCLK	HDMI port D Control Clock	-	-
D83	RSVD	-	-	-	-	DDPD_CTRLDATA	HDMI port D Control Data	DDPD_CTRLDATA	only used as boot strap

4.17 Display Configuration

The chapter describes possible display configurations and supported features for the integrated Intel® GMA HD4000 (Gen7) graphics.

Dual Display Configurations in O/S

Display	N/A	CRT	LVDS fix	LVDS DID	LVDS2DVI	DP/eDP	DP2DVI	DP2HDMI	DP2CRT	SDVO2LVDS	SDVO2DVI	SDVO2CRT
N/A	-	S	S	S	S	S	S	S	S	S	S	S
CRT	S	-	A	A	A	A	A	A	A	A	A	A
LVDS fix	S	A	-	-	-	A	A	A	A	A*	A	A
LVDS DID	S	A	-	-	-	A	A	A	A	A*	A	A
LVDS2DVI	S	A	-	-	-	A	A	A	A	A*	A	A
DP	S	A	A	A	A	A	A	A	A	A	A	A
DP2DVI	S	A	A	A	A	A	A	A	A	A	A	A
DP2HDMI	S	A	A	A	A	A	A	A	A	A	A	A
DP2CRT	S	A	A	A	A	A	A	A	A	A	A	A
eDP	-	-	-	-	-	-	-	-	-	-	-	-
SDVO2LVDS	S	A	A*	A*	A*	A	A	A	A	-	-	-
SDVO2DVI	S	A	A	A	A	A	A	A	A	-	-	-
SDVO2CRT	S	A	A	A	A	A	A	A	A	-	-	-

SDVO2DVI: only supported if BIOS DDI1 is enabled and set to SDVO - DVI 1.0 or SDVO - DVI-I

SDVO2CRT: only supported if BIOS DDI1 is enabled and set to SDVO - DVI-I

» S = Single Display

» A = All Modes (Single Display, Clone Mode, Extended Desktop)

» A* = All Modes, but requires a customized BIOS

» - = Not supported

» N/A = Display not attached

Dual Display configurations in Setup and POST

Display	N/A	CRT	LVDS fix	LVDS DID	LVDS2DVI	DP/eDP	DP2DVI	DP2HDMI	DP2CRT	SDVO2LVDS	SDVO2DVI	SDVO2CRT
N/A	-	S	S	S	S	S	S	S	S	S	S	-
CRT	S	-	C	C*	Twin	C	C	C	C	C	C	-
LVDS fix	S	C	-	-	-	C	C	C	C	C*1	C	-
LVDS DID	S	C*	-	-	-	C*	C*	C*	C*	C*1	C*	-
LVDS2DVI	S	Twin	-	-	-	C	C	C	C	C*1	C	-
DP	S	C	C	C*	C	C	C	C	C	C*	C*	-
DP2DVI	S	C	C	C*	C	C	C	C	C	C*	C*	-
DP2HDMI	S	C	C	C*	C	C	C	C	C	C*	C*	-
DP2CRT	S	C	C	C*	C	C	C	C	C	C*	C*	-
eDP	-	-	-	-	-	-	-	-	-	-	-	-
SDVO2LVDS	S	C	C*1	C*1	C*1	C*	C*	C*	C*	-	-	-
SDVO2DVI	S	C	C	C*	C	C*	C*	C*	C*	-	-	-
SDVO2CRT	-	-	-	-	-	-	-	-	-	-	-	-

SDVO2DVI: only supported if BIOS DDI1 is enabled and set to SDVO - DVI 1.0 or SDVO - DVI-I

» S = Single Display

» C = Clone Mode

» C* = Clone Mode, requires manual display configuration in setup. With Auto detection LVDS only is supported

» C*1 = Clone Mode, but requires a customized BIOS

» Twin = Twin Mode with 2 Displays on Display Pipe 1.

» - = Not supported

» N/A = Display not attached

In Clone Mode Display Pipe 2 only shows VESA Modes in POST, Setup and EFI Shell. DOS, Windows boot or the Windows Installation is using VGA Mode which is not supported by Display Pipe 2. With CRT and LVDS with EDID (e.g. LVDS2DVI Adapter) the Twin Mode is active without VESA mode restrictions

eDP - embedded Display Port

Intel® 6 & 7-Series Chipset based Computer-on-modules support the embedded Display Port shared on Digital Display Interface DDI3. To enable the eDP, LVDS must be switched off by hardware strap option. This feature is implemented in COMe-bSC2 (starting with hardware revision CE 2.x.x) and COMe-bIP2/6 by external strap option on the carrier board. The General Purpose Input GPI3 (COM Express Pin A85) is pulled-up with 10kOhm on the module. Leaving GPI3 open on the baseboard enables LVDS (default configuration). To enable the eDP instead of LVDS, GPI3 must be pulled-down with a resistor ≤1kOhm or tied directly to GND during boot-up.

The GPIO should not be used during boot-up until CB_RESET# becomes inactive

Digital Display Interface Features

The integrated Intel® GMA HD4000 (Gen7) graphics supports:

» High-bandwidth Digital Content Protection (HDCP) on HDMI and DisplayPort with up to 2 HDCP streams simultaneously

» One active Protected Audio and Video Path (PAVP) session on HDMI or DisplayPort

» Dual Stream DP/HDMI Audio if activated in BIOS (See BIOS Chapter HDAudio Configuration) and O/S (HDMI codec DDI enabled)

» DP/HDMI/DVI Hot-plug (low-active)

Supported Audio Formats on HDMI and DisplayPort

Audio Formats	HDMI	DisplayPort
AC-3 Dolby Digital	YES	NO
Dolby Digital Plus	YES	NO
DTS-HD	YES	NO
LPCM, 192kHz/24bit, 8 channel	YES	YES (Up to 2 channel 96kHz, 24bit)
Dolby True HD, DTS HD Master Audio	YES	NO

DDI Design Consideration

» For sufficient signal quality baseboard designs with long signal lanes or impedance leaps may require an Equalicer or Redriver for the digital display interfaces

» Due to backwards compatibility to former platforms the DDI hot-plug detection is converted to low active

» SDVO can be used for external conversion to VGA, LVDS, TV-out and requires additional hardware on your baseboard

» DisplayPort can be used directly or with external adapters for HDMI, DVI or VGA

» HDMI or DVI usage on a baseboard requires a level shifter

Find more details for DDI usage as DisplayPort, HDMI or DVI with schematic examples available on http://emdcustomersection.kontron.com

DVI-I Design Topology

DVI-I is supported on PCH Digital Display Port B (COM DDI1) only. The implementation involves routing VGA and DVI-D signals to DVI-I connector:

» VGA port RGB signals should be routed to Analog RGB pins on the DVI-I connector

» DVI Data and Clock signals on PCH Digital Display Port B should be routed to TMDS Data 0, 1 and 2 pins and TMDS Clock pin of DVI-I connector respectively

» DVI HPD signals should be routed to the HPD pin of the DVI-I connector

» DVI DDC Clock and Data signals on PCH Digital Display Port B should be routed to the DDC Clock and Data pins of the DVI-I connector.

3 independent Display Support

The COMe-bIP2 supports up to 3 independent displays in Windows and Linux by using 2 DDI Ports as DisplayPort. The third display can either be VGA or LVDS or DP/HDMI/DVI/SDVO

4.18 Hybrid Graphics / Multi-monitor

The COMe-bIP2 supports Hybrid Multi-monitor function which is one form of Intel's Hybrid Graphics where integrated graphics (in Chipset or CPU) is available to operate simultaneously with external PEG; PCIe or PCI graphics. This feature enables concurrent function of Intel's integrated Graphics Processing Unit (GPU/iGFX) along with a discrete GPU solution, allowing for operability of greater than two independently-driven displays. The O/S will handle control of the multiple GPU display adapters appropriately. For example, WindowsXP supports The Microsoft Windows XP Display Driver Model (XPDM) which allows loading and support of multiple graphics drivers. Windows 7 continues that legacy XPDM support but also adds WDDM v1.1 which, like XPDM, allows for simultaneous multiple graphics drivers (Windows Vista WDDM v1.0 did not allow this capability). Operating system applications will be adapter-unaware through use of the O/S GUI APIs and will utilize the adapter associated with the primary display, regardless of which display the image is located on.

Some applications may be adapter-aware, e.g., full-screen applications and system applications like the compositor. A number of software tools designed to assist multi-monitor use are available from third parties. One example is the UltraMon* utility for multi-monitor systems, which helps with the position of applications, assists desktop wallpapers and screen savers in multi-monitor configurations.

Hybrid Multi-monitor mode is recommended to be accomplished using a discrete third-party PCI Express graphics card either into the PEG slot of the platform or into an available PCI Express slot routed off of the I/O subsection of the chipset.

Requirements

» Baseboard supporting PEG (alternatively PCIe or PCI)

» Module BIOS which allows switching between iGFX and discrete GPU (iGFX must be set to primary boot display)

» O/S supporting heterogeneous display adapters (Linux / WindowsXP / Windows 7)

Setup a Multi-monitor system

» Start without the discrete GPU seated in the system

» Select IGD as Primary Boot Display in BIOS Setup

» Boot into O/S and install drivers requested for the integrated GPU

» Shut down the system and insert the discrete GPU

» Boot into O/S and install drivers requested for the discrete GPU (if necessary in Safe mode)

» Set the Windows Display properties as referenced below (example: WindowsXP)

In most cases the graphical user interfaces (e.g. ATI Catalyst Control Center) for both GPUs may not run properly. It's recommended to use O/S implemented Display Properties like in screenshot above

Detailed documentation is available in Intel Paper 323214

4.19 Intel® vPro™ technology

Kontron and Intel® are addressing the security and manageability challenges facing embedded systems today with the implementation of Intel® vPro™ technology to enable: » System integrity » Secure isolation » Remote systems management

First, system integrity is the ability to identify whether the system hardware or system software has been modified without authorization. When a system's integrity is known, the system can be thought of as a trusted system. Second, secure isolation is the ability to use platform hardware to separate processes, resources, and data on the system such that they cannot interact with each other in unintended ways. By providing hardware-assisted isolation, there is limitless security, privacy, and cost savings that can be realized through consolidation and workload isolation. Finally, remote systems management is the ability to troubleshoot, perform power management or system verification through secure channels. Significant cost savings and efficiencies can be realized through remote management allowing for increased system up time and the ability to manage or diagnose a system, even when powered down.

Intel® vPro™ technology itself is special functionality designed into both, the processor and the chipset. The three technologies that comprise Intel® vPro™ technology are: Intel Virtualization Technology (Intel® VT), Intel Trusted Execution Technology (Intel® TXT) and Intel Active Management Technology (Intel® AMT).

Intel® VT provides hardware-based assists making secure isolation more efficient and decreases the virtualization footprint, lowering the effective attack surface of a solution. This hardware-based technology can help to protect applications and information by running multiple operating systems (OSs) in isolation on the same physical system. A virtual guest OS can be created in an entirely separate space on the physical system to run specialized or critical applications. Virtual environments leverage Intel® VT for memory, CPU, and Directed I/O virtualization. Intel® TXT provides the ability to use hardware-based mechanisms to verify system integrity during the boot process. It also provides system memory scrubbing that protects against soft reset attacks. Virtualized environments take advantage of Intel® TXT launch environment verification to establish a dynamic root of trust providing added security to hypervisor or virtual machine monitor (VMM).

Mechanisms employed by Intel® AMT include domain authentication, session keys, persistent data storage in the Intel® AMT hardware, and access control lists. Only firmware images that are digitally signed by Intel are permitted to load and execute. This set of hardware-based features is targeted for businesses and allows remote access to the system, whether wired or wireless, for management and security tasks. Because of the special hardware capabilities provided by Intel® AMT, out of band access is available even when the OS is not functional or system power is off.

Intel® TXT and Intel® AMT are disabled by default. Please contact your local sales or support for BIOS versions with full vPro™ support

4.20 ACPI Suspend Modes and Resume Events

The COMe-bIP2 supports the S-states S0, S3, S4, S5. S5eco Support: YES

The following events resume the system from S3:

» USB Keyboard (1)

» USB Mouse (1)

» Power Button

» WakeOnLan (2)

The following events resume the system from S4:

» Power Button

» WakeOnLan (2)

The following events resume the system from S5:

» Power Button

» WakeOnLan (2)

The following events resume the system from S5Eco:

» Power Button

(1) OS must support wake up via USB devices and baseboard must power the USB Port with StBy-Voltage
(2) Depending on the Used Ethernet MAC/Phy WakeOnLan must be enabled in BIOS setup and driver options

5 System Resources

5.1 Interrupt Request (IRQ) Lines

IRQ #	Used For	Available	Comment
0	Timer0	No	-
1	Keyboard	No	-
2	Cascade	No	-
3	COM2	No	Type2: External SIO COM2, Type6: onboard COM2
4	COM1	No	Type2: External SIO COM1, Type6: onboard COM1
5	COM3	Note(4)	Type2: not used, Type6: External SIO COM1
6	-	Yes	-
7	SIO LPT	No	-
8	RTC	No	-
9	ACPI	No	-
10	COM4	Note(4)	Type2: not used, Type6: External SIO COM2
11	SMBus	No	-
12	PS/2 Mouse	No	-
13	FPU	No	-
14	-	Yes	-
15	-	Yes	-
16	LNK A	No	PCIe RP 0 + PCIe RP 4 + USB EHCI#1 + Intel ME + I.G.D.; Note(3)
17	LNK B	No	PCIe2Pata (Type2 only) + PCIe RP 1 + PCIe RP 5; Note(3)
18	LNK C	No	PCIe2PCI (Type2 only) + PCIe RP 2 + PCIe RP 6; Note(3)
19	LNK D	No	PCIe RP 3 + SATA AHCI; Note(3)
20	LNK E	No	Note(3)
21	LNK F	No	Note(3)
22	LNK G	No	Note(3)
23	LNK H	No	USB EHCI#2

(1) If the “Used For” device is disabled in setup, the corresponding interrupt is available for other device.
(2) Not available if ACPI is used
(3) ACPI OS decides on particular IRQ usage
(4) Depends on system configuration (onboard COM Port support and external SIO presence)

5.2 Memory Area

The first 640 kB of DRAM are used as main memory. Using DOS, you can address 1 MB of memory directly. Memory area above 1 MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for infor- mation about HIMEM.SYS and EMM386.EXE. Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Used for	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic controller
C0000h – CFFFFh	VGA BIOS	No	Used by onboard VGA ROM
D0000h – DFFFFh	-	Yes	Free for shadow RAM in standard configurations.
E0000h – FFFFFh	System BIOS	No	Fixed
20000000h-201FFFFFh	IGFX	No	Fixed
40000000h-401FFFFFh	IGFX	No	Fixed
E0000000h–FEAFFFFFh	PCIe Config Space	No	Fixed
FED00000h-FED003FFh	HPET	No	Fixed
FED10000h-FED17FFFh	MCH	No	Fixed
FED18000h-FED18FFFh	DMI	No	Fixed
FED19000h-FED19FFFh	EPBA	No	Fixed
FED1C000h-FED1FFFFh	RCBA	No	Fixed
FED20000h FED3FFFFh	TXT	No	Fixed
FED40000h FED44FFFh	TPM	No	Fixed
FED45000h FED8FFFFh	TPM	No	Fixed
FED90000h-FED93FFFh	VT-d	No	Fixed
FEE00000h-FEEFFFFFh	IOxAPIC	No	Fixed
FF000000h-FFFFFFFFh	BIOS Flash	No	Fixed

5.3 I/O Address Map

The I/O-port addresses of the are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0100h with additional hardware for compatibility reasons, even if available.

I/O Address	Used for	Available	Comment
0000 - 001F	System Ressources	No	Fixed
0020 - 003F	Interrupt Controller 1	No	Fixed
002E - 002F	Ext. SIO	No	Fixed
0040 - 005F	Timer, Counter	No	Fixed
004E - 004F	TPM	No	Fixed
0060 - 006F	Keyboard controller	No	Fixed
0070 - 007F	RTC and CMOS Registers	No	Fixed
0080	BIOS Postcode	No	Fixed
0081 - 009F	DMA Controller	No	Fixed
00A0 - 00BF	Interrupt Controller	No	Fixed
00C0 - 00DF	DMA Controller	No	Fixed
00F0 - 00FF	Math Coprocessor	No	Fixed
0290 - 029F	Ext. SIO	No	Fixed
03B0 - 03DF	VGA	No	Fixed
0400 - 047F	Chipset	No	Fixed
04D0 - 04D1	Chipset	No	Fixed
0500 - 057F	Chipset	No	Fixed
0680 - 069F	Chipset	No	Fixed
0A80 - 0A81	CPLD	No	Fixed
0B78 - 0B7F	Chipset	No	Fixed
0CF8 - 0CFF	Chipset	No	Fixed

5.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) respectivily the PCI Express Base 1.0a specification. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

PCI Device	B:D:F	PCI IRQ	Interface	Comment
Host Bridge	0:0:0	None	internal	Chipset
P.E.G. Root Port	0:1:0	LNK A	internal	Chipset
Video Controller	0:2:0	LNK A	internal	Chipset
XHCI	0:20:0	LNK A	internal	Chipset
ME	0:22:0	LNK A	internal	Chipset
GbE	0:25:0	LNK E	PCIe	Chipset
HDA	0:27:0	LNK G	PCIe	Chipset
PCIe Port 0	0:28:0	LNK A	internal	Chipset
PCIe Port 0 Slot	-	A/B/C/D	PCIe	Port 0
PCIe Port 1	0:28:1	LNK A	internal	Chipset
PCIe Port 1 Slot	-	B/C/D/A	PCIe	Port 1
PCIe Port 2	0:28:2	LNK A	internal	Chipset
PCIe Port 2 Slot	-	C/D/A/B	PCIe	Port 2
PCIe Port 3	0:28:3	LNK A	internal	Chipset
PCIe Port 3 Slot	-	D/A/B/A	PCIe	Port 3
PCIe Port 4	0:28:4	LNK A	internal	Chipset
PCIe Port 4 Slot	-	A/B/C/D	PCIe	Port 4
PCIe Port 5	0:28:5	LNK A	internal	Chipset
PCIe Port 5 Slot	-	B/C/D/A	PCIe	Port 5
PCIe Port 6	0:28:6	LNK A	internal	Chipset
PCIe Port 6 Slot	-	C/D/A/B	PCIe	Port 6
PCIe Port 7	0:28:7	LNK A	internal	Chipset
EHCI	0:29:0	LNK H	internal	Chipset
LPC Bridge	0:31:0	-	internal	Chipset
SATA	0:31:2	LNK D	internal	Chipset
SMBus	0:31:3	LNK C	internal	Chipset
PCIe2PATA	X:00:0	LNK A	PCIe	Slot 5
PCIe2PCI	Y:00:0	LNK A	PCIe	Slot 6

5.5 I2C Bus

I2C Address	Used For	Available	Comment
58h	S5 Eco	No	S5 Eco Resistor
A0h	JIDA-EEPROM	No	Module EEPROM
AEh	FRU-EEPROM	No	Recommended for Baseboard EEPROM

5.6 JILI I2C Bus

I2C Address	Used For	Available	Comment
A0h	JILI-EEPROM	No	EEPROM for JILI Data

5.7 SDVO I2C Bus

I2C Address	Used For	Available	Comment
-	-	-	-

5.8 System Management (SM) Bus

The 8-bit SMBus addresses uses the LSB (Bit 0) for the direction. Bit0 = 0 defines the write address, Bit0 = 1 defines the read address for the device. The 8-bit addresses listed below shows the write adress for all devices. 7-bit SMBus adresses shows the device address without Bit0.

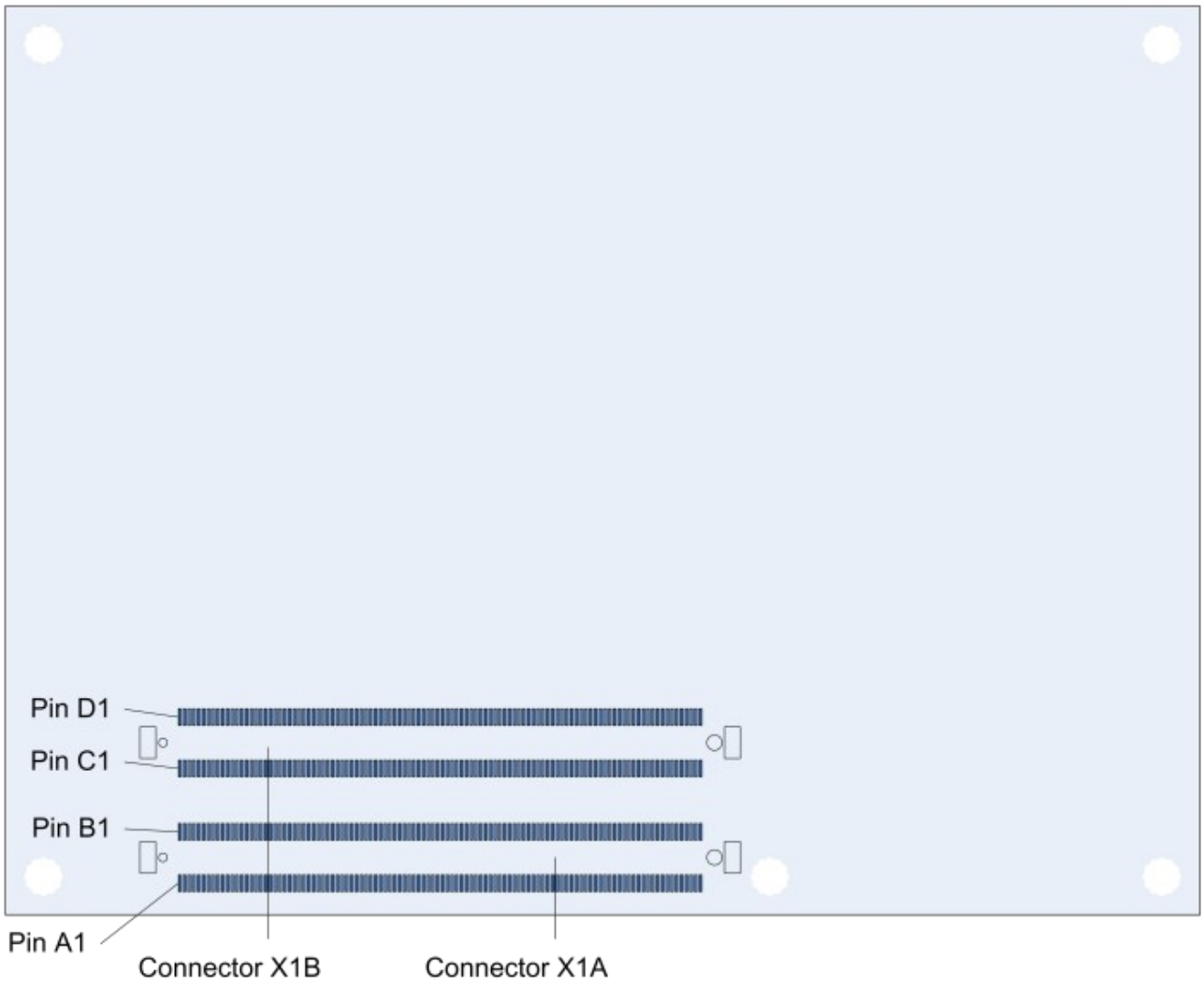
8-bit Address	7-bit Address	Device	Comment	SMBus
12h	0x09	SMART_CHARGER	Not to be used with any SM bus device except a charger	SMB
14h	0x0A	SMART_SELECTOR	Not to be used with any SM bus device except a selector or manager	SMB
16h	0x0B	SMART_BATTERY	Not to be used with any SM bus device except a battery	SMB
30h	0x18	DDR3 Thermal Sensor Chan. A	Do not use under any circumstances	SMB
34h	0x1A	DDR3 Thermal Sensor Chan. B	Do not use under any circumstances	SMB
58h	0x2C	HWM NCT7802Y (non ECC Design)	Do not use under any circumstances	SMB
5Ch	0x2E	HWM ADT7490 (ECC Design)	Do not use under any circumstances	SMB
A0h	0x50	DDR3 channel A SPD	Do not use under any circumstances	SMB
A4h	0x52	DDR3 channel B SPD	Do not use under any circumstances	SMB
C8h	0x64	Ethernet 82579	Do not use under any circumstances	SML0

A JIDA Bus No. like in former Modules cannot be provided because the EAPI driver implementation enumerates the I2C busses dynamically. Please follow the initialisation process like it is provided in the EAPI specification.

6 Connectors

The pin-outs for Interface Connectors X1A and X1B are documented for convenient reference. Please see the COM Express® Specification and COM Express® Design Guide for detailed, design-level information.

6.1 Connector Location



7 Pinout List

7.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection

To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN60950

7.2 Connector X1A Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	GBE0_MDI3_N / Ethernet Receive Data -	DP-I	-	-
A3	GBE0_MDI3+	GBE0_MDI3_P / Ethernet Receive Data -	DP-I	-	-
A4	GBE0_LINK100#	GBE0_LINK100# / Ethernet Speed LED	O-3.3	-	-
A5	GBE0_LINK1000#	GBE0_LINK1000# / Ethernet Speed LED	O-3.3	-	-
A6	GBE0_MDI2-	GBE0_MDI2_N / Ethernet Receive Data -	DP-I	-	-
A7	GBE0_MDI2+	GBE0_MDI2_P / Ethernet Receive Data -	DP-I	-	-
A8	GBE0_LINK#	GBE0_LINK# / LAN Link LED	OD	-	-
A9	GBE0_MDI1-	GBE0_MDI1_N / Ethernet Receive Data -	DP-I	-	-
A10	GBE0_MDI1+	GBE0_MDI1_P / Ethernet Receive Data +	DP-I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	GBE0_MDI0_N / Ethernet Transmit Data -	DP-O	-	-
A13	GBE0_MDI0+	GBE0_MDI0_P / Ethernet Transmit Data +	DP-O	-	-
A14	GBE0_CTREF	GBE0_CTREF	O-1,8	-	n. c. on module, because not needed with 82579LM
A15	SUS_S3#	PM_SLP_S3_EXT#	O-3.3	PD 10k	-
A16	SATA0_TX+	SATA_TX0_P / SATA 0 Transmit Data +	DP-O	-	-
A17	SATA0_TX-	SATA_TX0_N / SATA 0 Transmit Data -	DP-O	-	-
A18	SUS_S4#	PM_SLP_S4#	O-3.3	-	-
A19	SATA0_RX+	SATA_RX0_P / SATA 0 Receive Data +	DP-I	-	-
A20	SATA0_RX-	SATA_RX0_N / SATA 0 Receive Data -	DP-I	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA_TX2_P / SATA 2 Transmit Data +	DP-O	-	-
A23	SATA2_TX-	SATA_TX2_N / SATA 2 Transmit Data -	DP-O	-	-
A24	SUS_S5#	PM_SLP_S5#	O-3.3	-	-
A25	SATA2_RX+	SATA_RX2_P / SATA 2 Receive Data +	DP-I	-	-
A26	SATA2_RX-	SATA_RX2_N / SATA 2 Receive Data -	DP-I	-	-
A27	BATLOW#	PM_BATLOW# / Battery Low	I-3.3	PU 10k 3.3V (S5)	-
A28	ATA_ACT#	ATA_LED# / SATA LED	OD-3.3	PU 10k 3.3V (S0)	can pull down 6mA max.
A29	AC/HDA_SYNC	HDA_SYNC / HD Audio Sync	O-3.3	PD 1MEG	-
A30	AC/HDA_RST#	HDA_RST# / HD Audio Reset	O-3.3	-	-
A31	GND	Power Ground	PWR	-	-
A32	AC/HDA_BITCLK	HDA_BITCLK / HD Audio Clock	O-3.3	-	-
A33	AC/HDA_SDOUT	HDA_SDOUT / HD Audio Data	O-3.3	-	int. PD 20k in PCH
A34	BIOS_DIS0#	BIOS_DIS0#	I-3.3	PU 10k 3.3V (S5)	-
A35	THRMTRIP#	EXT_THRMTRIP#	O-3.3	PU 10k 3.3V (S0)	-
A36	USB6-	USB6_N / USB Data – Port6	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A37	USB6+	USB6_P / USB Data + Port6	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A38	USB_6_7_OC#	USB_67_OC# / USB OverCurrent Port 6/7	I-3.3	PU 10k 3.3V (S5)	-
A39	USB4- U	SB4_N / USB Data - Port4	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A40	USB4+	USB4_P / USB Data + Port4	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB2_N / USB Data - Port2	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A43	USB2+	USB2_P / USB Data + Port2	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A44	USB_2_3_OC#	USB_23_OC# / USB OverCurrent Port 2/3	I-3.3	PU 10k 3.3V (S5)	-
A45	USB0-	USB0_N / USB Data - Port0	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A46	USB0+	USB0_P / USB Data + Port0	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
A47	VCC_RTC	V_BAT	PWR 3V	-	-
A48	EXCD0_PERST#	EXCD0_PERST#/Express card reset	O-3.3	-	-
A49	EXCD0_CPPE#	EXCD0_CPPE#/ capable c. request	I-3.3	PU 10k 3.3V (S0)	-
A50	LPC_SERIRQ	LPC_SERIRQ / Serial Interrupt Request	I/O-3.3	PU 8k25 3.3V (S0)	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	opt. PCI Express lane 5 + Transmit	Nc	-	just available if PCIe2PATA bridge is not stuffed
A53	PCIE_TX5-	opt. PCI Express lane 5 - Transmit	Nc	-	just available if PCIe2PATA bridge is not stuffed
A54	GPI0	EXT_GPI0 / General Purpose Input 0	I-3.3	PU 10k 3.3V (S0)	-
A55	PCIE_TX4+	PCI Express lane 4 + Transmit	DP-O	-	-
A56	PCIE_TX4-	PCI Express lane 4 - Transmit	DP-O	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 + Transmit	DP-O	-	-
A59	PCIE_TX3-	PCI Express lane 3 - Transmit	DP-O	-	-
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 + Transmit	DP-O	-	-
A62	PCIE_TX2-	PCI Express lane 2 - Transmit	DP-O	-	-
A63	GPI1	EXT_GPI1 / General Purpose Input 1	I-3.3	PU 10k 3.3V (S0)	-
A64	PCIE_TX1+	PCI Express lane 1 + Transmit	DP-O	-	-

A65	PCIE_TX1-	PCI Express lane 1 - Transmit	DP-O	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	EXT_GPI2 / General Purpose Input 2	I-3.3	PU 10k 3.3V (S0)	-
A68	PCIE_TX0+	PCI Express lane 0 + Transmit	DP-O	-	-
A69	PCIE_TX0-	PCI Express lane 0 - Transmit	DP-O	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_A_DATA0_P / LVDS Channel A Data0+	DP-O	-	-
A72	LVDS_A0-	LVDS_A_DATA0_N / LVDS Channel A Data0-	DP-O	-	-
A73	LVDS_A1+	LVDS_A_DATA1_P / LVDS Channel A Data1+	DP-O	-	-
A74	LVDS_A1-	LVDS_A_DATA1_N / LVDS Channel A Data1-	DP-O	-	-
A75	LVDS_A2+	LVDS_A_DATA2_P/ LVDS Channel A Data2+	DP-O	-	-
A76	LVDS_A2-	LVDS_A_DATA2_N / LVDS Channel A Data2 -	DP-O	-	-
A77	LVDS_VDD_EN	LVDS_VDD_EN / LVDS Panel Power Control	O-3.3	PD 100k	-
A78	LVDS_A3+	LVDS_A_DATA3_P / LVDS Channel A Data3+	DP-O	-	-
A79	LVDS_A3-	LVDS_A_DATA3_N / LVDS Channel A Data3-	DP-O	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_A_CLK_P / LVDS Channel A Clock+	DP-O	-	-
A82	LVDS_A_CK-	LVDS_A_CLK_N / LVDS Channel A Clock-	DP-O	-	-
A83	LVDS_I2C_CK	LVDS_DDC_CLK / JILI I2C Clock	I/O-3.3	PU 2k21 3.3V (S0)	-
A84	LVDS_I2C_DAT	LVDS_DDC_DATA / JILI I2C Data	I/O-3.3	PU 2k21 3.3V (S0)	-
A85	GPI3	EXT_GPI3 / General Purpose Input 3	I-3.3	PU 10k 3.3V (S0)	strapping function (if pulled low till release of CB_RESET#, LVDS is disabled to enable eDP)
A86	KBD_RST#	KBD_RST# / Keyboard Reset	I-3.3	PU 10k 3.3V (S0)	-
A87	KBD_A20GATE	KBD_A20GATE	I-3.3	PU 10k 3.3V (S0)	-
A88	PCIE0_CK_REF+	CLK_PCIE_CON_P	DP-O	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_CON_N	DP-O	-	-
A90	GND	Power Ground	PWR	-	-
A91	SPI_POWER	V3.3_SPI_POWER	O-3.3	-	power supply pin for external SPI flash
A92	SPI_MISO	SPI_SO / SPI slave output	I-3.3	-	int. PU 20k in PCH
A93	GPO0	EXT_GPO0 / General Purpose Output 0	O-3.3	PD 10k	-
A94	SPI_CLK	SPI_CLK / SPI clock	O-3.3	-	-
A95	SPI_MOSI	SPI_SI / SPI slave input	O-3.3	-	int. PD 20k in PCH
A96	GND	Power Ground	PWR	-	-
A97	TYPE10#	n.c. for type 2 module	Nc	-	-
A98	RSVD	n.c.	Nc	-	-
A99	RSVD	n.c.	Nc	-	-
A100	GND	Power Ground	PWR	-	-
A101	RSVD	n.c.	Nc	-	-
A102	RSVD	n.c.	Nc	-	-
A103	RSVD	n.c.	Nc	-	-
A104	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
A105	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
A106	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
A107	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
A108	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
A109	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
A110	GND	Power Ground	PWR	-	-

7.3 Connector X1A Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	GBE0_ACT# / Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC_FRAME# / LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC_AD0 / LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in PCH
B5	LPC_AD1	LPC_AD1 / LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in PCH
B6	LPC_AD2	LPC_AD2 / LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in PCH
B7	LPC_AD3	LPC_AD3 / LPC Adress & DATA Bus	I/O-3.3	-	int. PU 20k in PCH
B8	LPC_DRQ0#	LPC_DRQ#0 / LPC Request 0	I-3.3	PU 2k 3.3V (S0)	int. PU 20k in PCH
B9	LPC_DRQ1#	LPC_DRQ#1 / LPC Request 1	I-3.3	PU 2k 3.3V (S0)	int. PU 20k in PCH
B10	LPC_CLK	CLK_LPC_33M_EXT /33MHz LPC clock	O-3.3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	EXT_PWRBTN# / Power Button	I-3.3	PU 10k 3.3V (S5eco)	-
B13	SMB_CK	SMB_CLK_EXT / SMBUS Clock	O-3.3	PU 3k3 3.3V (S5)	-
B14	SMB_DAT	SMB_DATA_EXT / SMBUS Data	I/O-3.3	PU 3k3 3.3V (S5)	-
B15	SMB_ALERT#	SMB_ALERT# / SMBUS Interrupt	I/O-3.3	PU 1k0 3.3V (S5)	-
B16	SATA1_TX+	SATA_TX1_P / SATA 1 Transmit Data +	DP-O	-	-
B17	SATA1_TX-	SATA_TX1_N / SATA 1 Transmit Data -	DP-O	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3.3	-	-
B19	SATA1_RX+	SATA_RX1_P / SATA 1 Receive Data +	DP-I	-	-
B20	SATA1_RX-	SATA_RX1_N / SATA 1 Receive Data -	DP-I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	SATA_TX3_P / SATA 3 Transmit Data +	DP-O	-	-
B23	SATA3_TX-	SATA_TX3_N / SATA 3 Transmit Data -	DP-O	-	-
B24	PWR_OK	EXT_PWR_OK / Power OK	I-3.3	PU 511k 3.3V	pullup voltage depends on ATX or single supply mode / 5V tolerant
B25	SATA3_RX+	SATA_RX3_P / SATA 3 Receive Data +	DP-I	-	-
B26	SATA3_RX-	SATA_RX3_N / SATA 3 Receive Data -	DP-I	-	-
B27	WDT	WDT / Watch Dog Timer	O-3.3	-	-
B28	AC/HDA_SDIN2	HDA_SDIN2_ICH/ HD Audio Serial Input Data 2	I-3.3	-	int. PD 20k in PCH
B29	AC/HDA_SDIN1	HDA_SDIN1_ICH/ HD Audio Serial Input Data 1	I-3.3	-	int. PD 20k in PCH
B30	AC/HDA_SDIN0	HDA_SDIN0_ICH/ HD Audio Serial Input Data 0	I-3.3	-	int. PD 20k in PCH
B31	GND	Power Ground	PWR	-	-
B32	SPKR	HDA_SPKR / Speaker	O-3.3	-	int. PD 20k in PCH
B33	I2C_CK	I2C_CLK_EXT / I2C clock	O-3.3	PU 2k21 3.3V (S5)	-
B34	I2C_DAT	I2C_DATA_EXT / I2C data	I/O-3.3	PU 2k21 3.3V (S5)	-
B35	THRM#	PM_THRM# / Over Temperature	I-3.3	PU 10k 3.3V (S0)	-
B36	USB7-	USB7_N / USB Data – Port7	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B37	USB7+	USB7_P / USB Data + Port7	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B38	USB_4_5_OC#	USB_45_OC# / USB OverCurrent Port 4/5	I-3.3	PU 10k 3.3V (S5)	-
B39	USB5-	USB5_N / USB Data – Port5	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B40	USB5+	USB5_P / USB Data + Port5	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB3_N / USB Data – Port3	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B43	USB3+	USB3_P / USB Data + Port3	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B44	USB_0_1_OC#	USB_01_OC# / USB OverCurrent Port 0/1	I-3.3	PU 10k 3.3V (S5)	-
B45	USB1-	USB1_N / USB Data – Port1	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B46	USB1+	USB1_P / USB Data + Port1	DP-I/O	-	int. PD 15k in PCH / 5V tolerant
B47	EXCD1_PERST#	EXCD1_PERST# / Express card reset	O-3.3	-	-
B48	EXCD1_CPPE#	EXCD1_CPPE# / capable c. request	I-3.3	PU 10k 3.3V (S0)	-
B49	SYS_RESET#	EXT_SYS_RESET# / Reset Input	I-3.3	PU 10k 3.3V (S5)	-
B50	CB_RESET#	CB_RESET# / Carrier board Reset	O-3.3	PU 10k 3.3V (S5)	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	opt. PCI Express lane 5 + receive	Nc	-	just available if PCIe2PATA bridge is not stuffed
B53	PCIE_RX5-	opt. PCI Express lane 5 - receive	Nc	-	just available if PCIe2PATA bridge is not stuffed
B54	GPO1	EXT_GPO1 / General Purpose Output 1	O-3.3	PD 10k	-
B55	PCIE_RX4+	PCI Express lane 4 + receive	DP-I	-	-
B56	PCIE_RX4-	PCI Express lane 4 - receive	DP-I	-	-
B57	GPO2	EXT_GPO2 / General Purpose Output 2	O-3.3	PD 10k	-
B58	PCIE_RX3+	PCI Express lane 3 + receive	DP-I	-	-
B59	PCIE_RX3-	PCI Express lane 3 - receive	DP-I	-	-
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCI Express lane 2 + receive	DP-I	-	-
B62	PCIE_RX2-	PCI Express lane 2 - receive	DP-I	-	-
B63	GPO3	EXT_GPO3 / General Purpose Output 3	O-3.3	PD 10k	-

B64	PCIE_RX1+	PCI Express lane 1 + receive	DP-I	-	-
B65	PCIE_RX1-	PCI Express lane 1 - receive	DP-I	-	-
B66	WAKE0#	PCIE_WAKE#	I/O-3.3	PU 1k2 3.3V (S5)	-
B67	WAKE1#	WAKE1#	I-3.3	PU 10k 3.3V (S5)	-
B68	PCIE_RX0+	PCI Express lane 0 + receive	DP-I	-	-
B69	PCIE_RX0-	PCI Express lane 0 - receive	DP-I	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_B_DATA0_P / LVDS Channel B Data0+	DP-O	-	-
B72	LVDS_B0-	LVDS_B_DATA0_N / LVDS Channel B Data0-	DP-O	-	-
B73	LVDS_B1+	LVDS_B_DATA1_P / LVDS Channel B Data1+	DP-O	-	-
B74	LVDS_B1-	LVDS_B_DATA1_N / LVDS Channel B Data1-	DP-O	-	-
B75	LVDS_B2+	LVDS_B_DATA2_P/ LVDS Channel B Data2+	DP-O	-	-
B76	LVDS_B2-	LVDS_B_DATA2_N / LVDS Channel B Data2 -	DP-O	-	-
B77	LVDS_B3+	LVDS_B_DATA3_P / LVDS Channel B Data3+	DP-O	-	-
B78	LVDS_B3-	LVDS_B_DATA3_N / LVDS Channel B Data3-	DP-O	-	-
B79	LVDS_BKLT_EN	LVDS_BKLT_CTRL / Panel Backlight ON	O-3.3	PD 100k	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_B_CLK_P / LVDS Channel B Clock+	DP-O	-	-
B82	LVDS_B_CK-	LVDS_B_CLK_N / LVDS Channel B Clock-	DP-O	-	-
B83	LVDS_BKLT_CTRL	LVDS_BKLT_CTRL / Backlight Brightness Contr.	O-3.3	-	-
B84	VCC_5V_SBY	+V_STBY_ETX / 5V Standby	PWR 5V (S5)	-	optional (not neccessary in single supply mode)
B85	VCC_5V_SBY	+V_STBY_ETX / 5V Standby	PWR 5V (S5)	-	optional (not neccessary in single supply mode)
B86	VCC_5V_SBY	+V_STBY_ETX / 5V Standby	PWR 5V (S5)	-	optional (not neccessary in single supply mode)
B87	VCC_5V_SBY	+V_STBY_ETX / 5V Standby	PWR 5V (S5)	-	optional (not neccessary in single supply mode)
B88	BIOS_DIS1#	BIOS_DIS1#	I-3.3	PU 10k 3.3V (S5)	-
B89	VGA_RED	CRT_RED / Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	CRT_GREEN / Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	CRT_BLUE / Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	CRT_HSYNC / Analog Video H-Sync	O-3.3	-	-
B94	VGA_VSYNC	CRT_VSYNC / Analog Video V-Sync	O-3.3	-	-
B95	VGA_I2C_CK	CRT_DDC_CLK / Display Data Channel Clock	I/O-3.3	PU 1k1 3.3V (S0)	-
B96	VGA_I2C_DAT	CRT_DDC_DATA / Display Data Channel Data	I/O-3.3	PU 1k1 3.3V (S0)	-
B97	SPI_CS#	SPI_CS# / SPI chip select	O-3.3	-	-
B98	RSVD	n. c.	nc	-	-
B99	RSVD	n. c.	nc	-	-
B100	GND	Power Ground	PWR	-	-
B101	RSVD	n. c.	nc	-	optional FAN_PWM signal (O-3.3) like in type 6 pinout
B102	RSVD	n. c.	nc	-	optional FAN_TACH signal (I-3.3) like in type 6 pinout
B103	RSVD	n. c.	nc	-	-
B104	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
B105	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
B106	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
B107	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
B108	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
B109	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
B110	GND	Power Ground	PWR	-	-

7.4 Connector X1B Row C

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	-	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I-5T	PU 4k7 3.3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-3.3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3.3	PU 20k 3.3V (S5)	+ int. PU 20k in PCH
C16	PCI_GNT2#	PCI Bus Grant 2	O-3.3	-	-
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 3.3V (S0)	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3.3	-	-
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 3.3V (S0)	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3.3	-	-
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-5T	PU 8k2 3.3V (S0)	-
C23	PCI_RST#	PCI Bus Reset	O-3.3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	I/O-5T	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	I/O-5T	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	I/O-5T	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	I/O-5T	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	I/O-5T	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	I/O-5T	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	I/O-5T	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	I/O-5T	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	I/O-5T	-	-
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 3.3V (S0)	-
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 3.3V (S0)	-
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 3.3V (S0)	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	I/O-5T	PU 8k2 3.3V (S0)	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	I/O-5T	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	I/O-5T	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	I/O-5T	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O-5T	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 3.3V (S0)	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 3.3V (S0)	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIexpress Graphics Receive + (0)	DP-I	-	-
C53	PEG_RX0-	PCIexpress Graphics Receive - (0)	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	PCIexpress Graphics Receive + (1)	DP-I	-	-
C56	PEG_RX1-	PCIexpress Graphics Receive - (1)	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	PCIexpress Graphics Receive + (2)	DP-I	-	-
C59	PEG_RX2-	PCIexpress Graphics Receive - (2)	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIexpress Graphics Receive + (3)	DP-I	-	-
C62	PEG_RX3-	PCIexpress Graphics Receive - (3)	DP-I	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-

C65	PEG_RX4+	PCIexpress Graphics Receive + (4)	DP-I	-	-
C66	PEG_RX4-	PCIexpress Graphics Receive - (4)	DP-I	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	PCIexpress Graphics Receive + (5)	DP-I	-	-
C69	PEG_RX5-	PCIexpress Graphics Receive - (5)	DP-I	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIexpress Graphics Receive + (6)	DP-I	-	-
C72	PEG_RX6-	PCIexpress Graphics Receive - (6)	DP-I	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3.3	-	opt. PU 2k21 3.3V (S0) = enable SDVO/DP B interface
C74	PEG_RX7+	PCIexpress Graphics Receive + (7)	DP-I	-	-
C75	PEG_RX7-	PCIexpress Graphics Receive - (7)	DP-I	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	PCIexpress Graphics Receive + (8)	DP-I	-	-
C79	PEG_RX8-	PCIexpress Graphics Receive - (8)	DP-I	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIexpress Graphics Receive + (9)	DP-I	-	-
C82	PEG_RX9-	PCIexpress Graphics Receive - (9)	DP-I	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIexpress Graphics Receive + (10)	DP-I	-	-
C86	PEG_RX10-	PCIexpress Graphics Receive - (10)	DP-I	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIexpress Graphics Receive + (11)	DP-I	-	-
C89	PEG_RX11-	PCIexpress Graphics Receive – (11)	DP-I	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIexpress Graphics Receive + (12)	DP-I	-	-
C92	PEG_RX12-	PCIexpress Graphics Receive - (12)	DP-I	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIexpress Graphics Receive + (13)	DP-I	-	-
C95	PEG_RX13-	PCIexpress Graphics Receive - (13)	DP-I	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	DPD_CTRL_CLK	I/O-3.3	-	-
C98	PEG_RX14+	PCIexpress Graphics Receive + (14)	DP-I	-	-
C99	PEG_RX14-	PCIexpress Graphics Receive - (14)	DP-I	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIexpress Graphics Receive + (15)	DP-I	-	-
C102	PEG_RX15-	PCIexpress Graphics Receive - (15)	DP-I	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
C105	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
C106	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
C107	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
C108	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
C109	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
C110	GND	Power Ground	PWR	-	-

7.5 Connector X1B Row D

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	PD 5k62	-
D9	IDE_IOW#	IDE IO Write	O-3.3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3.3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k	-
D13	IDE_A0	IDE Adress Bus	O-3.3	-	-
D14	IDE_A1	IDE Adress Bus	O-3.3	-	-
D15	IDE_A2	IDE Adress Bus	O-3.3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3.3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3.3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3.3	PU 10k 3.3V (S0)	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3.3	-	-
D20	PCI_REQ3#	PCI Bus Reqest 0	I-5T	PU 8k2 3.3V (S0)	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	-
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 3.3V (S0)	-
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 3.3V (S0)	-
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 3.3V (S0)	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 3.3V (S0)	-
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 3.3V (S0)	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 3.3V (S0)	-
D48	PCI_CLKRUN#	PCI Clock Run	I-5T	PU 8k25 3.3V (S0)	-
D49	PCI_M66EN	PCI 66MHz enable	I-5T	PD 1k	-
D50	PCI_CLK	CLK_PCI_33M_EXT / PCI Clock 33MHz	O-3.3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIexpress Graphics Transmit + (0)	DP-O	-	-
D53	PEG_TX0-	PCIexpress Graphics Transmit - (0)	DP-O	-	-
D54	PEG_LANE_RV#	PCIexpress Graphics Lane Reversal	I-3.3	PU 10k 3.3V (S0)	-
D55	PEG_TX1+	PCIexpress Graphics Transmit + (1)	DP-O	-	-
D56	PEG_TX1-	PCIexpress Graphics Transmit - (1)	DP-O	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	PCIexpress Graphics Transmit + (2)	DP-O	-	-
D59	PEG_TX2-	PCIexpress Graphics Transmit - (2)	DP-O	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	PCIexpress Graphics Transmit + (3)	DP-O	-	-
D62	PEG_TX3-	PCIexpress Graphics Transmit - (3)	DP-O	-	-
D63	RSVD	DPC_CTRL_CLK	I/O-3.3	-	-
D64	RSVD	DPC_CTRL_DATA	I/O-3.3	-	int. PD 20k in PCH / opt. PU 2k21 3.3V (S0) = enable DP C interface

D65	PEG_TX4+	PCIexpress Graphics Transmit + (4)	DP-O	-	-
D66	PEG_TX4-	PCIexpress Graphics Transmit - (4)	DP-O	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIexpress Graphics Transmit + (5)	DP-O	-	-
D69	PEG_TX5-	PCIexpress Graphics Transmit - (5)	DP-O	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIexpress Graphics Transmit + (6)	DP-O	-	-
D72	PEG_TX6-	PCIexpress Graphics Transmit - (6)	DP-O	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	I/O-3.3	-	-
D74	PEG_TX7+	PCIexpress Graphics Transmit + (7)	DP-O	-	-
D75	PEG_TX7-	PCIexpress Graphics Transmit - (7)	DP-O	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# / IDE cable type detect	I/O-3.3	PD 100k	-
D78	PEG_TX8+	PCIexpress Graphics Transmit + (8)	DP-O	-	-
D79	PEG_TX8-	PCIexpress Graphics Transmit - (8)	DP-O	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIexpress Graphics Transmit + (9)	DP-O	-	-
D82	PEG_TX9-	PCIexpress Graphics Transmit - (9)	DP-O	-	-
D83	RSVD	DPD_CTRL_DATA	I/O-3.3	-	int. PD 20k in PCH / opt. PU 2k21 3.3V (S0) = enable DP D interface
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIexpress Graphics Transmit + (10)	DP-O	-	-
D86	PEG_TX10-	PCIexpress Graphics Transmit - (10)	DP-O	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	PCIexpress Graphics Transmit + (11)	DP-O	-	-
D89	PEG_TX11-	PCIexpress Graphics Transmit - (11)	DP-O	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	PCIexpress Graphics Transmit + (12)	DP-O	-	-
D92	PEG_TX12-	PCIexpress Graphics Transmit - (12)	DP-O	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIexpress Graphics Transmit + (13)	DP-O	-	-
D95	PEG_TX13-	PCIexpress Graphics Transmit - (13)	DP-O	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	PCIexpress Graphics Enable	I-3.3	PU 10k 3.3V (S0)	-
D98	PEG_TX14+	PCIexpress Graphics Transmit + (14)	DP-O	-	-
D99	PEG_TX14-	PCIexpress Graphics Transmit - (14)	DP-O	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIexpress Graphics Transmit + (15)	DP-O	-	-
D102	PEG_TX15-	PCIexpress Graphics Transmit - (15)	DP-O	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
D105	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
D106	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
D107	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
D108	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
D109	VCC_12V	main input voltage (8.5-20V)	PWR 8.5-20V	-	-
D110	GND	Power Ground	PWR	-	-

The termination resistors in these tables are already mounted on the module. Refer to the design guide for information about additional termination resistors.

8 BIOS Operation

The module is equipped with AMI® Aptio, which is located in an onboard SPI serial flash memory.

8.1 Determining the BIOS Version

The AMI® Aptio version is displayed in the main menu of the setup utility.

» BIOS Vendor: American Megatrends

» Core Version: x.x.x.x

» BIOS Date: mm/dd/yyyy hh:mm:ss

» BIOS Version: CCR2RXXX

8.2 BIOS Update

Kontron provides continuous BIOS updates for Computer-on-Modules. The updates are provided for download on http://emdcustomersection.kontron.com with a detailed change description within the according Product Change Notification (PCN). Please register for EMD Customer Section to get access to BIOS downloads and PCN service.

Modules with BIOS Region/Setup only inside the flash can be updated with AFU utilities (usually 1-3MB BIOS binary file size) directly. Modules with Intel® Management Engine, Ethernet, Flash Descriptor and other options additionally to the BIOS Region (usually 4-8MB BIOS binary file size) requires a different update process with Intel Flash Utility FPT and a wrapper to backup and restore configurations and the MAC address. Therefore it is strongly recommended to use the batch file inside the BIOS download package available on EMD Customer Section.

» Boot the module to DOS/EFI Shell with access to the BIOS image and Firmware Update Utility provided on EMD Customer Section

» Execute Flash.bat in DOS or Flash.nsh in EFI Shell

Any modification of the update process may damage your module!

Backup the BIOS / Create a BIOS with custom defaults:

» Change your BIOS settings according your needs

» Save and Exit Setup with option “Save as User Defaults”. Your customized settings are now stored inside the flash in a second area additional to the manufacturer defaults

» Boot the module to DOS or EFI Shell with access to the update utilities

» Extract the BIOS region including your custom defaults with **afuefix64.efi CBIOS.bin /O** in EFI Shell or **afudos.exe CBIOS.rom /O** in DOS

Now you can clone the BIOS with your customized default settings to other modules or external SPI flashes with above mention AFU utilites. On modules with Management Engine and Ethernet inside the Flash the same BIOS core version should already be programmed on the target.

AMI APTIO update utilities for DOS, EFI Shell and Windows are available for free at AMI.com:
http://www.ami.com/support/downloads/amiflash.zip

8.3 Setup Guide

The Aptio Setup Utility changes system behavior by modifying the Firmware configuration. The setup program uses a number of menus to make changes and turn features on or off.

Functional keystrokes in POST:

Key	Function
DEL	Enter Setup
F2	Enter Setup
F7	Boot Menu

8.4 POST Codes

Important POST codes during boot-up

AB	BIOS Setup
AD	EFI Shell
AE	Windows

8.4.1 Start AMI® Aptio Setup Utility

To start the AMI® BIOS setup utility, press <DEL> or <F2> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
+/-	Change Option
<Enter>	Execute command or select submenu.
<F1>	General Help window.
<F2>	Previous Values
<F3>	Load the optimized default configuration.
<F4>	Save and exit.
<Esc>	Exit menu.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (►) marks all submenus.

Item Specific Help Window

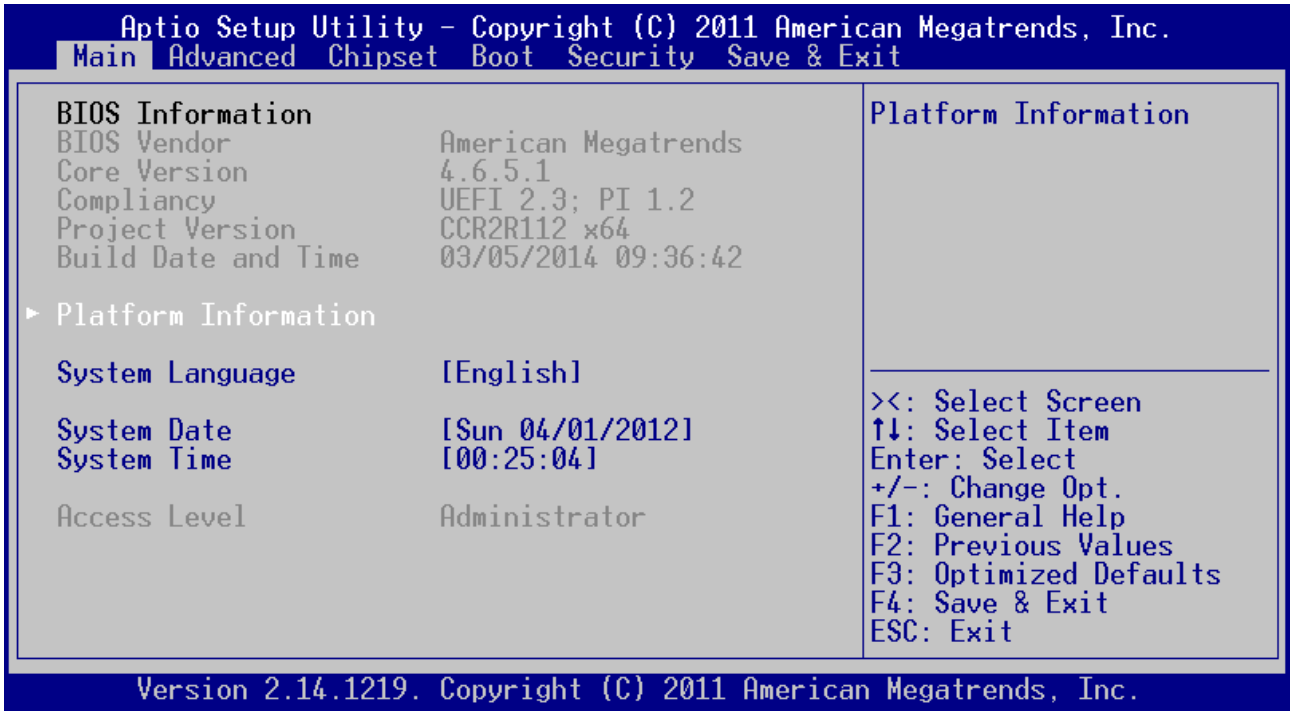
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

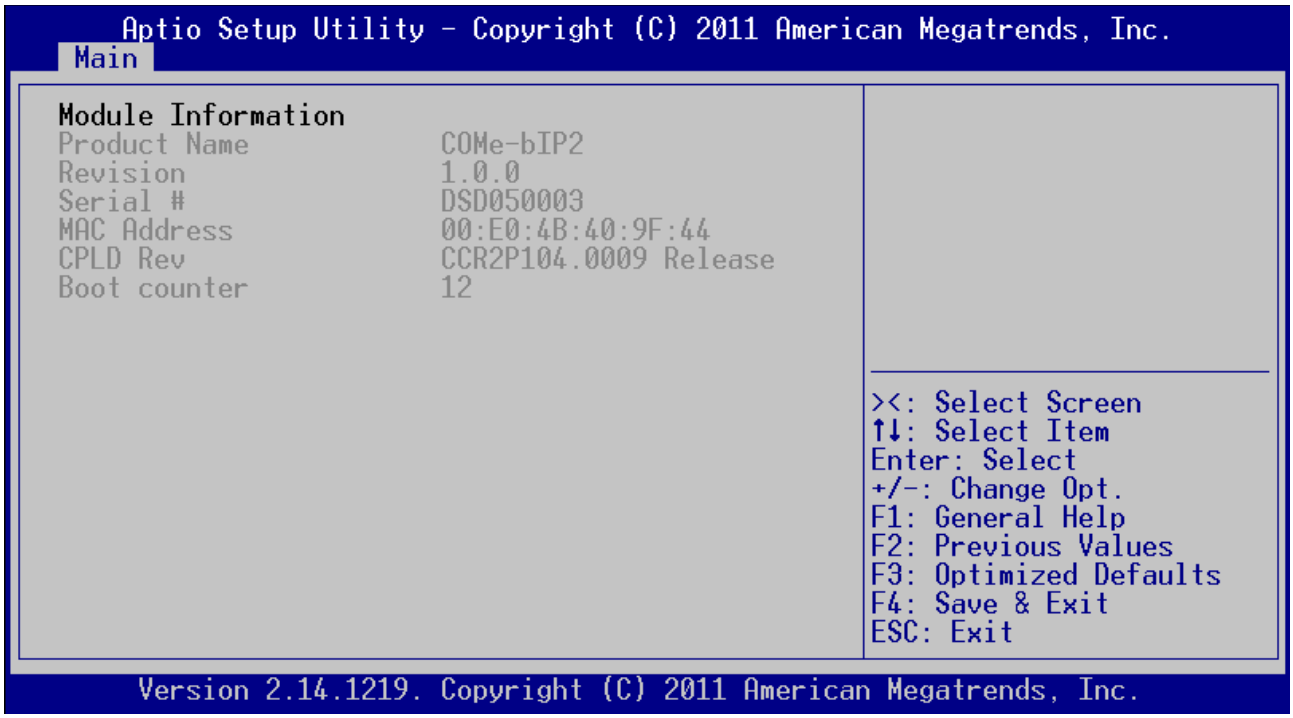
8.5 BIOS Setup

8.5.1 Main

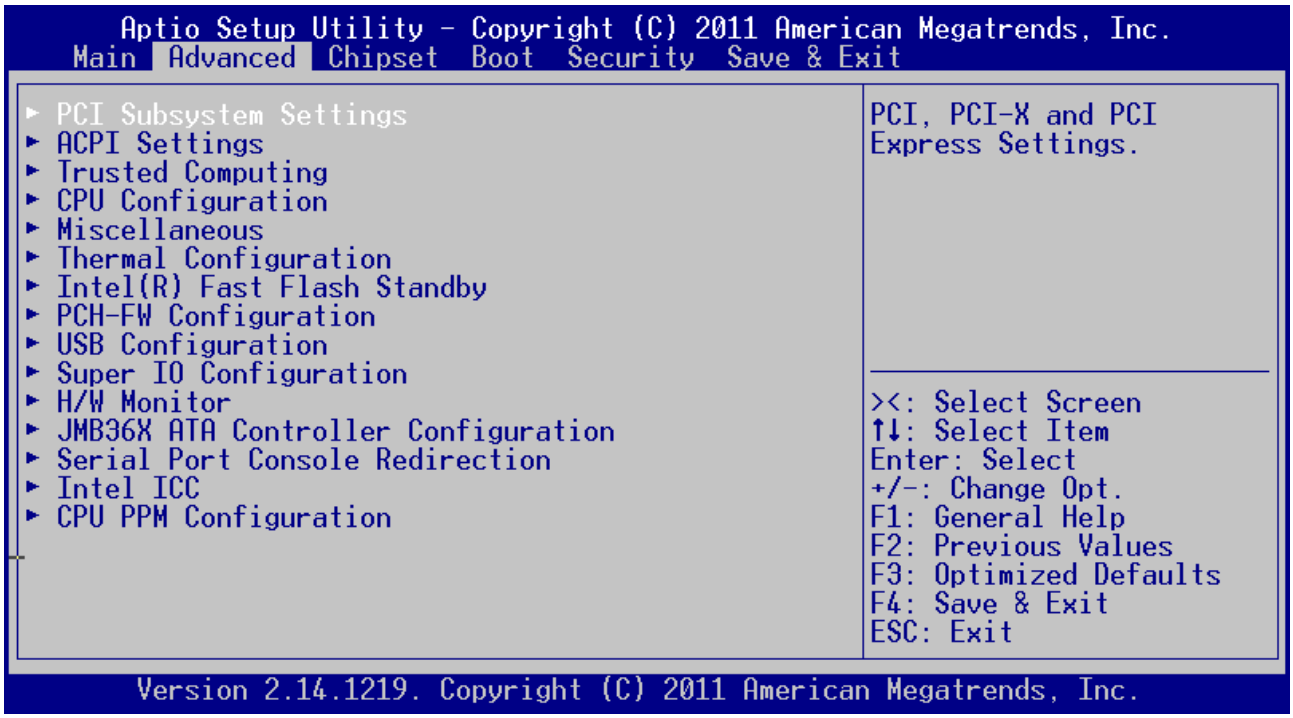


Feature	Options	Description
System Language	**English**	Choose the system default language
System Date	[mm/dd/yyyy]	Set the Date. Use 'Tab' to switch between Date elements
System Time	[hh:mm:ss]	Set the Time. Use 'Tab' to switch between Time elements

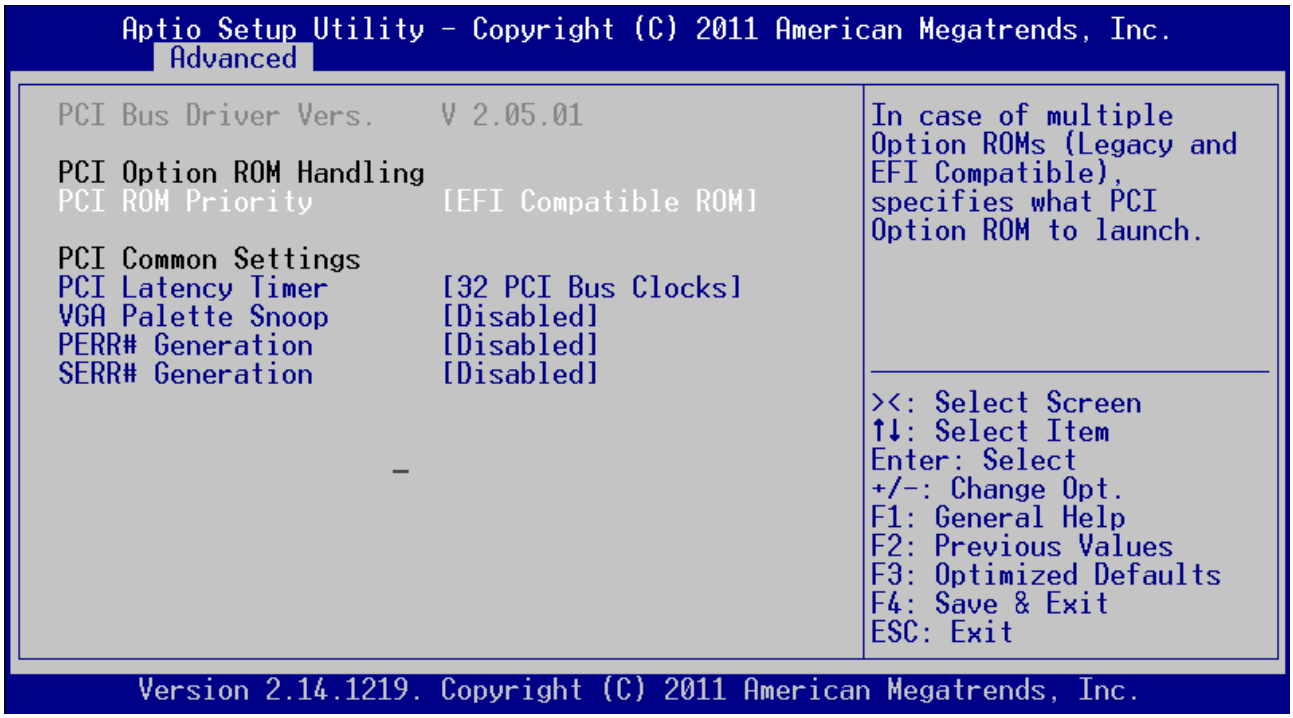
Platform Information



8.5.2 Advanced

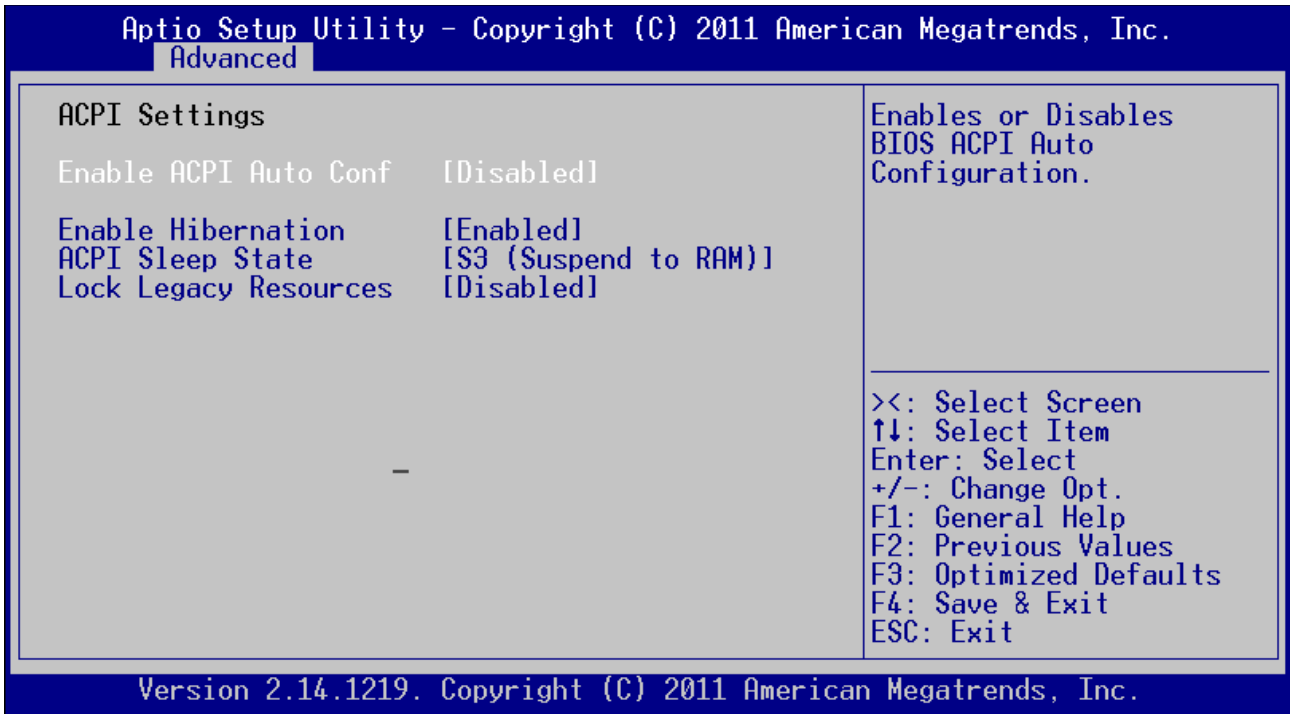


PCI Subsystem Settings



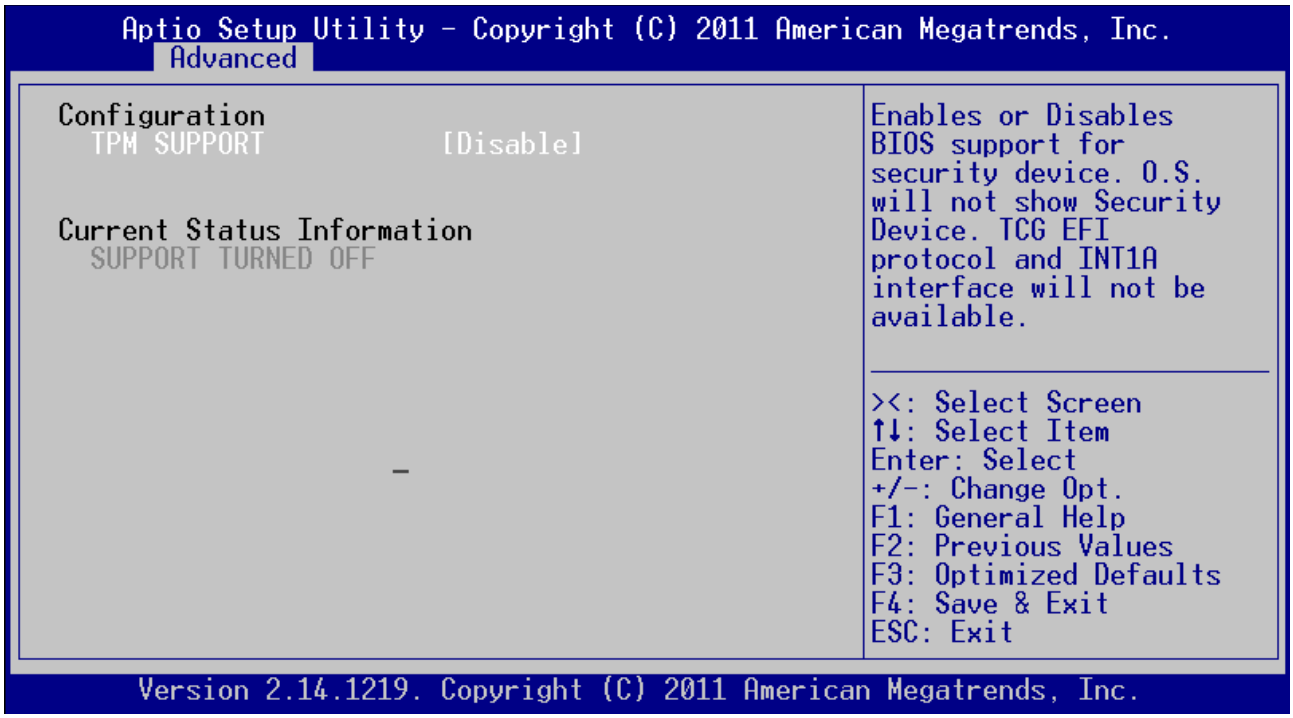
Feature	Options	Description
PCI ROM Priority	Legacy ROM **EFI Compatible ROM**	In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch
PCI Latency Timer	**32** ... 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA Palette Registers Snooping
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate PERR#
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate SERR#

ACPI Settings



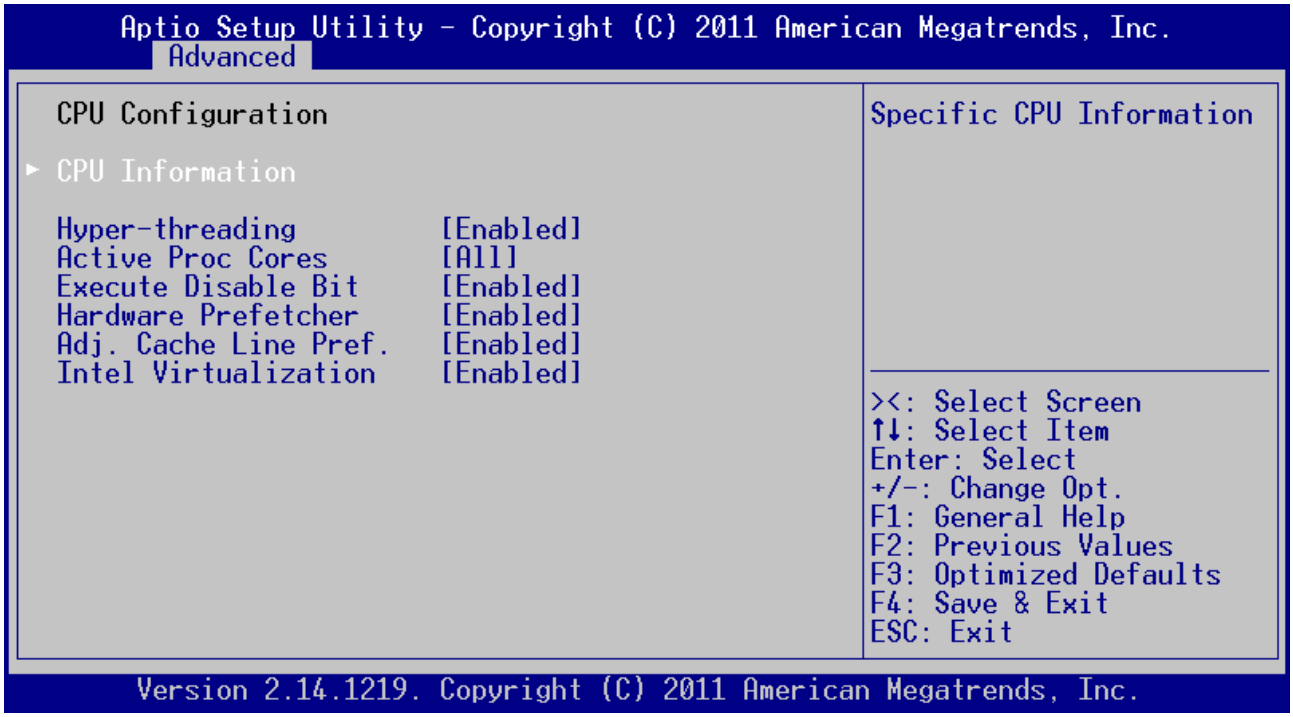
Feature	Options	Description
Enable ACPI Auto Congiguration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State)
ACPI Sleep State	Suspend Disabled **S3 (StR)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed
Lock Legacy Ressources	**Disabled** Enabled	Enables or Disables Lock of Legacy Ressources

Trusted Computing



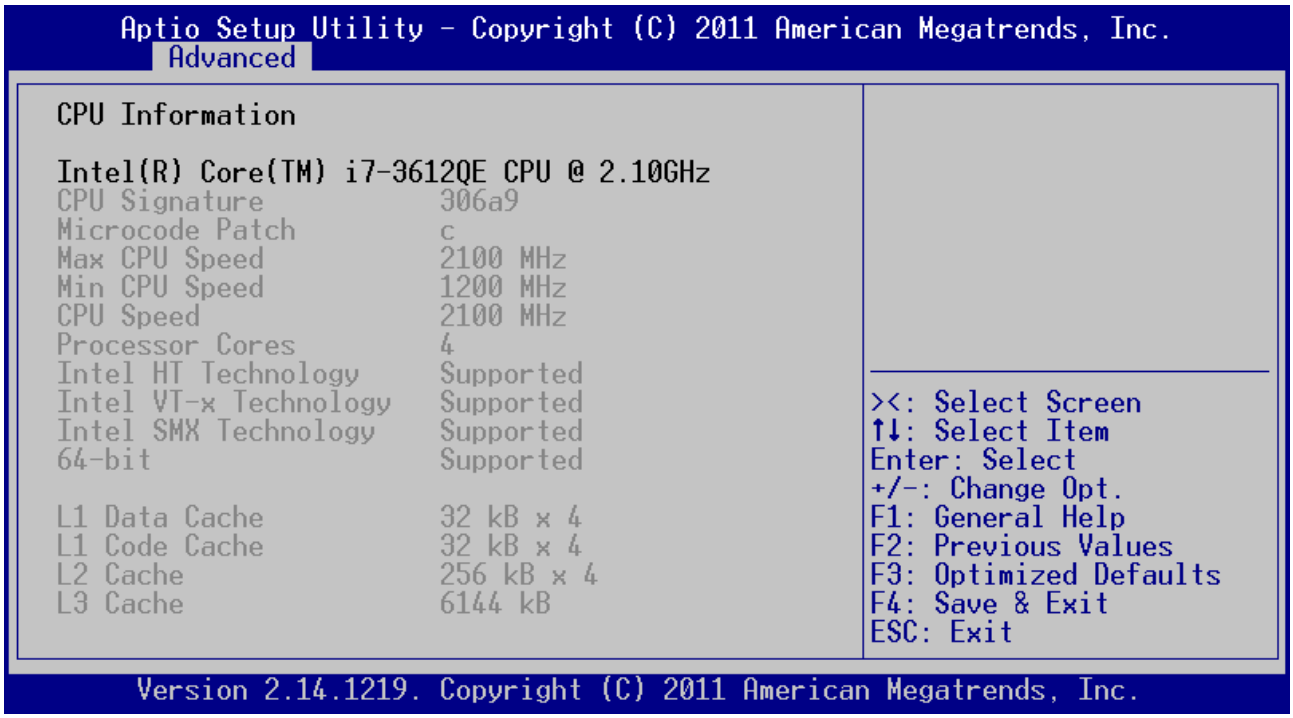
Feature	Options	Description
TPM Support	**Disable** Enable	Enables or Disables TPM support. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available
TPM State	**Disabled** Enabled	Enable/Disable Security Device. Note: Your Computer will reboot during restart in order to change Sate of the Device
Pending Operation	**None** Enable Take Ownership Disable Take Ownership TPM Clear	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change Sate of the Device

CPU Configuration

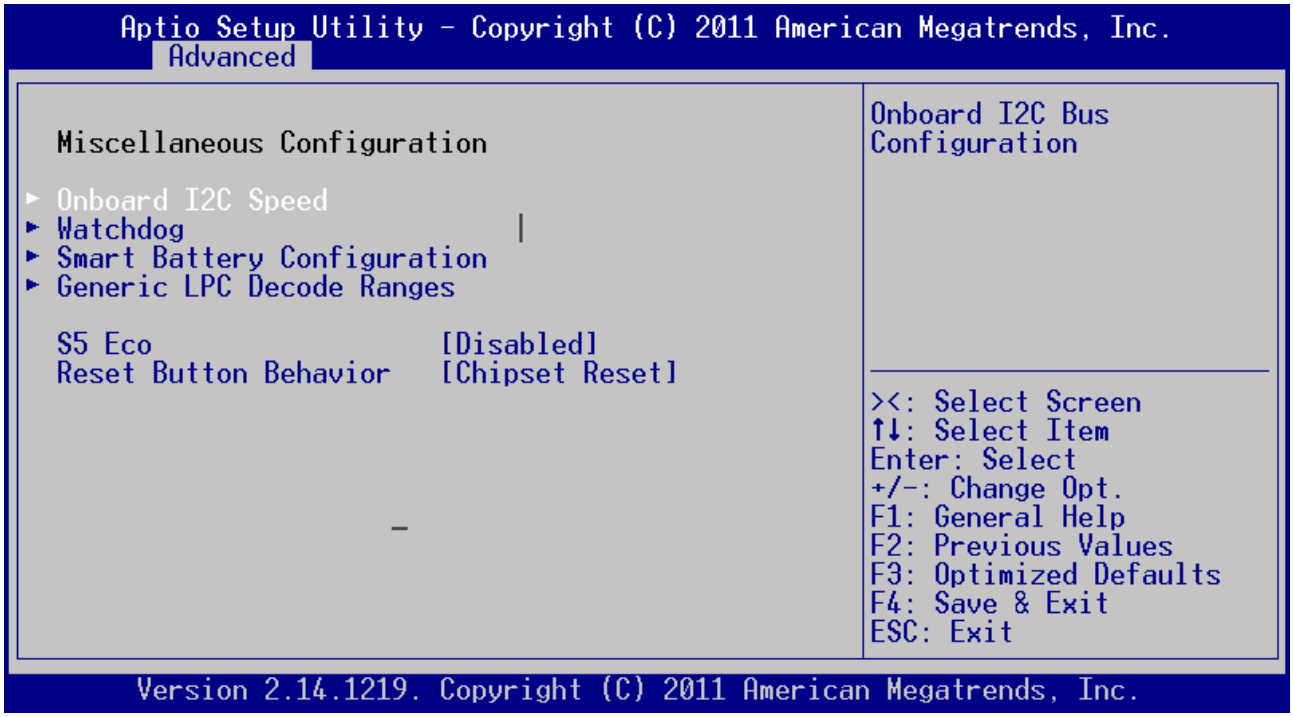


Feature	Options	Description
Hyper-Threading	Disabled **Enabled**	Enables/Disables the Intel® Hyper Threading Technology HTT supported by Core i7/i5
Active Proc Cores	**All** 1 2 3	Number of cores to enable in each processors package
Execute Disable Bit	Disabled **Enabled**	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS
Hardware Prefetcher	Disabled **Enabled**	Turn on/off the MLC streamer prefetcher
Adj. Cache Line Pref.	Disabled **Enabled**	Turn on/off prefetching of adjacent cache lines
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

CPU Information

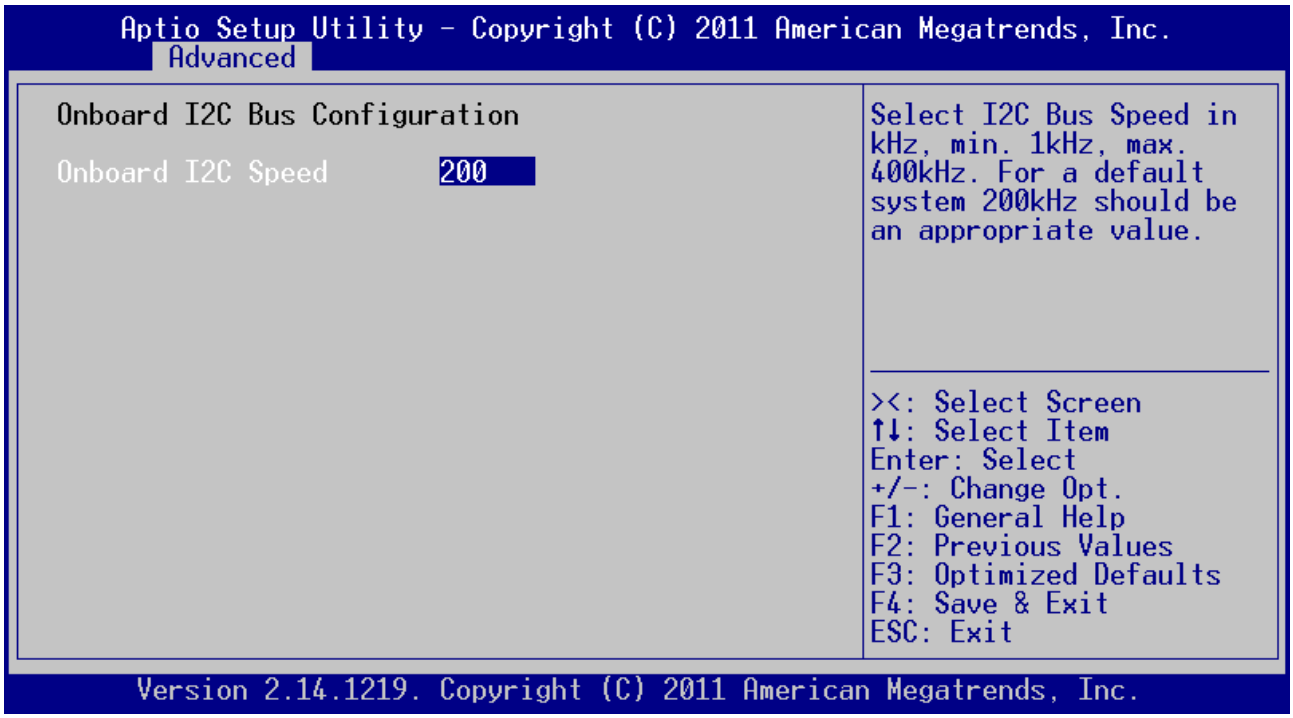


Miscellaneous



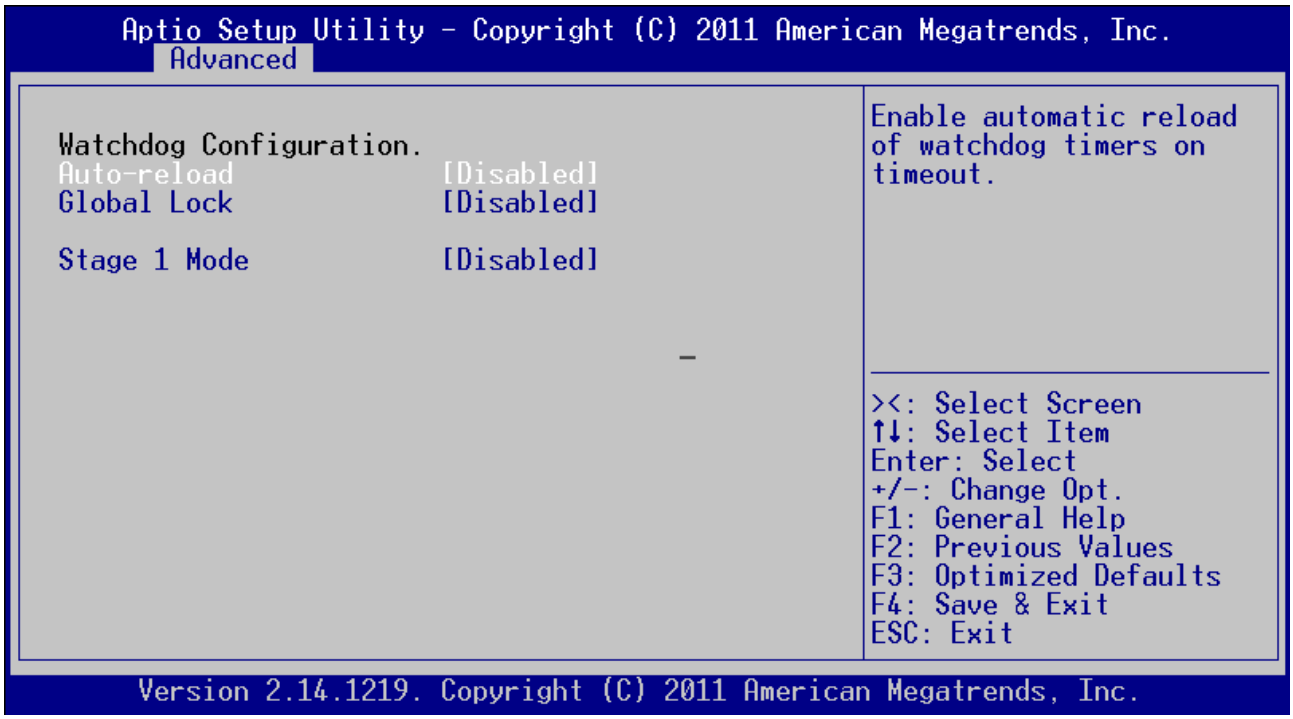
Feature	Options	Description
S5 Eco	**Disabled** Enabled	Reduce supply current in Soft Off State S5 to less than 1mA. If enabled, power button is the only wakeup source in S5. See chapter S5 Eco for more details
Reset Button Behavior	**Chipset Reset** Power Cycle	Select the behavior of Reset Button. Select Power Cycle to hold the module in reset while reset button is pressed

Onboard I2C Bus Configuration



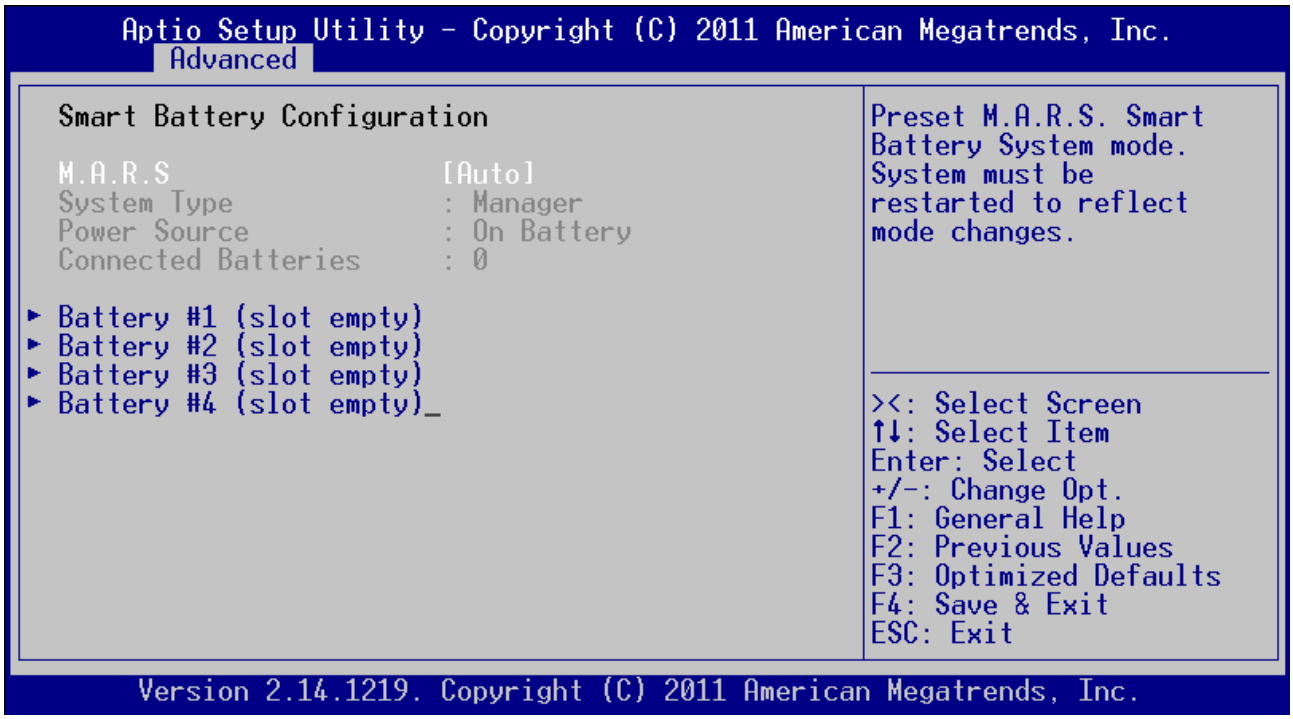
Feature	Options	Description
Onboard I2C Speed	1 ... **200** ... 400	Select I2C Bus Speed in kHz, min. 1kHz, max 400kHz

Watchdog



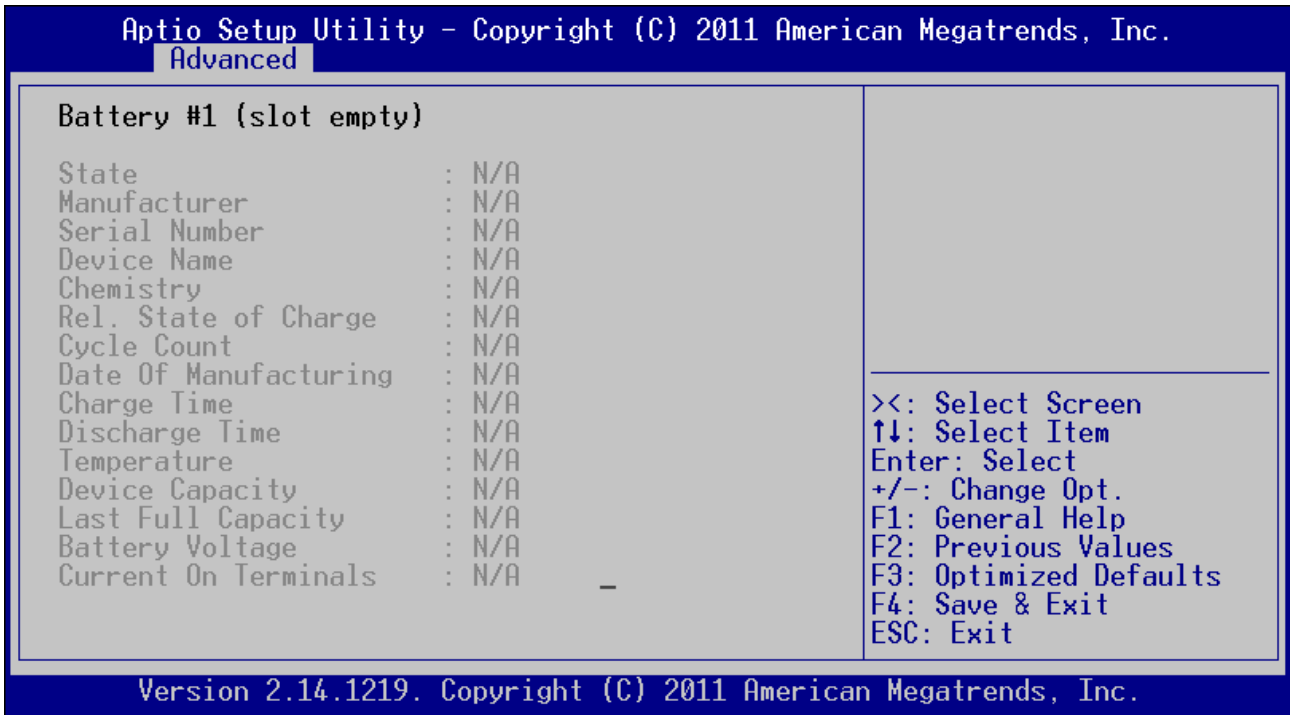
Feature	Options	Description
Auto-reload	**Disabled** Enabled	Enable automatic reload of watchdog timers on timeout
Global Lock	**Disabled** Enabled	If set to enabled, all Watchdog registers (except WD_KICK) become read only until the board is reset
Stage 1 Mode	**Disabled** Reset NMI SCI Delay WDT Signal only	Select Action for first Watchdog stage
- Assert WDT Signal	**Disabled** Enabled	Enable/Disable assertion of WDT signal to baseboard on stage timeout
- Stage 1 Timout	1s 5s 10s **30s** 1m 3m 10m 30m	Select Timeout value for first watchdog stage
Stage 2 Mode	**Disabled** Reset NMI SCI WDT Signal only	Select Action for second Watchdog stage
- Assert WDT Signal	**Disabled** Enabled	Enable/Disable assertion of WDT signal to baseboard on stage timeout
- Stage 2 Timout	1s 5s 10s **30s** 1m 3m 10m 30m	Select Timeout value for second watchdog stage

Smart Battery Configuration

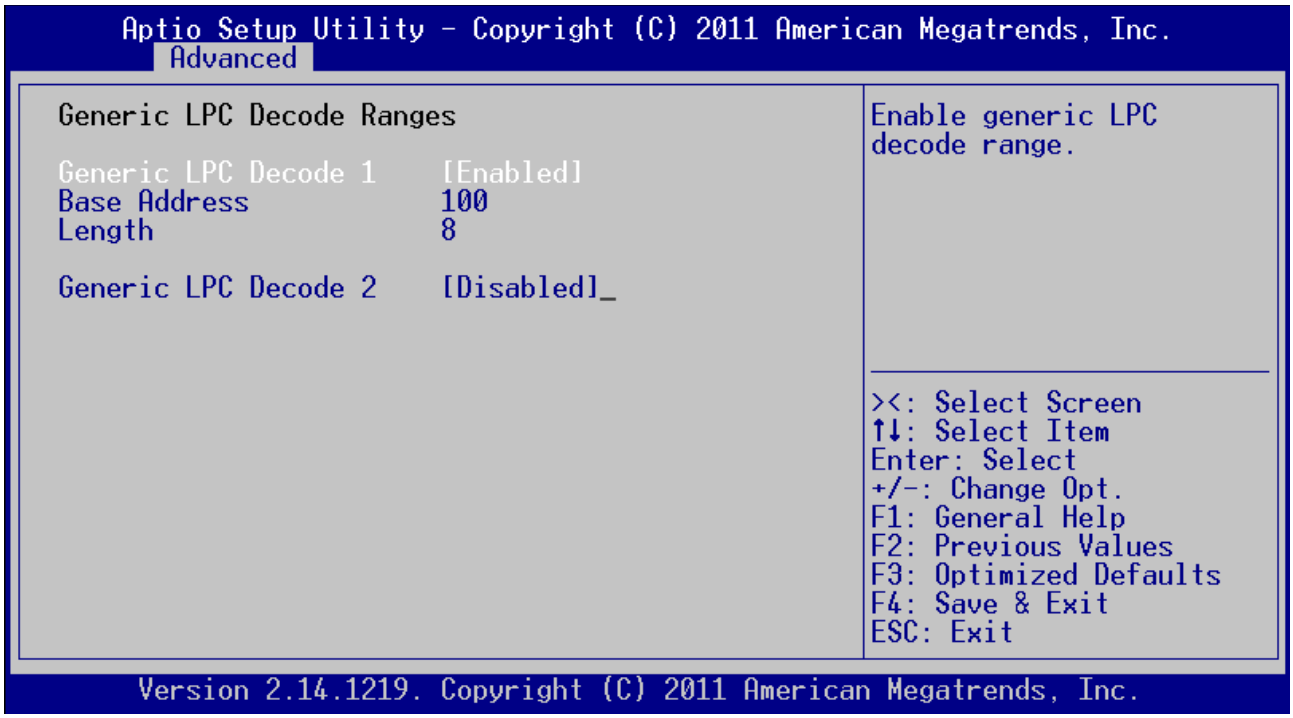


Feature	Options	Description
M.A.R.S.	Disabled **AUTO** Charger Manager	Preset M.A.R.S. Smart Battery System mode. System must be restarted to reflect mode changes

Battery Information

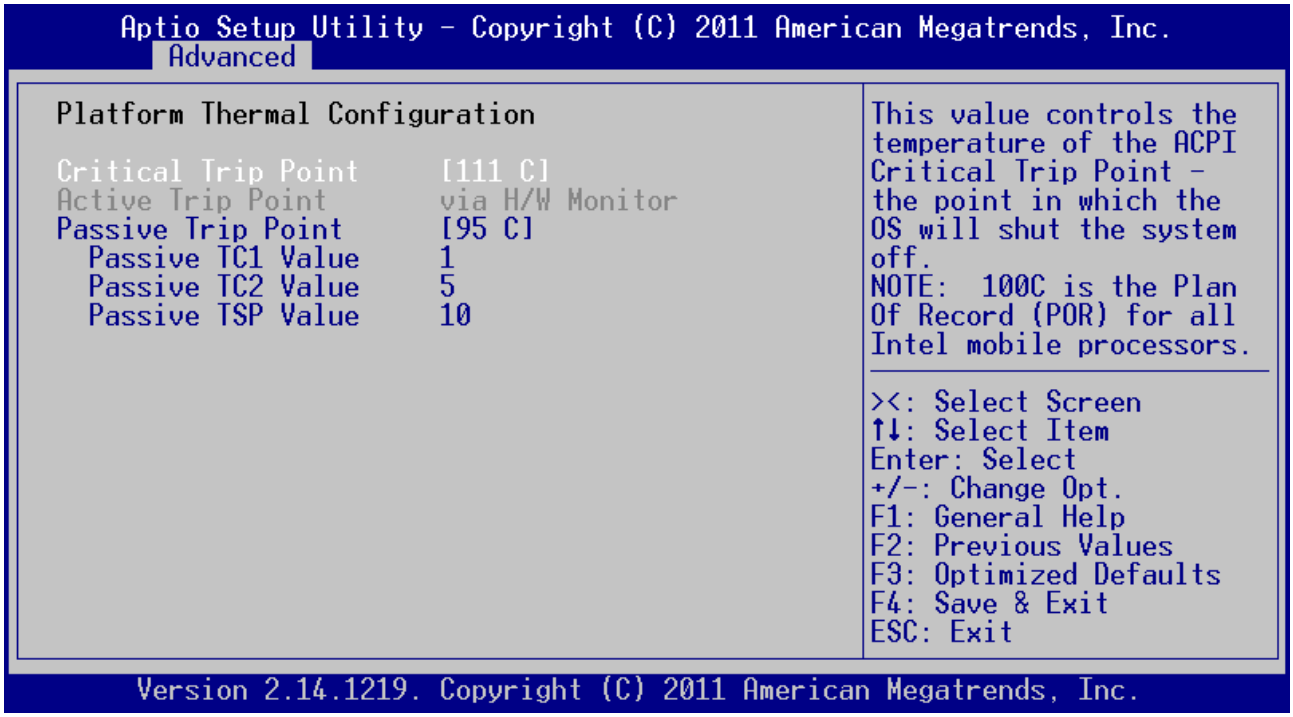


Generic LPC Decode Ranges



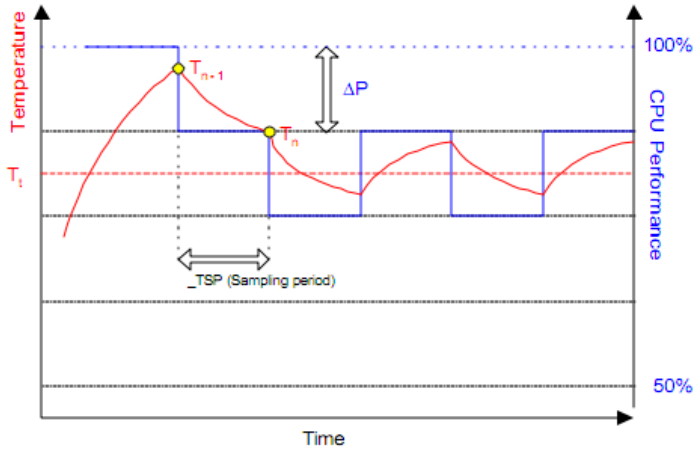
Feature	Options	Description
Generic LPC Decode 1	**Disabled** Enabled	Enable generic LPC decode range
- Base Address	**0100h**	Base address of the generic decode range. Valid between 0100h - FFF0h. Must be 8-byte alligned
- Length	**0008h**	Length of the generic decode range. Valid between 0800h - 0100h. Must be multiple of 8.
Generic LPC Decode 2	**Disabled** Enabled	Enable generic LPC decode range
- Base Address	**0100h**	Base address of the generic decode range. Valid between 0100h - FFF0h. Must be 8-byte alligned
- Length	**0008h**	Length of the generic decode range. Valid between 0800h - 0100h. Must be multiple of 8.

Thermal Configuration



Feature	Options	Description
Critical Trip Point	**111°C** 15°C ... 119°C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off. Note: 100°C is the Plan Of Record (POR) for all Intel mobile processors
Passive Trip Point	Disabled 15°C ... **95°C** ... 119°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor
- Passive TC1 Value	**1**	This value sets the TC1 value for the ACPI Passive Cooling Formula. Range 1 - 16
- Passive TC2 Value	**5**	This value sets the TC2 value for the ACPI Passive Cooling Formula. Range 1 - 16
- Passive TSP Value	**10**	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenth of a second how often the OS will read the temperature when passive cooling is enabled. Range 2 - 32

Passive Cooling



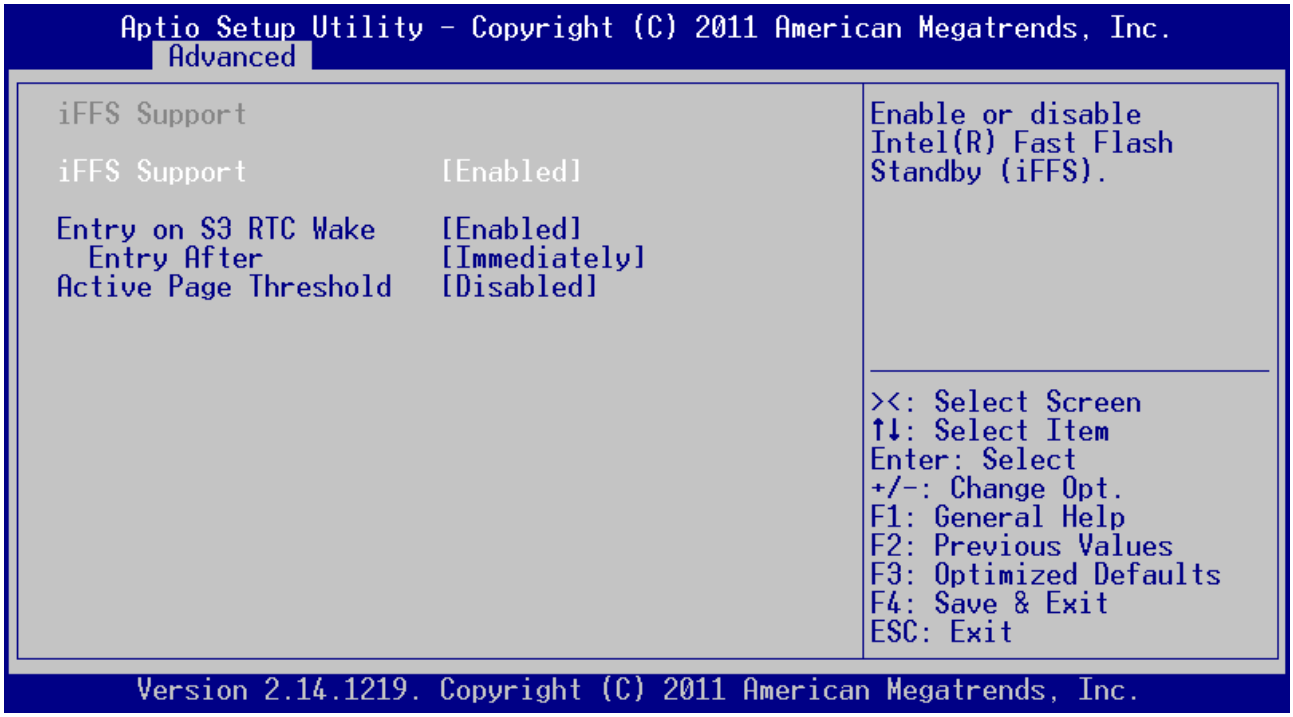
The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation

ΔP[%] = TC1(Tn-Tn-1) + TC2(Tn-Tt)

ΔP is the performance delta, Tt is the target temperature = passive cooling trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply. It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

See chapter 12 of the ACPI specification (www.acpi.info) for more details

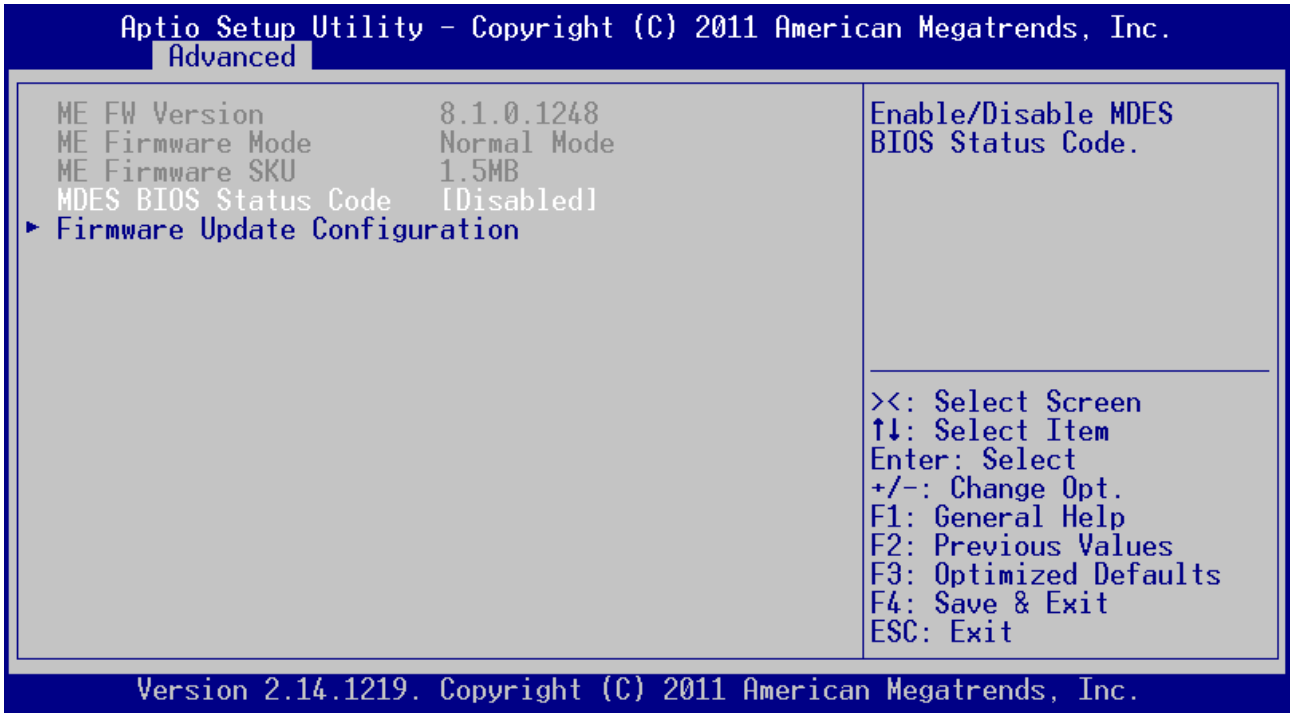
Intel Fast Flash Standby



Feature	Options	Description
iFFS	**Disabled** Enabled	Enable/Disable Intel Fast Flash Standby / Intel Rapid Start Technology
Entry on S3 RTC Wake	Disabled **Enabled**	iFFS invocation upon S3 RTC wake
Entry After	**Immediately** 1 minute 2 minutes 5 minutes 10 minutes 15 minutes 30 minutes 1 hour 2 hours	Enable RTC wake timer at S3 entry
Active Page Threshold	**Disabled** Enabled	Support iFFS with small partition

Please read chapter Intel Fast Flash Standby before enabling

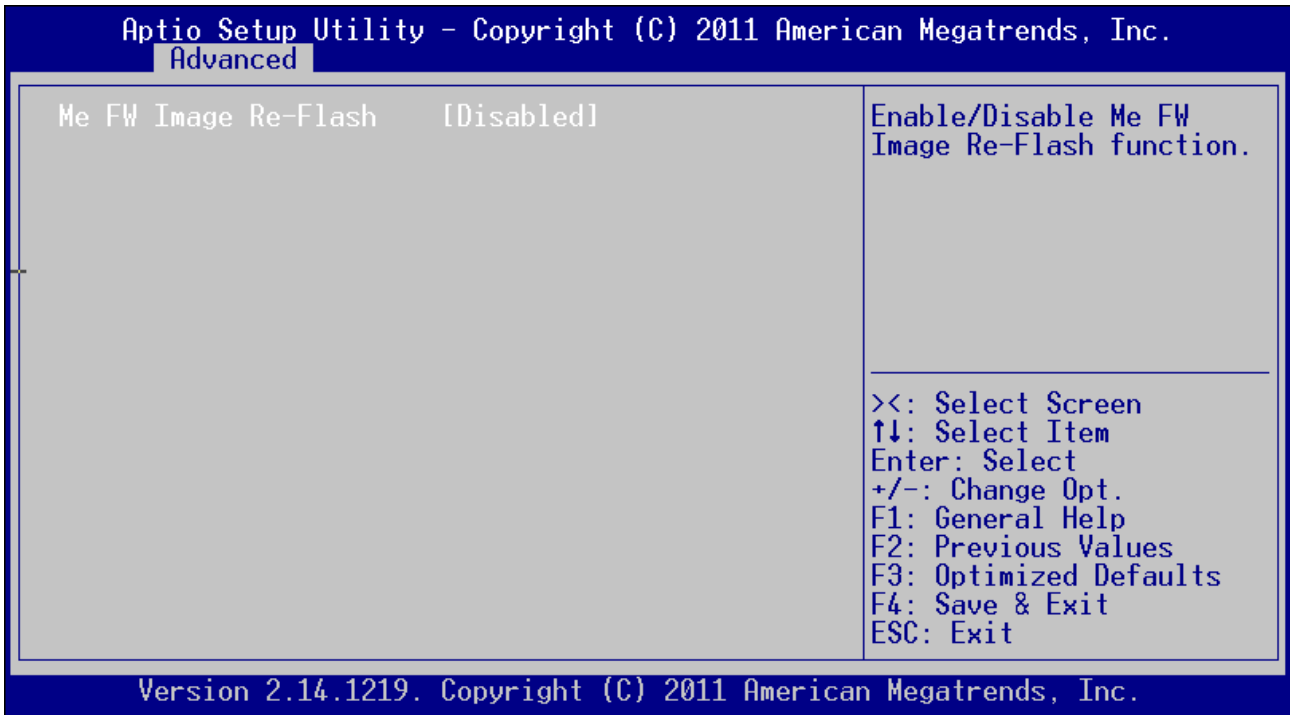
PCH-FW Configuration



Feature	Options	Description

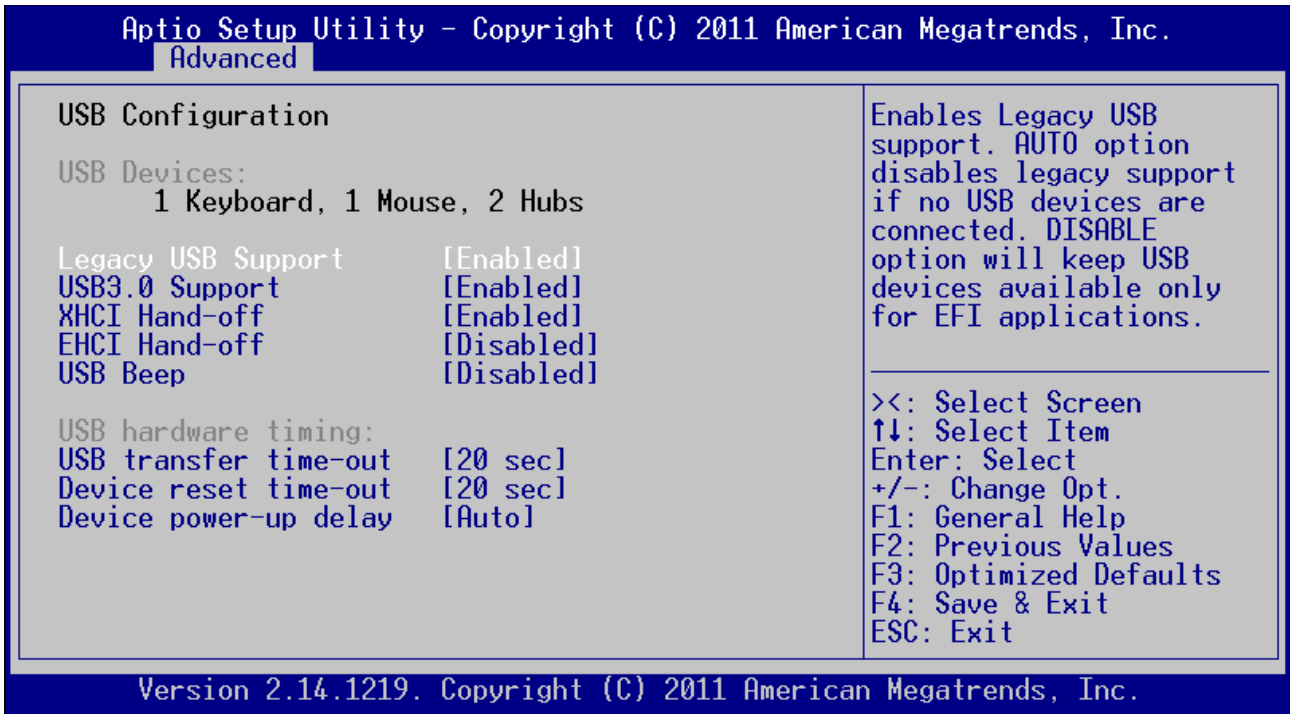
MDES BIOS Status Code	**Disabled** Enabled	Enable/Disable MDES BIOS Status Code

Firmware Update Configuration



Feature	Options	Description
Me FW Image Re-Flash	**Disabled** Enabled	Enable/Disable Me FW Image Re-Flash function

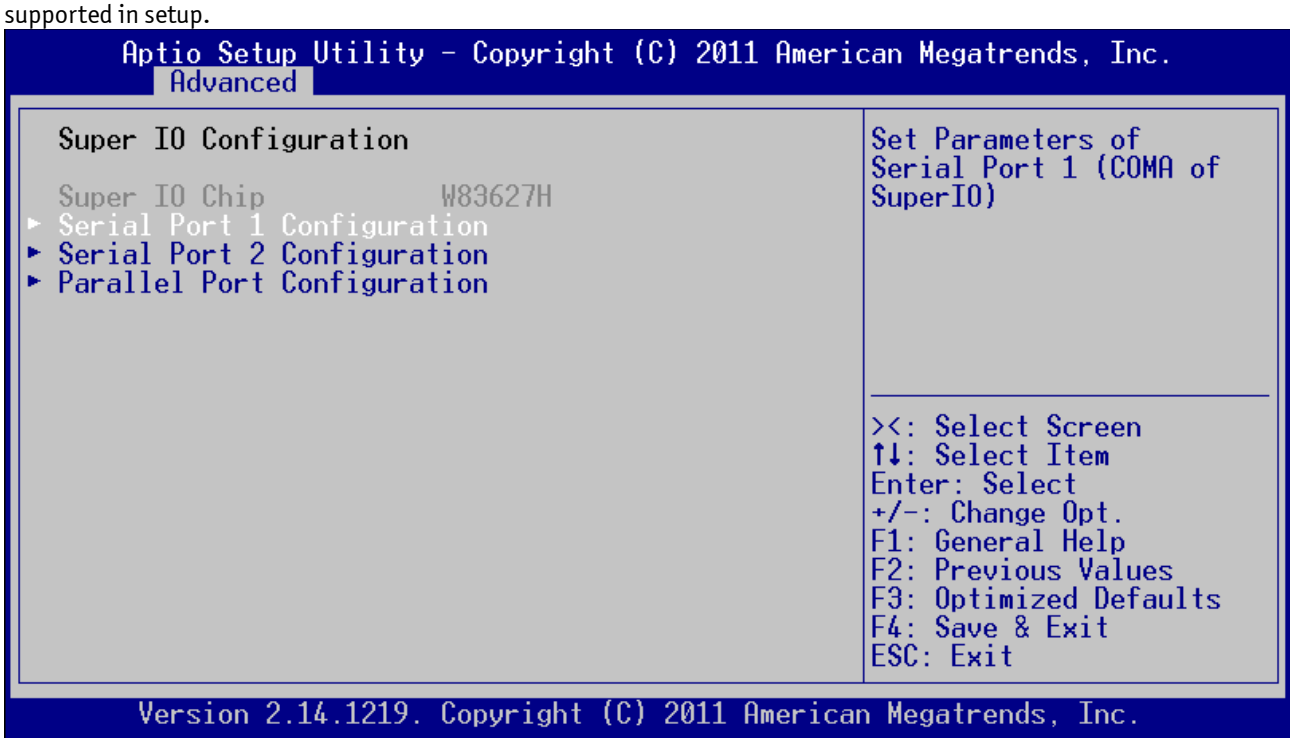
USB Configuration



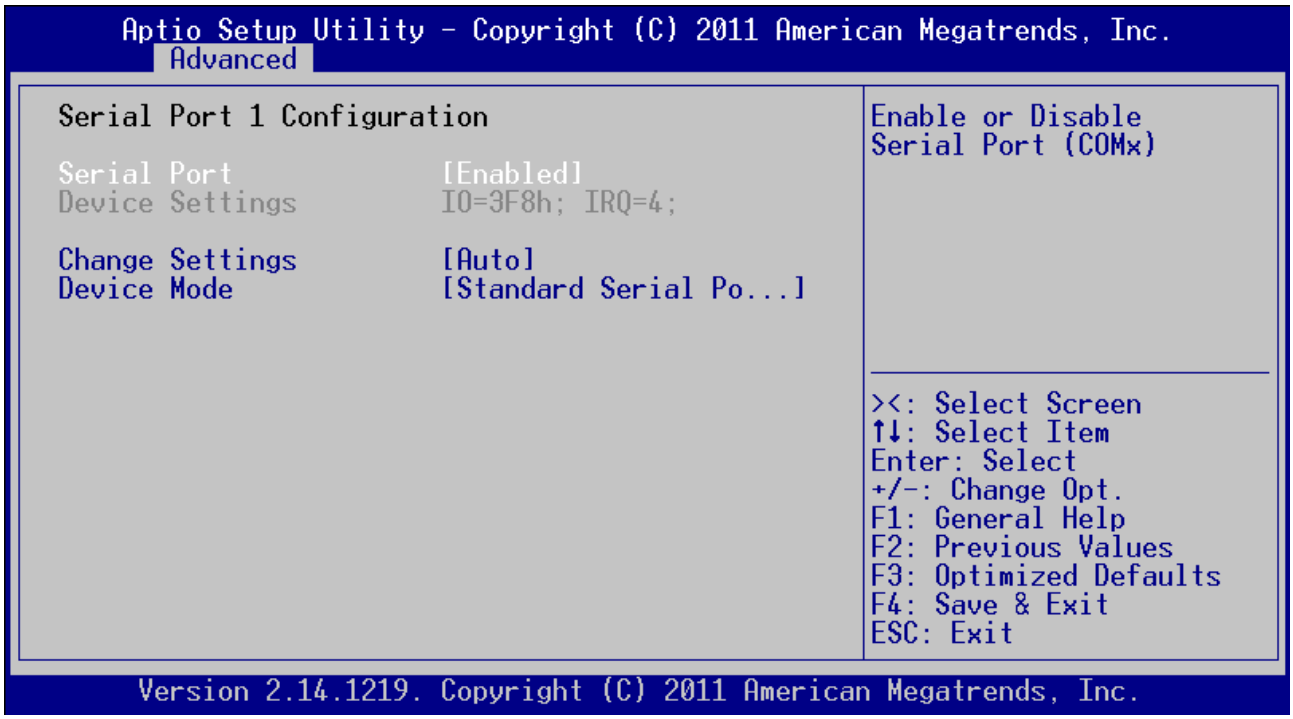
Feature	Options	Description
Legacy USB Support	**Enabled** Disabled AUTO	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
USB3.0 Support	Enabled **Disabled**	Enable/Disable USB3.0 (XHCI) Controller support. On Type 2 board only supported by external PCIe Card
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off Support. The XHCI ownership change should be claimed by XHCI driver
EHCI Hand-off	Enabled **Disabled**	This is a workaround for OSes without EHCI hand-off Support. The EHCI ownership change should be claimed by EHCI driver
USB Beep	Enabled **Disabled**	Send speaker beep for device attach / detach
USB transfer time-out	1sec 5sec 10sec **20sec**	The time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10sec **20sec** 30sec 40sec	USB mass storage device Start Unit command time-out
Device power-up delay	**AUTO** Manual	Maximum time the device will take before it properly reports itself to the Host controller. 'AUTO' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor
Device power-up delay in seconds	**5**	Delay range is 1...40 seconds, in one second increments

Super IO Configuration

This setup option is available if a LPC SuperI/O Nuvoton 83627 is present on the baseboard. By default the COMe-bIP2 supports the legacy interfaces of a 5V 83627HF(J) or 3.3V 83627DHG-P on external LPC. The SIO hardware monitor is not supported in setup.

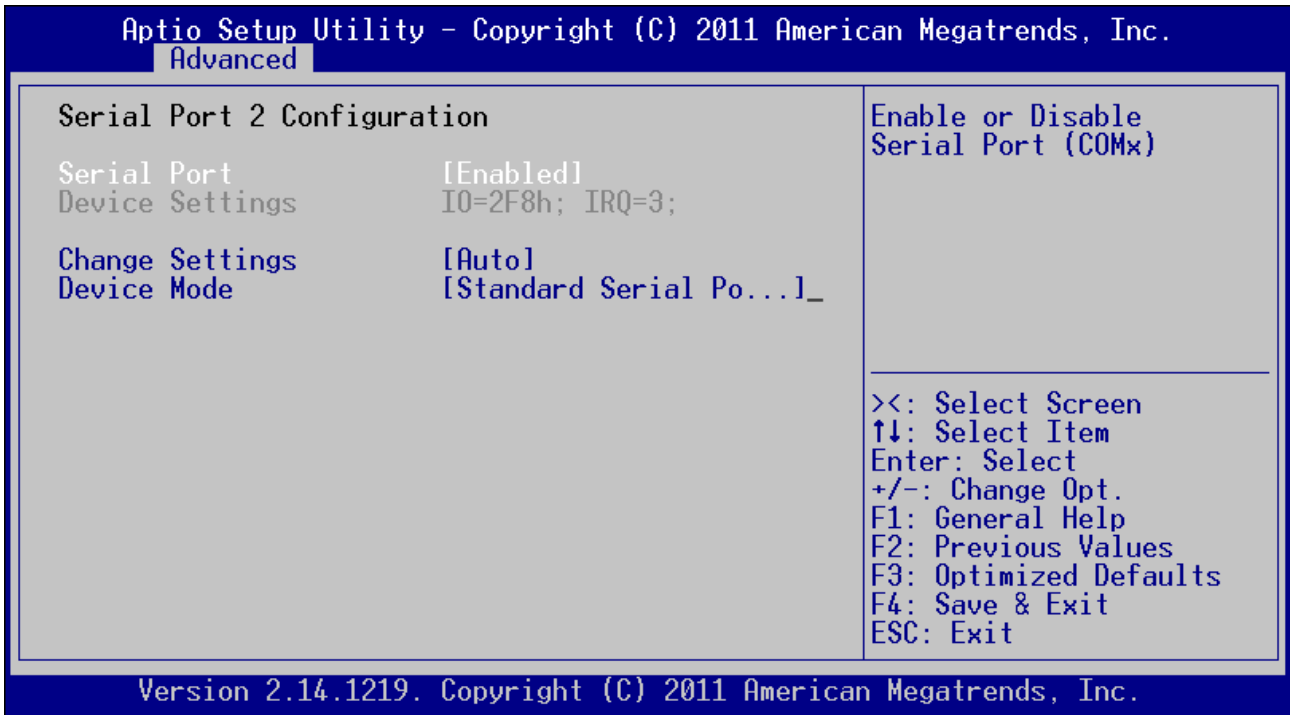


Serial Port 1 Configuration



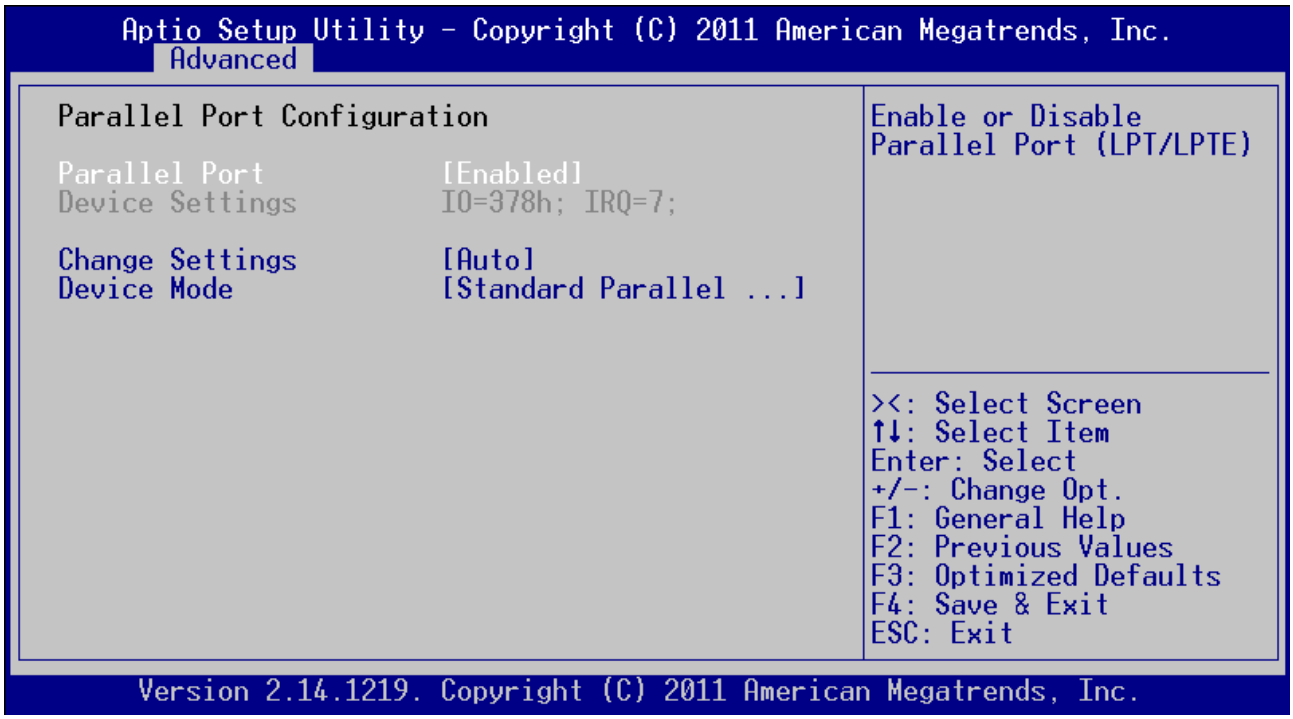
Feature	Options	Description
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM) 0
Change Settings	**AUTO** IO=3F8h; IRQ=4; IO=3F8h, IRQ=3,4,5,6,7,10,11,12; IO=2F8h, IRQ=3,4,5,6,7,10,11,12; IO=3E8h, IRQ=3,4,5,6,7,10,11,12; IO=2E8h, IRQ=3,4,5,6,7,10,11,12;	Select an optimal setting for SuperIO device.
Device Mode	**Standard Serial Port Mode** IrDA 1.0 (HP SIR) Mode ASKIR Mode	Change the Serial Port mode.

Serial Port 2 Configuration



Feature	Options	Description
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM) 1
Change Settings	**AUTO** IO=2F8h; IRQ=3; IO=3F8h, IRQ=3,4,5,6,7,10,11,12; IO=2F8h, IRQ=3,4,5,6,7,10,11,12; IO=3E8h, IRQ=3,4,5,6,7,10,11,12; IO=2E8h, IRQ=3,4,5,6,7,10,11,12;	Select an optimal setting for SuperIO device.
Device Mode	**Standard Serial Port Mode** IrDA 1.0 (HP SIR) Mode ASKIR Mode	Change the Serial Port mode.

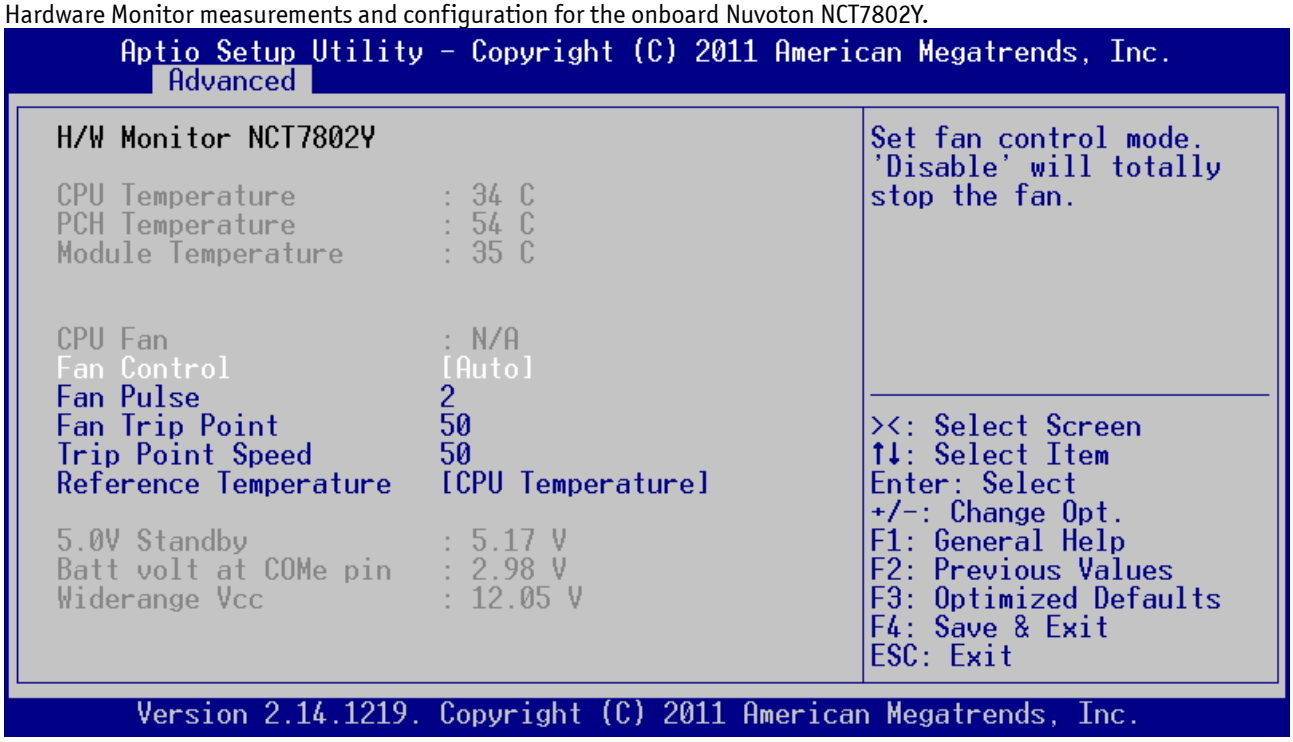
Parallel Port Configuration



Feature	Options	Description
Parallel Port	Disabled **Enabled**	Enable or Disable the Parallel Port (LPT/LPTE)
Change Settings	**AUTO** IO=378h; IRQ=5; IO=378h, IRQ=5,6,7,10,11,12; IO=278h, IRQ=5,6,7,10,11,12; IO=3BCh, IRQ=5,6,7,10,11,12; IO=378h; IO=278h; IO=3BCh;	Select an optimal setting for SuperIO device.
Device Mode	**Standard Parallel Port Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Change the Printer Port mode.

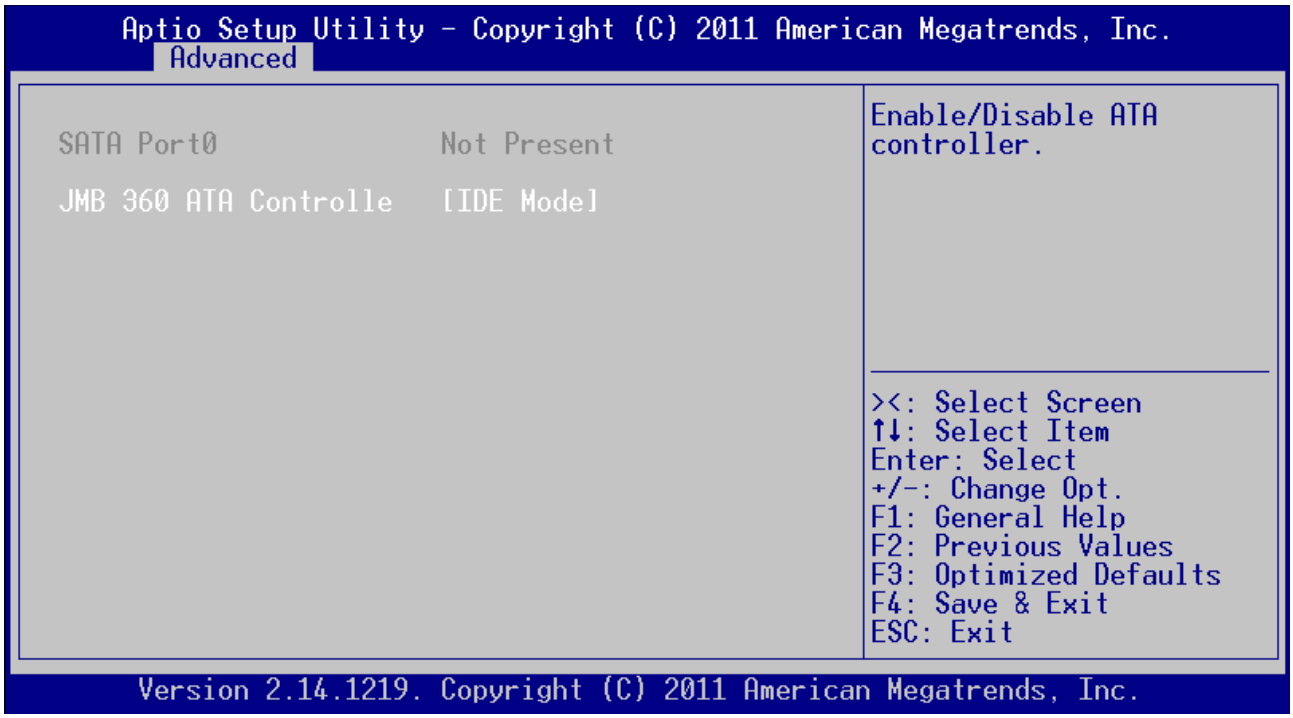
H/W Monitor

Hardware Monitor measurements and configuration for the onboard Nuvoton NCT7802Y.



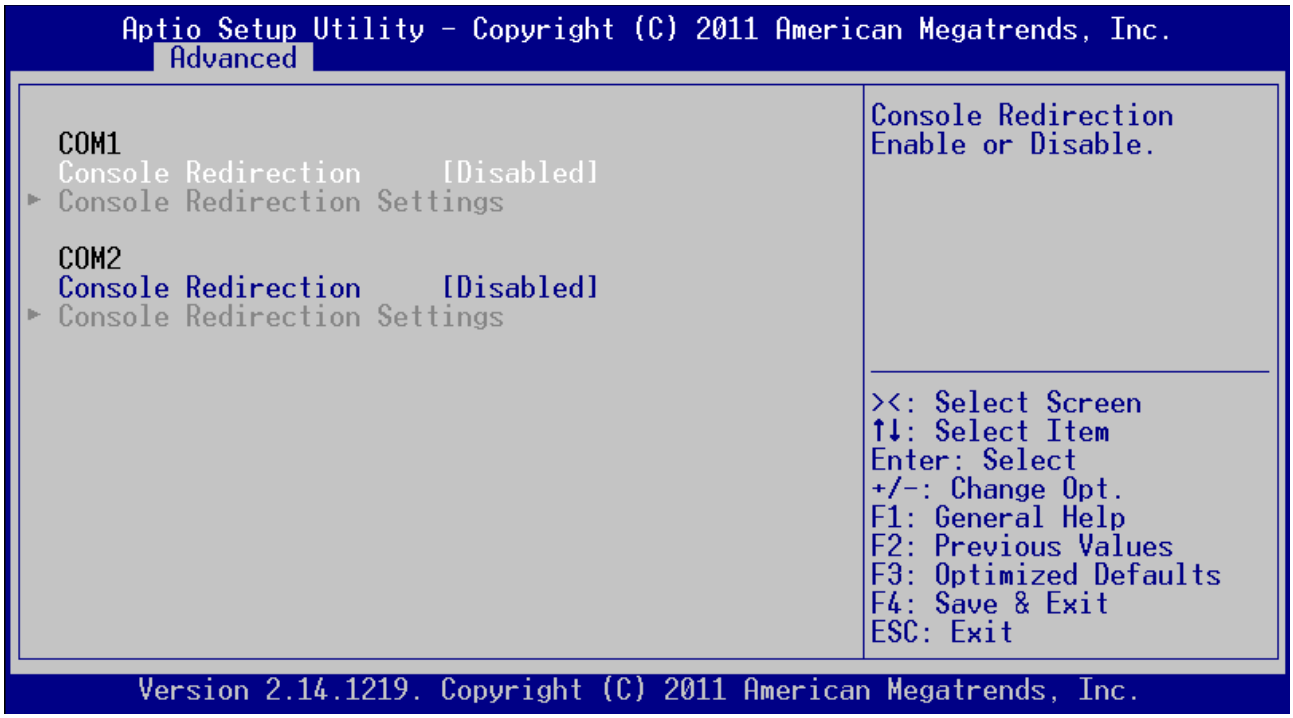
Feature	Value/Options	Description
CPU Temperatue	xx°C	Shows the measured temperature of the CPU Diode with onboard HWM
PCH Temperature	xx°C	Shows the internal Platform Controller Hub temperature
Module Temperature	xx°C	Shows the internal hardwaremonitor temperature
CPU FAN	xxxx rpm	Shows the fan speed of onboard FAN connector
FAN Control	Disabled Manual **Auto**	Set fan control mode. 'Disable' will totally stop the fan
Fan Pulse	**2**	Select the number of pulses the CPU fan produces during one revolution. Range 1-4
Fan Trip Point	**50**	Temperature where fan accelerates. Range 20 - 80°C
Fan Speed	**70**	Manual fan speed in %. Minimum value is 30 (in Manual mode only)
Trip Point Speed	**50**	Fan speed at trip point in %. Minimum value is 30. Fan always runs at 100% at Tjmax - 10°C
Reference Temperature	PCH Temperature Module Temperature **CPU Temperature**	Determines the temperature source which is used for automatic fan control
5.0V Standby	x.xx V	Shows the 5V Standby Voltage input
Batt volt at COMe pin	x.xx V	Shows the RTC Battery Voltage input measured at COMe connector
Widerange Vcc	x.xx V	Shows the Module Main Input Voltage

JMB36X ATA Controller Configuration



Feature	Options	Description
ATA Controller	Disabled **IDE Mode** AHCI Mode	Enable/Disable the onboard PATA Controller

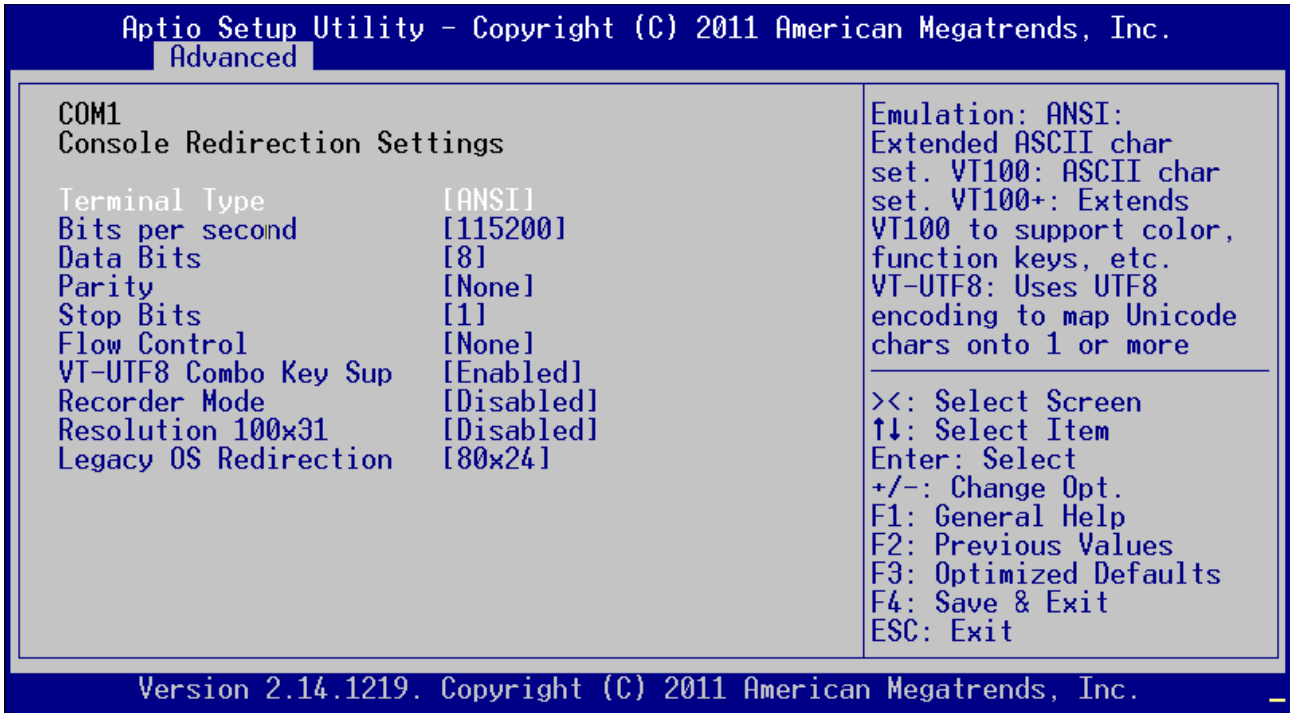
Serial Port Console Redirection



Feature	Options	Description
Console Redirection	**Disabled** Enabled	Enable/Disable Serial Port COM1 Console Redirection
Console Redirection	**Disabled** Enabled	Enable/Disable Serial Port COM2 Console Redirection

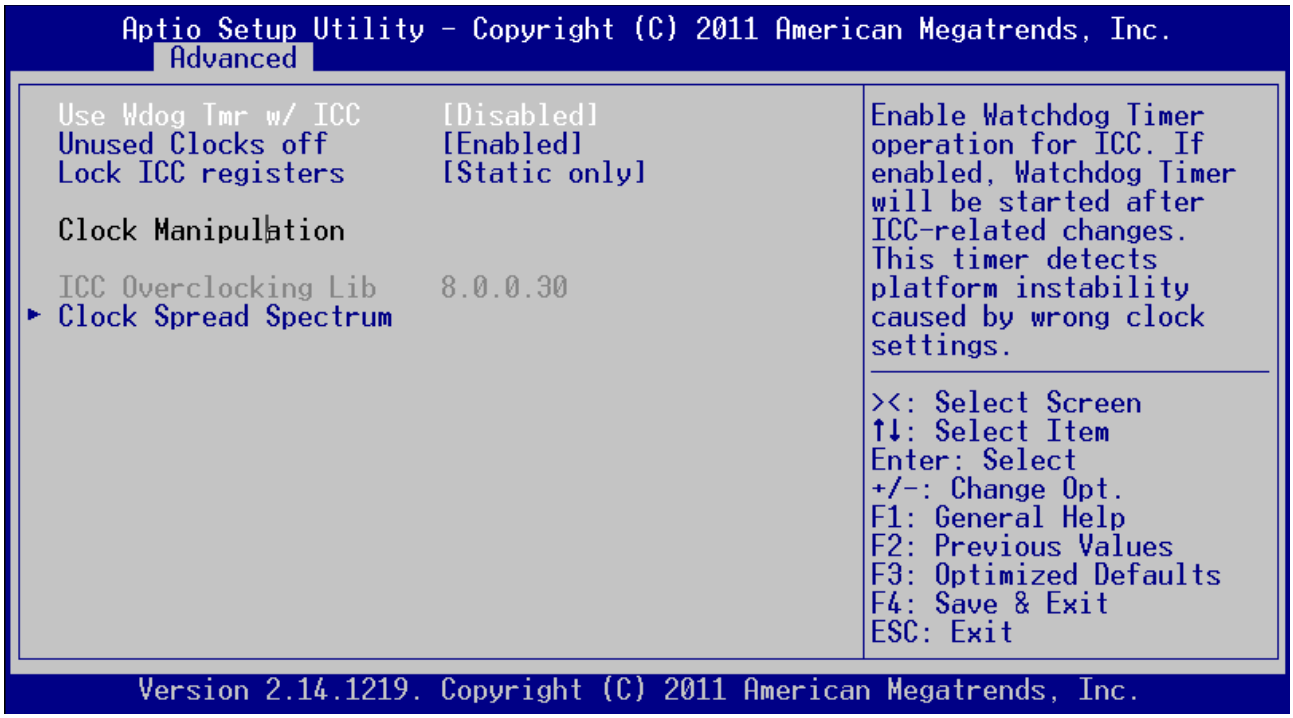
Serial Port Console Redirection is not allowed to activate at more than one port simultaneously

Console Redirection Settings



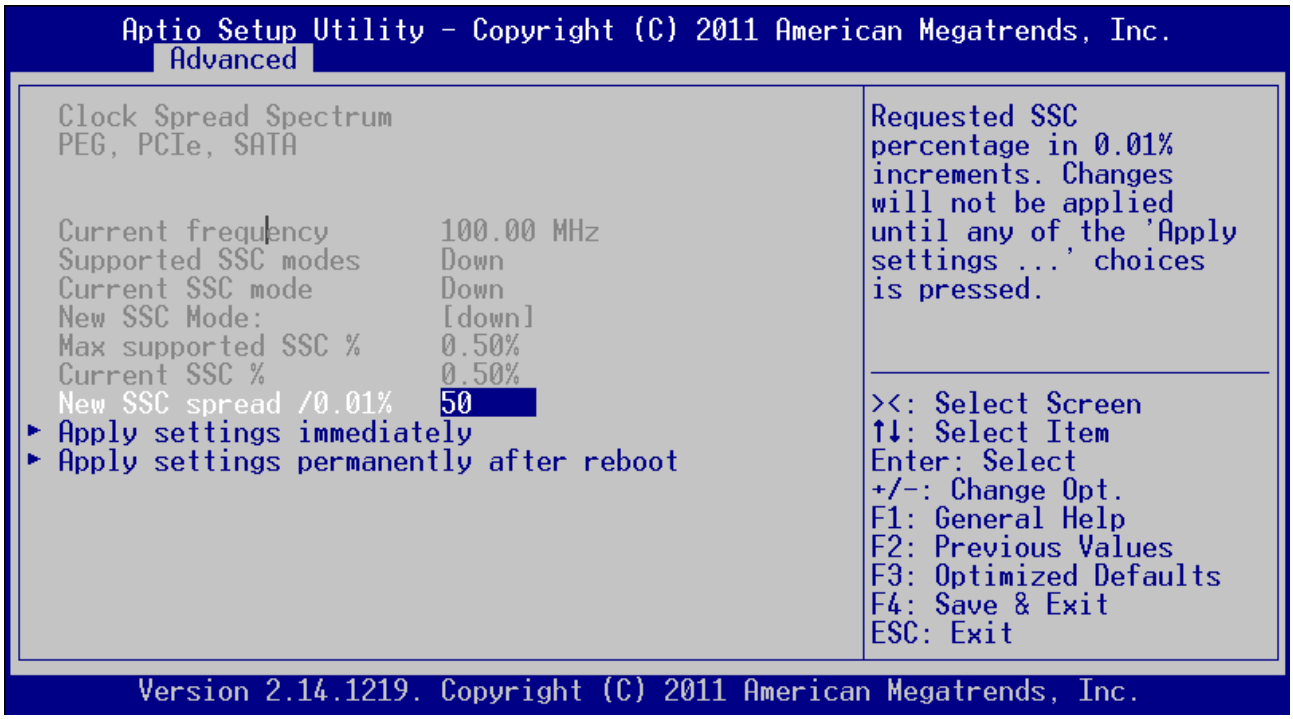
Feature	Options	Description
Terminal Type	VT100 VT100+ VT_UTF8 **ANSI**	VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes ANSI: Extended ASCII char set.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.
Stop Bits	**1** 2	Stop Bits indicate the end of a serial data packet. (A Start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture terminal data.
Resolution 100×31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	**80×24** 80×25	On Legacy OS, the Number of Rows and Columns supported redirection

Intel ICC



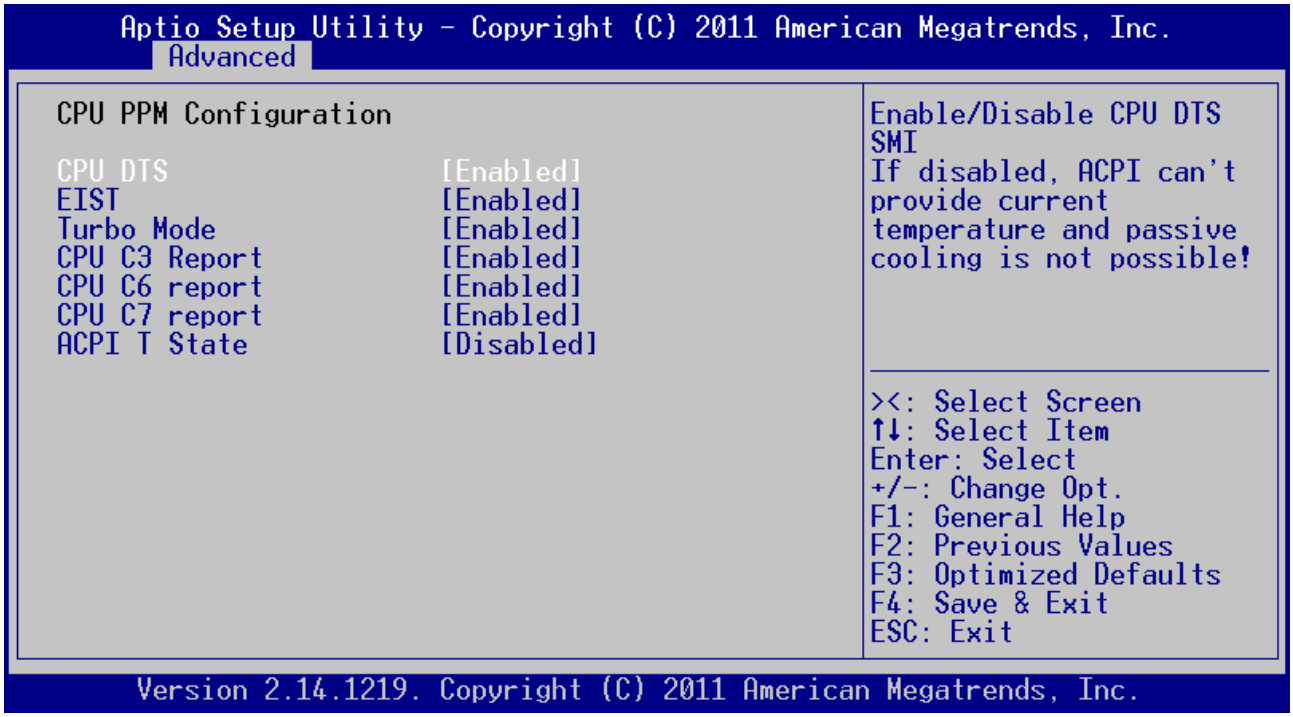
Feature	Options	Description
Use Wdog Timer w/ ICC	**Disabled** Enabled	Enable Watchdog Timer operation for ICC. If enabled, Watchdog Timer will be started after ICC-related changes. This timer detects platform instability caused by wrong clock settings
Unused Clocks off	**Enabled** Disabled	Disabled: all clocks turned on. Enabled: clocks for empty PCI/PCIe slots will be turned off to save power. Platform must be powered off for changes to take effect.
Lock ICC registers	**Static only** All registers	All registers: all ICC registers will be locked. Static only: only static ICC registers will be locked.

Clock Spread Spectrum



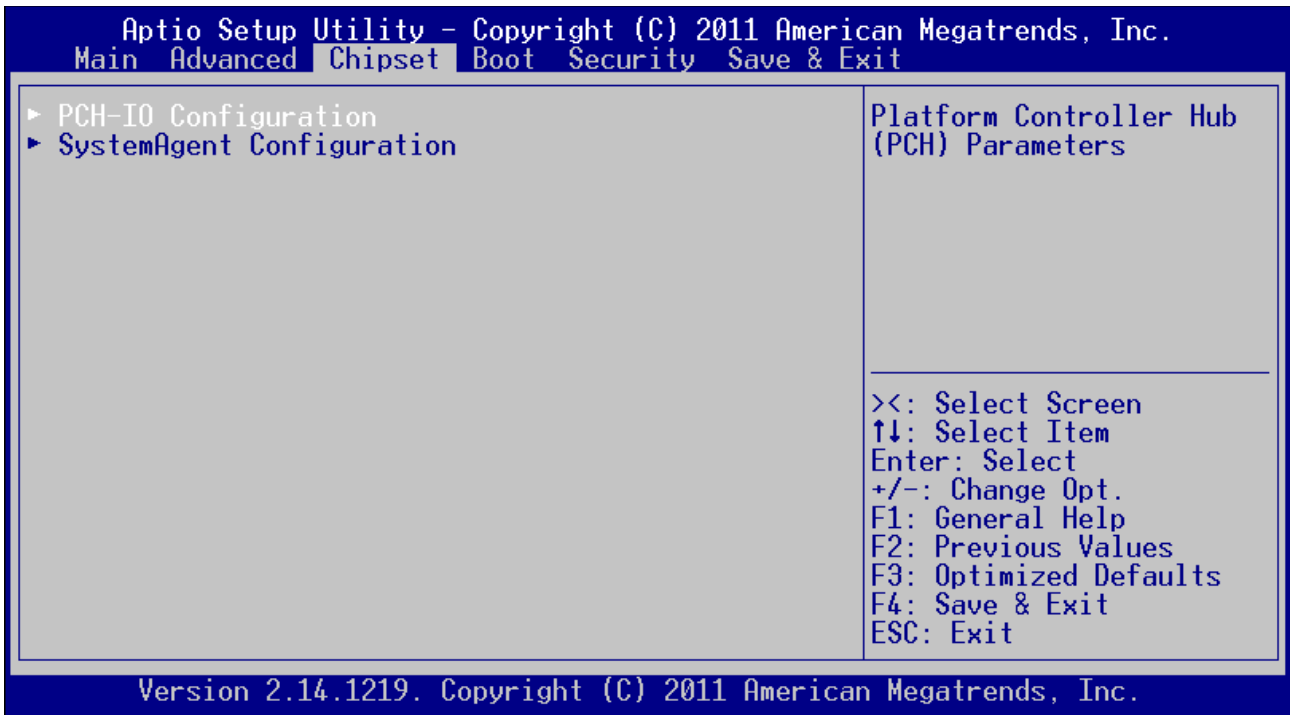
Feature	Options	Description
New SSC spread /0.01%	**50**	Request SSC percentage in 0.01% increments. Changes will not be applied until any of the 'Apply settings ...' choices is pressed.
Apply settings immediately	-	Changes will be applied immediately, but forgotten after reboot. This mode of making changes is more likely to cause platform instability and spontaneous restart.
Apply settings permanently after reboot	-	Changes will be applied permanently, starting after the next reboot. Use this to provide changes that are verified and safe.

CPU PPM Configuration

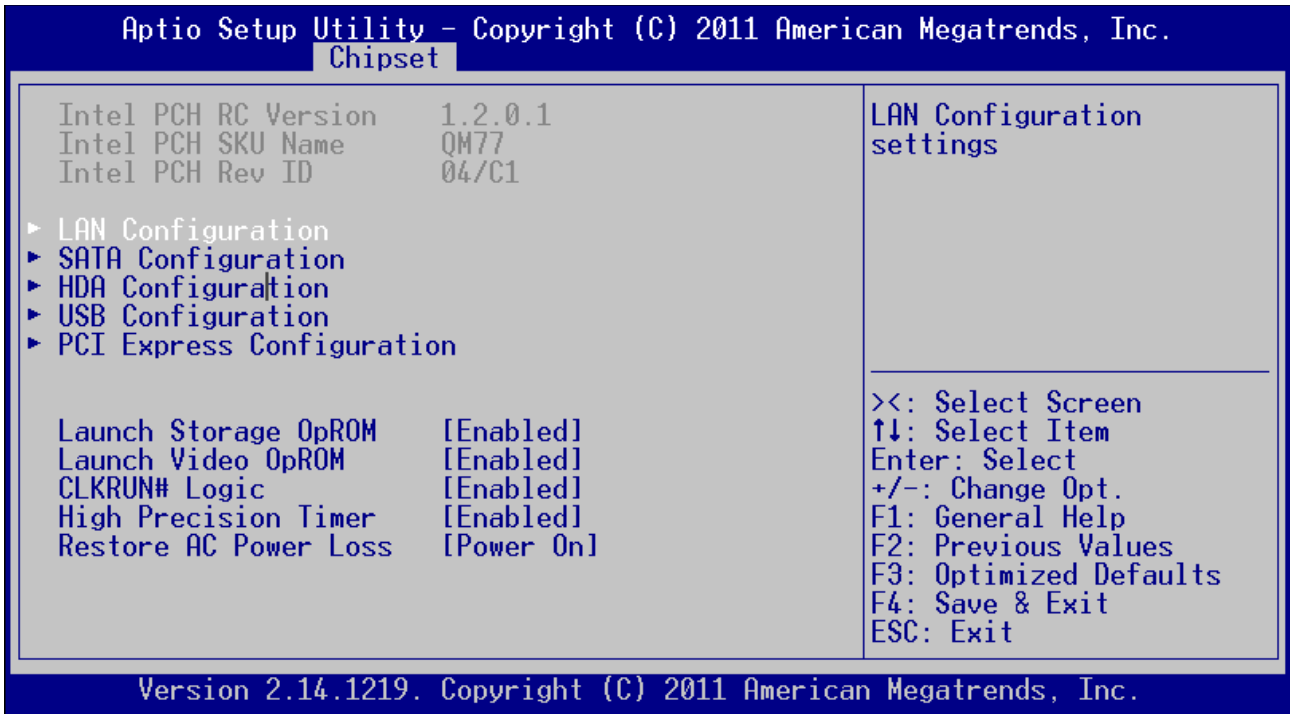


Feature	Options	Description
CPU DTS	Disabled **Enabled**	Enable/Disable CPU DTS SMI. If disabled, ACPI can't provide current temperature and passive cooling is not possible
EIST	Disabled **Enabled**	Enable/Disable the Intel Speedstep Technology
Turbo Mode	Disabled **Enabled**	Enables/Disables the Intel Processor Turbo Mode 2.0
CPU C3 Report	Disabled **Enabled**	Enable/Disable CPU C3 (ACPI C2) report to OS
CPU C6 Report	Disabled **Enabled**	Enable/Disable CPU C6 (ACPI C3) report to OS
CPU C7 Report	Disabled **Enabled**	Enable/Disable CPU C7 (ACPI C3) report to OS
Configurable TDP	**TDP Nominal*** TDP UP TDP Down Disabled	Allow reconfiguration of TDP levels bases on current power and thermal delivery capabilities of the system. See CPU Specifications in chapter product specification for CPUs supporting cTDP. Setup option available on supported SKUs only
ACPI T-State	**Disabled** Enabled	Enable/Disable ACPI T-state support

8.5.3 Chipset

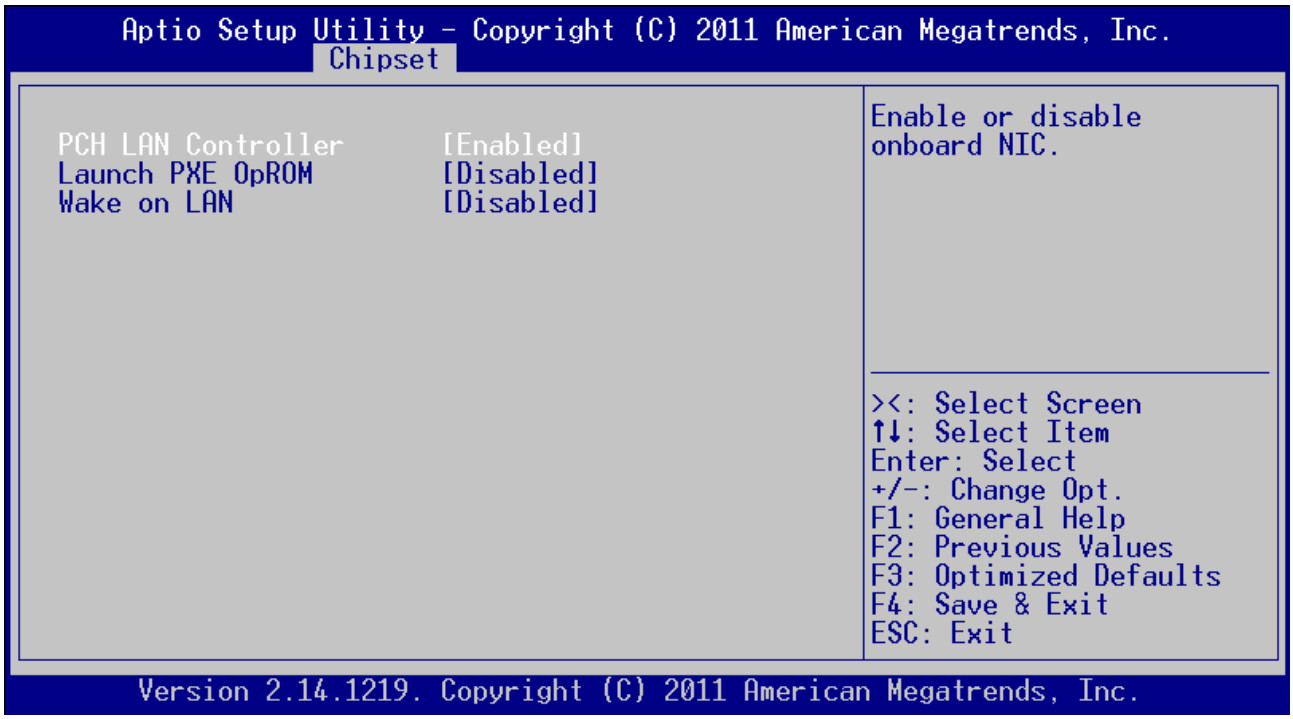

Aptio Setup Utility – Copyright (C) 2011 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
► PCH-IO Configuration
► SystemAgent Configuration
Platform Controller Hub (PCH) Parameters
><: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.

PCH-IO Configuration



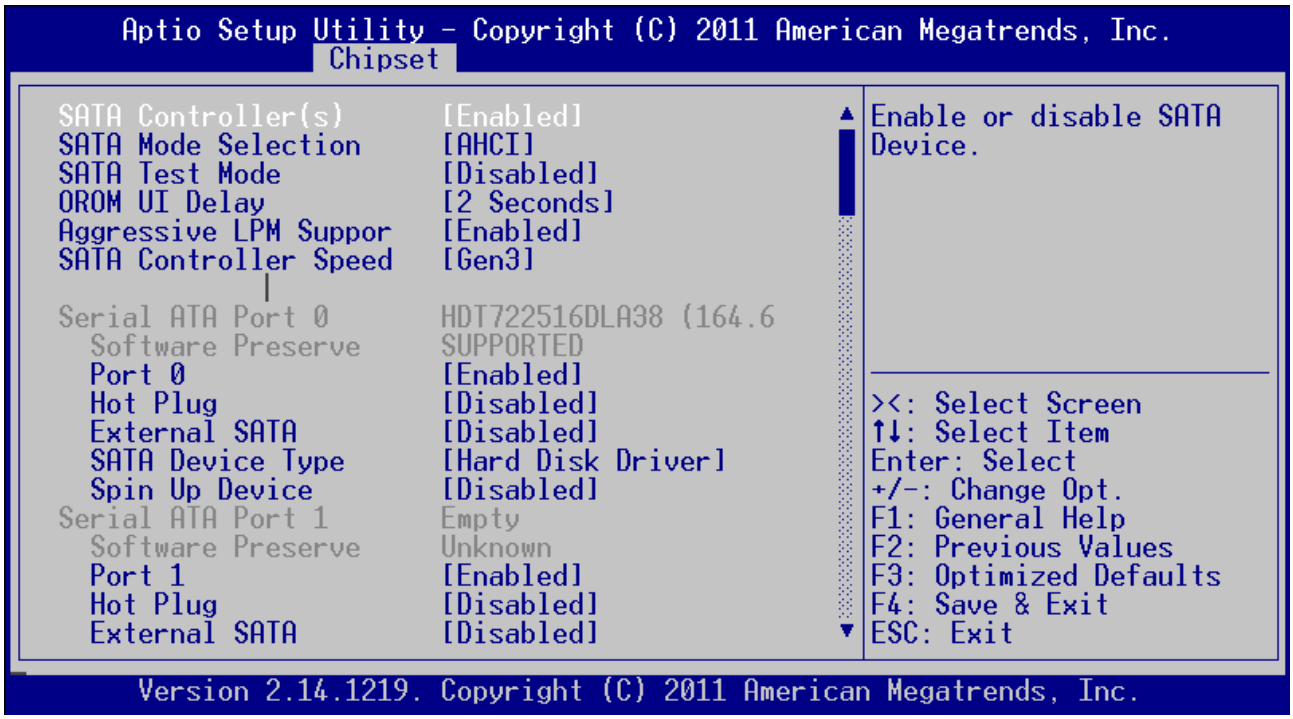
Feature	Options	Description
Launch Storage OpROM	Disabled **Enabled**	Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM
Launch Video OpROM	Disabled **Enabled**	Enable or Disable execution of the legacy Option ROM for video devices
CLKRUN# logic	Disabled **Enabled**	Enable the CLKRUN# logic to stop the PCI clocks
High Precision Timer	Disabled **Enabled**	Enable or Disable the High Precision Event Timer
Restore AC Power Loss	Power Off **Power On** Last State	Select AC power state when power is re-applied after a power failure

LAN Configuration



Feature	Options	Description
PCH LAN Controller	**Enabled** Disabled	Enable/Disable onboard NIC
Launch PXE OpROM	**Disabled** Enabled	Enable/Disable Boot Option for Legacy Network Devices
Wake on LAN	**Disabled** Enabled	Enable/Disable integrated LAN to wake the system

SATA Configuration

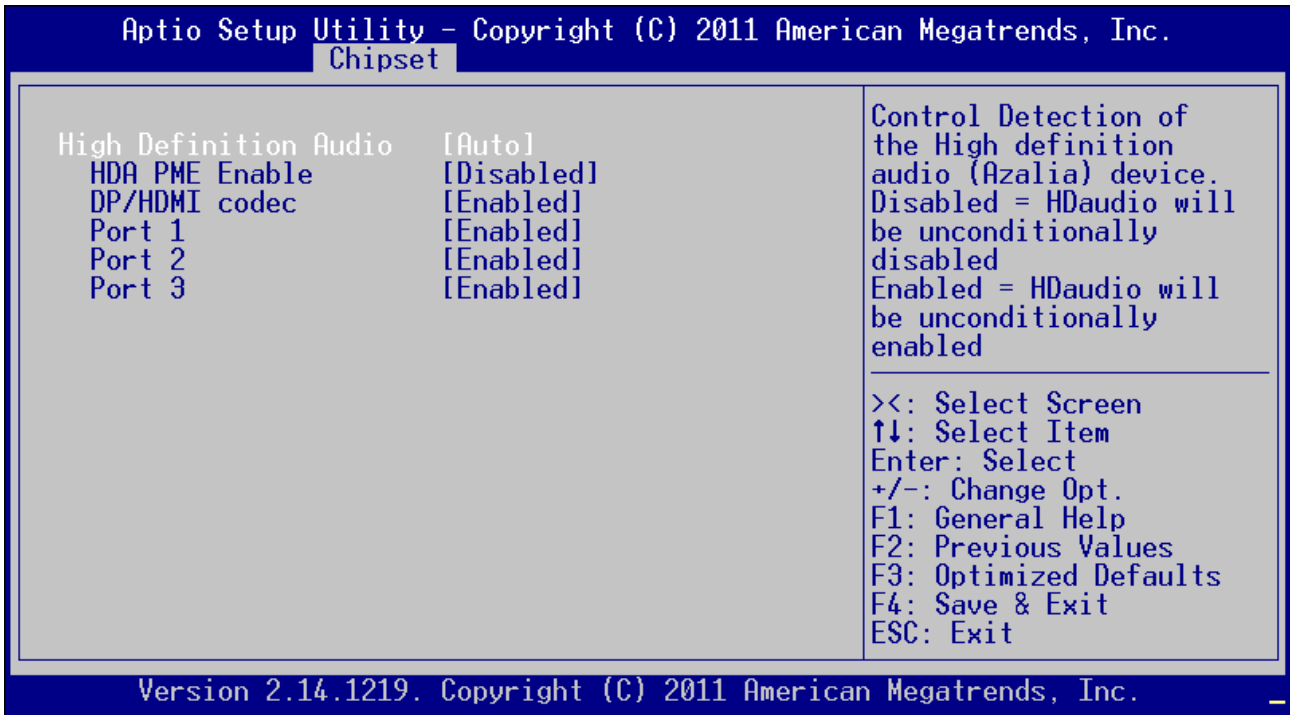


Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable/Disable SATA Device
SATA Mode Selection	IDE **AHCI** RAID	Determines how SATA controller(s) operate
SATA Test mode	**Disabled** Enabled	Enable or disable Test Mode
OROM UI Delay	**2 Seconds** 4 Seconds 6 Seconds 8 Seconds	If enabled, indicates the delay of the OPROM UI Splash Screen in a normal status
Aggressive LPM Support	Disabled **Enabled**	Enable PCH to aggressively enter link power state
SATA Controller Speed	Gem1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support
Alternate ID	Enabled **Disabled**	Report alternate Device ID

Serial ATA Port 0/1/2/3 Configuration

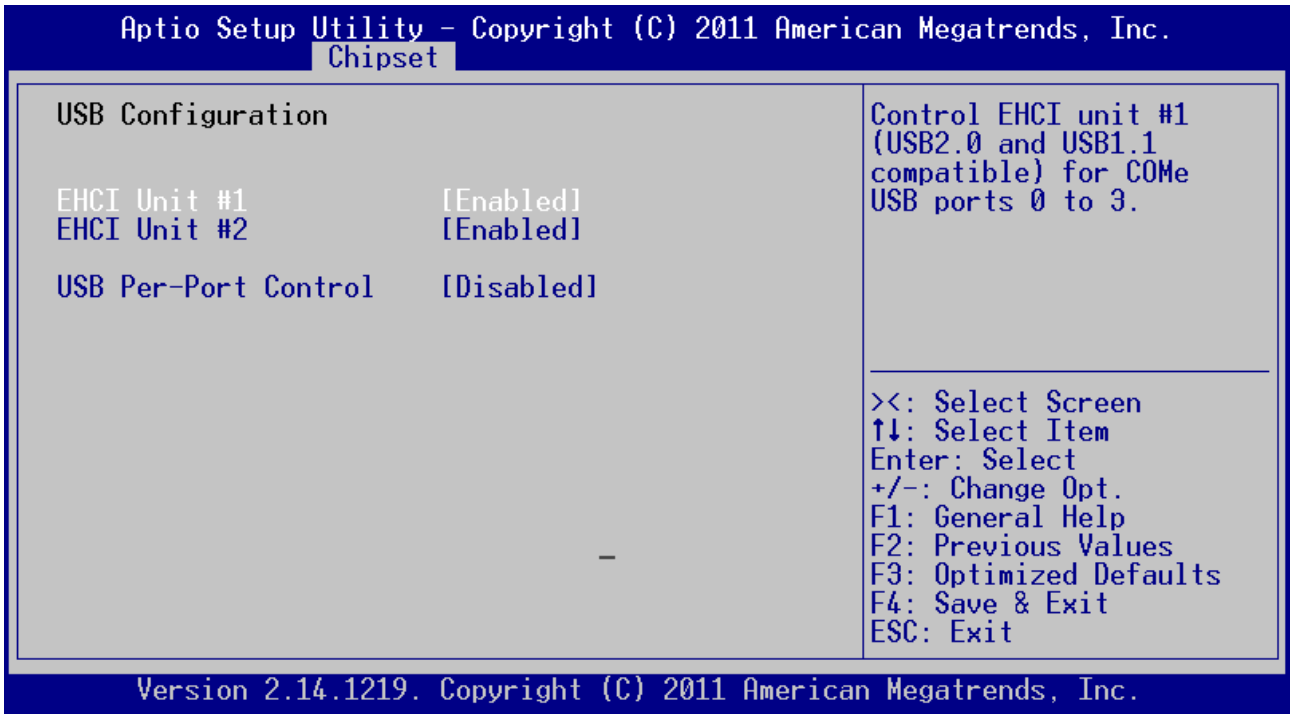
Feature	Options	Description
PORT 0 PORT 1 PORT 2 PORT 3	**Enabled** Disabled	Enable or Disable SATA Port
Hot Plug	**Disabled** Enabled	Designates this port as Hot Pluggable
External SATA	**Disabled** Enabled	Enable/Disable eSATA Support
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Driver or Hard Disk Drive
Spin Up Device	**Disabled** Enabled	If enabled for any of the ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot

HDA Configuration



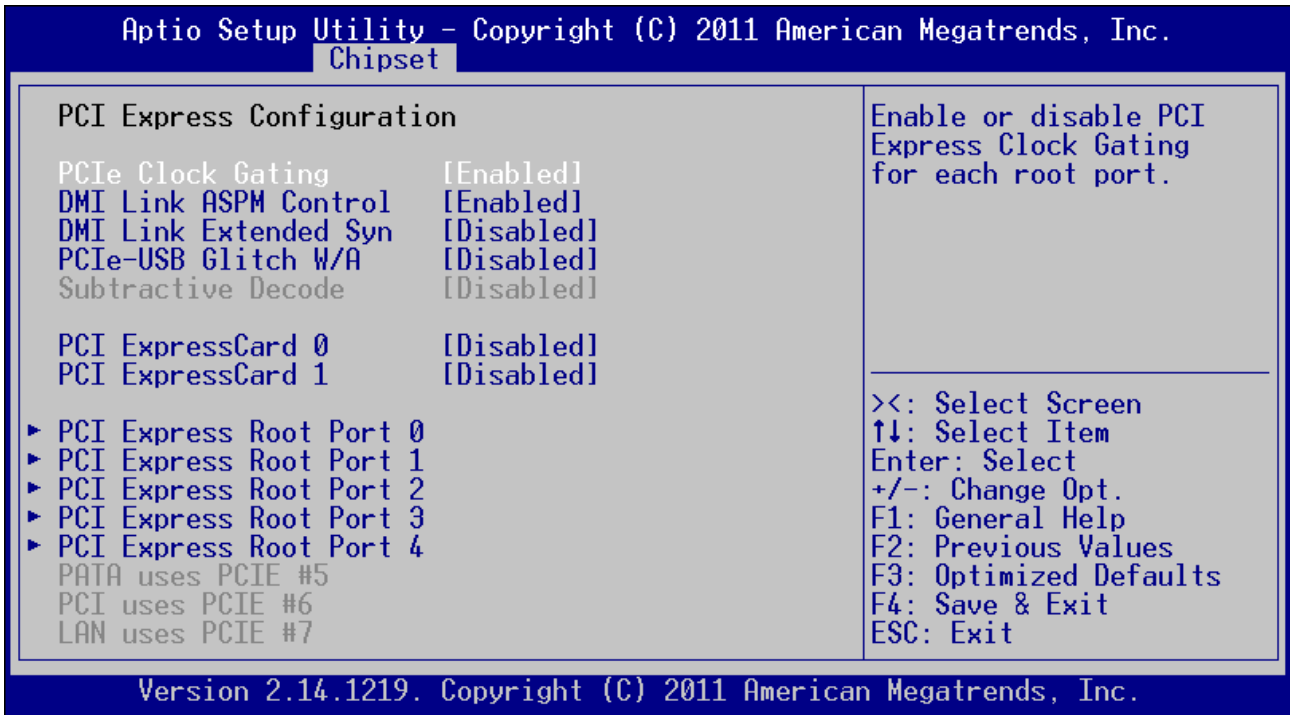
Feature	Options	Description
High Definition Audio	Disabled Enabled **Auto**	Control Detection of the High definition audio (Azalia) device. Disabled = HDaudio will be unconditionally disabled. Enabled = HDaudio will be unconditionally enabled. Auto = HDaudio will be enabled if present, disabled otherwise
HDA PME Enable	**Disabled** Enabled	Enable/Disable Power Management capability of Audio Controller
DP/HDMI Codec	Disabled **Enabled**	Enable/Disable internal DisplayPort/HDMI audio codec
Port 1	Disabled **Enabled**	Enable/Disable internal HDMI codec for DDI1
Port 2	Disabled **Enabled**	Enable/Disable internal HDMI codec for DDI2
Port 3	Disabled **Enabled**	Enable/Disable internal HDMI codec for DDI3

USB Configuration



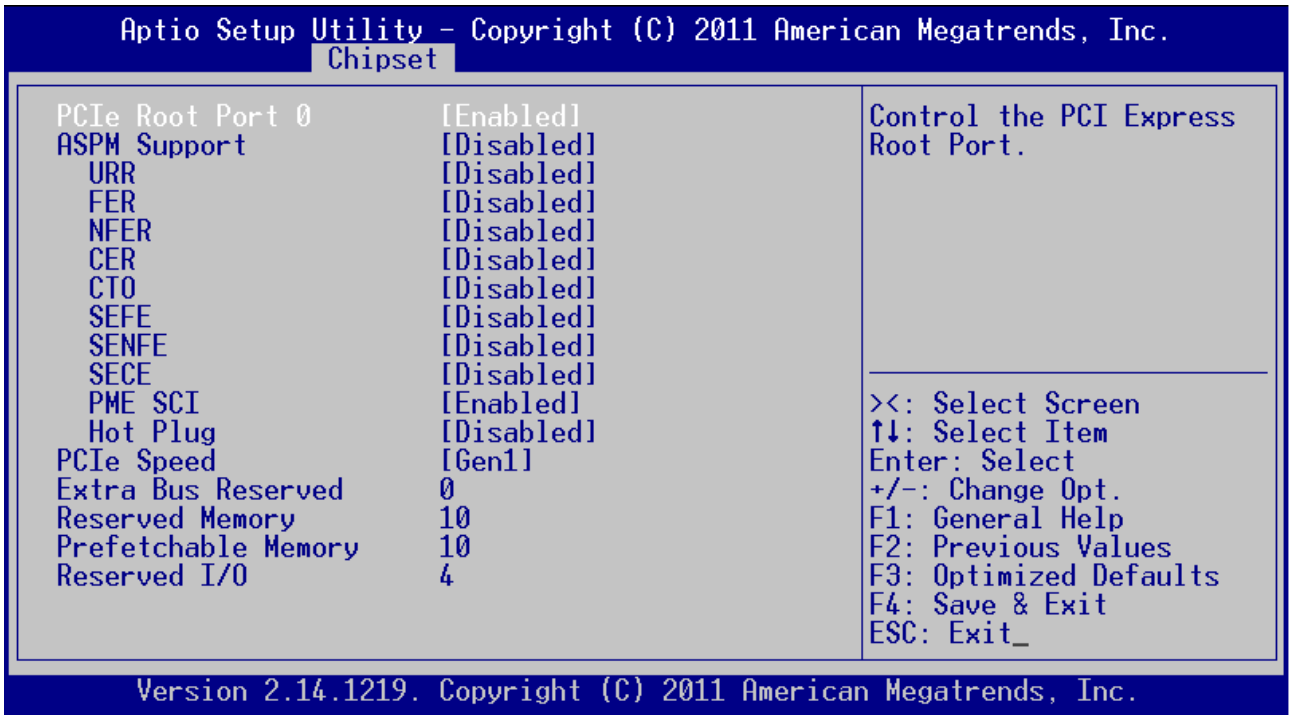
Feature	Options	Description
EHCI1	**Enabled** Disabled	Enables or Disables EHCI1 for COMe USB 0-3. xHCI must be disabled separately. One EHCI controller must always be enabled
EHCI2	**Enabled** Disabled	Enables or Disables EHCI2 for COMe USB 4-7. One EHCI controller must always be enabled
USB Per-Port Control	**Disabled** Enabled	Control each of the USB ports (0-13) disabling
USB Port #0 Disable USB Port #1 Disable USB Port #2 Disable USB Port #3 Disable USB Port #4 Disable USB Port #5 Disable USB Port #6 Disable USB Port #7 Disable	Disabled **Enabled**	Disable USB port

PCI Express Configuration



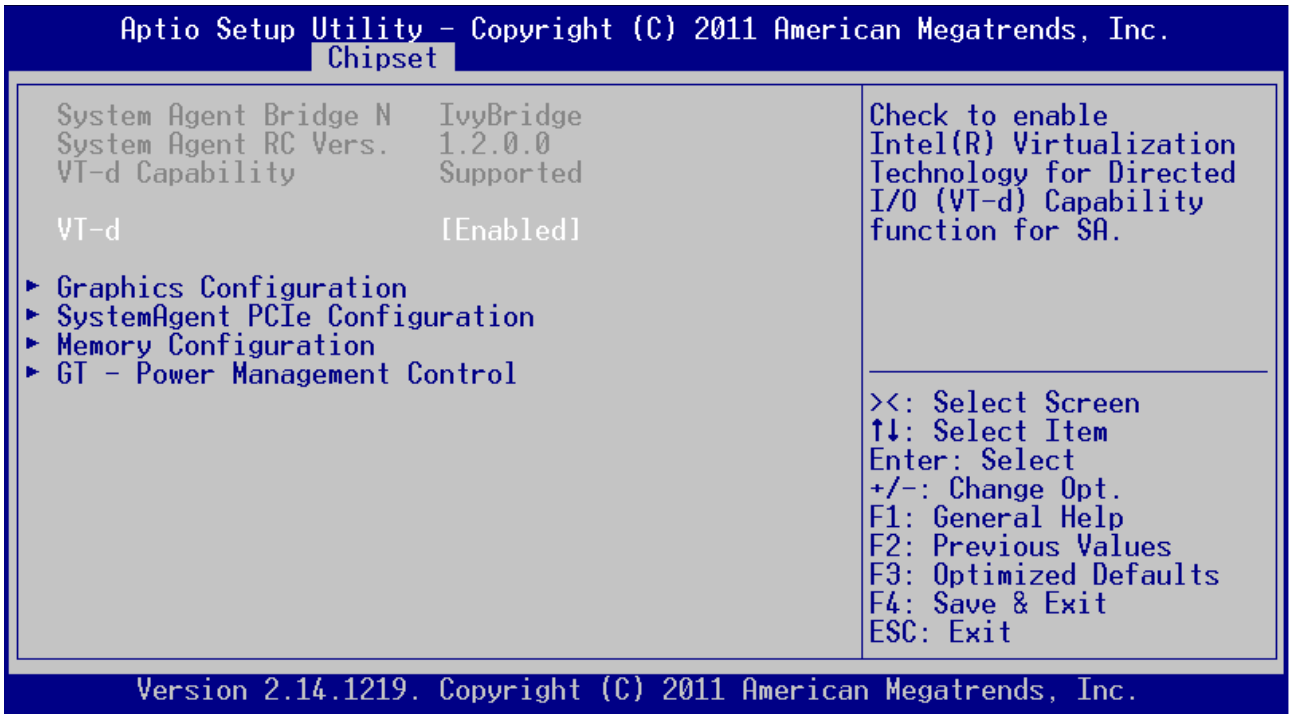
Feature	Options	Description
PCIe Clock Gating	Disabled **Enabled**	Enable or Disable PCI Express Clock Gating for each root port
DMI Link ASPM Control	Disabled **Enabled**	Controls Active State Power Management on both NB side and SB side of the DMI Link
DMI Link Ext Synch	**Disabled** Enabled	Controls Extended Synch on SB side of the DMI Link
PCIe-USB Glitch W/A	Disabled **Enabled**	PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIe/PEG Port
PCI ExpressCard 0 PCI ExpressCard 1	Port 0 Port 1 Port 2 Port 3 Port 4 Port 5 **Disabled**	Controls PCIe Port for ExpressCard support

PCI Express Root Port 0/1/2/3/4



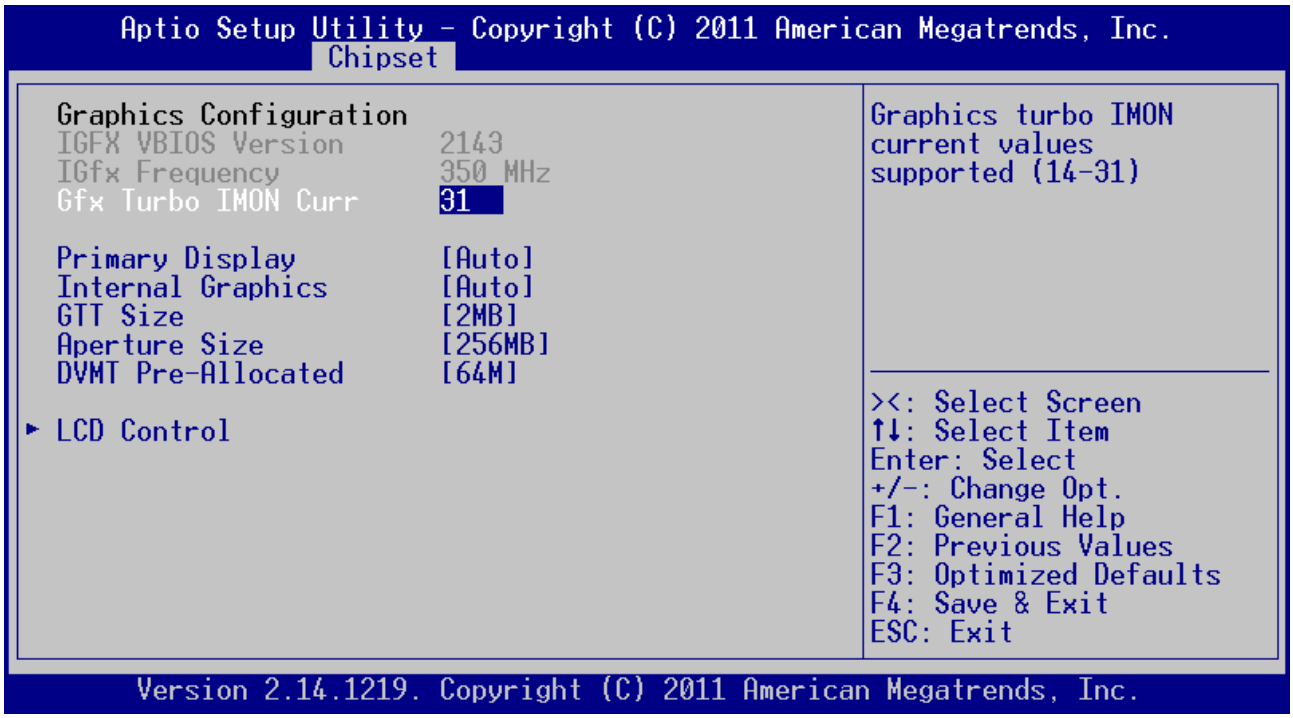
Feature	Options	Description
PCI Express Root Port	Disabled **Enabled**	Control the PCI Express Root Port
ASPM Support	**Disabled** L0s L1 L0sL1 Auto	Automatically enable ASPM based on reported capabilities and known issues
URR	**Disabled** Enabled	Enable or Disable PCI Express Unsupported Request Reporting
FER	**Disabled** Enabled	Enable or Disable PCI Express Device Fatal Error Reporting
NFER	**Disabled** Enabled	Enable or Disable PCI Express Device Non-Fatal Error Reporting
CER	**Disabled** Enabled	Enable or Disable PCI Express Device Correctable Error Reporting
CTO	**Disabled** Enabled	Enable or Disable PCI Express Completion Timer Timeout
SEFE	**Disabled** Enabled	Enable or Disable Root PCI Express System Error on Fatal Error
SENFE	**Disabled** Enabled	Enable or Disable Root PCI Express System Error on Non-Fatal Error
SECE	**Disabled** Enabled	Enable or Disable Root PCI Express System Error on Correctable Error
PME SCI	Disabled **Enabled**	Enable or Disable PCI Express PME SCI
Hot Plug	**Disabled** Enabled	Enable or Disable PCI Express Hot Plug
PCIe Speed	Auto **Gen1** Gen2	Configure PCIe Speed
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory (1-20 MB) Range for this Root Bridge
Prefetchable Memory	**10**	Prefetchable Memory (1-20 MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4k/8k(12k/16k/20k) Range for this Root Bridge

SystemAgent Configuration



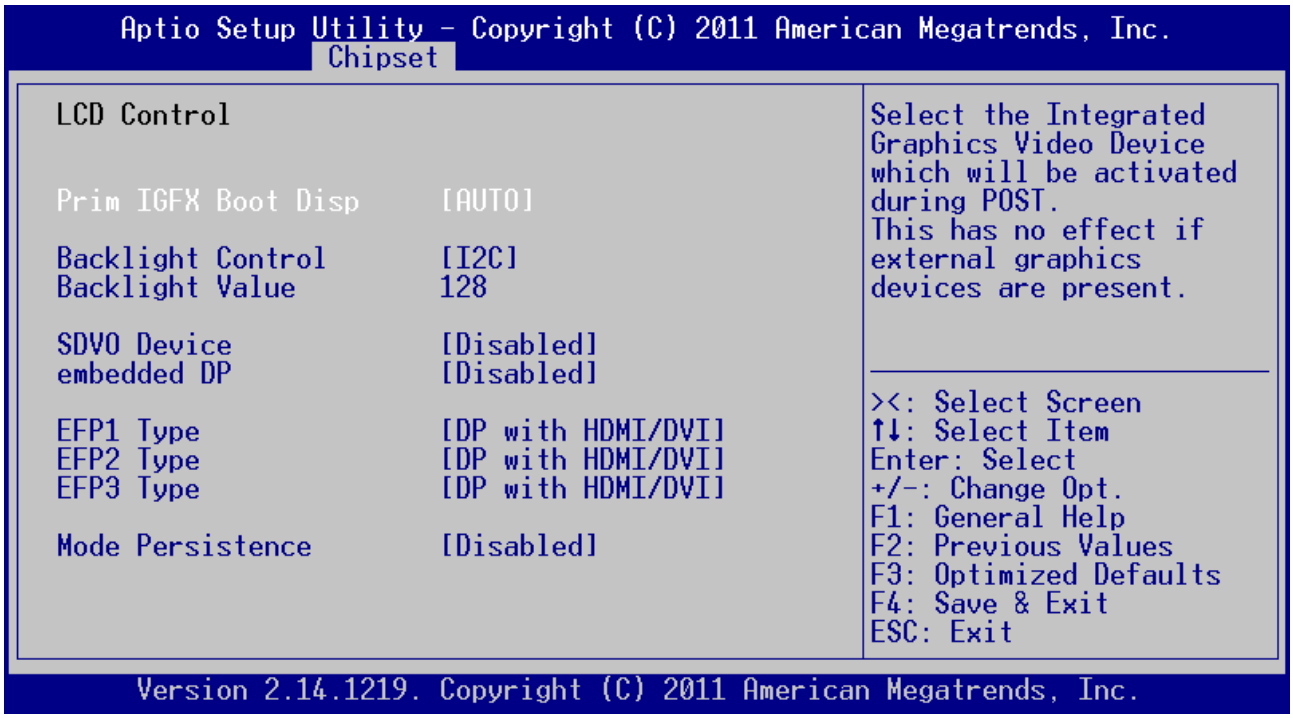
Feature	Options	Description
VT-d	Disabled **Enabled**	Check to enable Intel® Virtualization Technology for Directed I/O (VT-d) Capability function for SA

Graphics Configuration



Feature	Options	Description
Gfx Turbo IMON Curr	**31**	Graphics turbo IMON current values supported (14-31)
Primary Display	**Auto** IGFX PEG PCI	Select which of IGFX/PEG/PCI Graphics device should be Primary Display
Internal Graphics	**Auto** Disabled Enabled	Keep IGFX enabled based on the setup options
GTT Size	1MB **2MB**	Select the GTT Size
Aperture Size	128MB **256MB** 512MB	Select the Aperture Size
DVMT Pre-Allocated	0M ... **64M** ... 1024M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics device

LCD Control

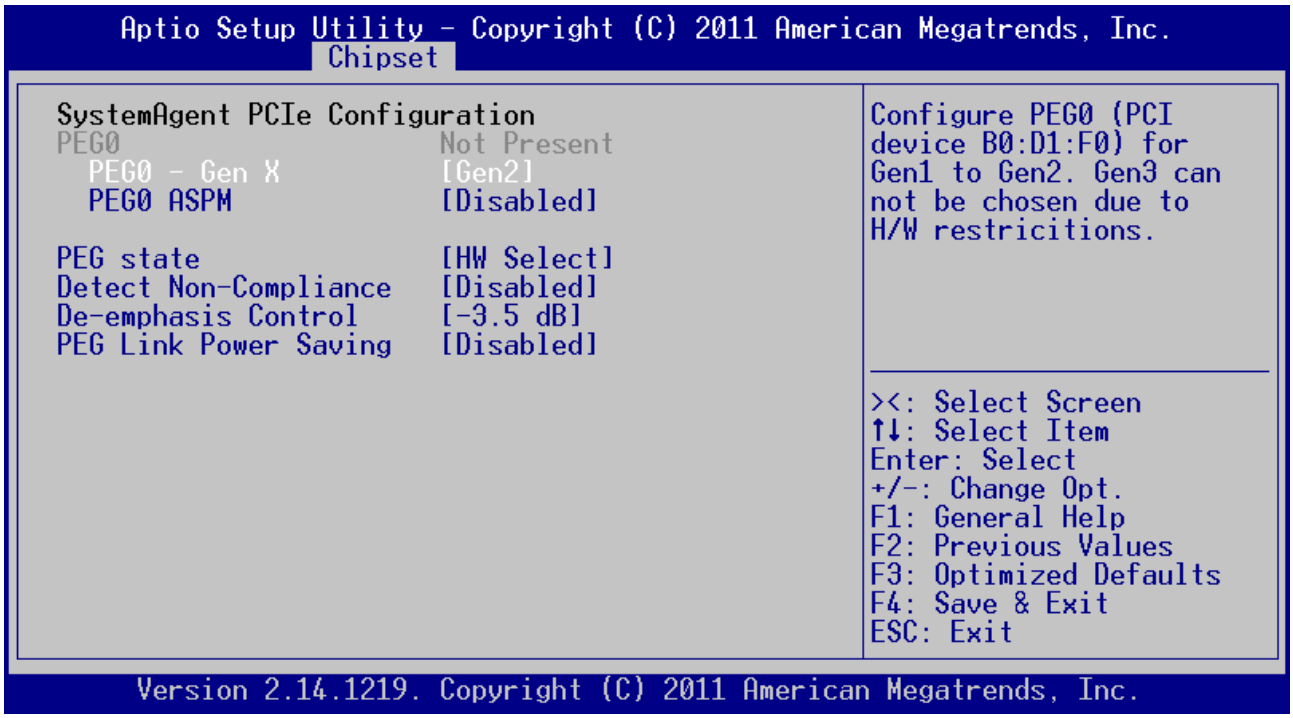


Feature	Options	Description
Prim IGFX Boot Disp	**Auto** CRT LVDS EFP 1 EFP 2 EFP 3 LFP2	Select the Integrated Graphics Video Device which will be activated during POST. This has no effect if external graphics devices are present
Sec IGFX Boot Disp	**Disabled** CRT LVDS EFP 1 EFP 2 EFP 3 LFP2	Select Secondary Integrated Graphics Display Device
Int. LVDS Panel Type	**AUTO** VGA 640×480 1×18 WVGA 800×480 1×18 SVGA 800×600 1×18 XGA 1024×768 1×18 XGA 1024×768 1×24 WXGA 1280×768 1×24 WXGA 1280×768 1×24 WXGA 1280×800 1×18 WXGA 1366×768 1×24 WXGA+ 1440×900 2×18 WXGA+ 1440×900 2×24 SXGA 1280×1024 2×18 SXGA 1280×1024 2×24 WSXGA+ 1680×1050 2×18 WSXGA+ 1680×1050 2×24 UXGA 1600×1200 2×18 UXGA 1600×1200 2×24 WUXGA 1920×1200 2×18 WUXGA 1920×1200 2×24	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item
Backlight Control	None/External PWM PWM Inverted **I2C**	Backlight Control Setting
Backlight Value	**128**	Set LCD backlight brightness (0-255)
SDVO Device	**Disabled** SDVO - DVI 1.0 SDVO - DVI-I SDVO - LVDS	Selects the SDVO Device
embedded DP	**Disabled** Enabled	Enabled the embedded Display Port device
EFP1 Type EFP2 Type EFP3 Type	DisplayPort Only **DP with HDMI/DVI** DP with DVI HDMI/DVI DVI only	Integrated HDMI/DisplayPort Configuration with External Connectors

Mode Persistence	**Disabled** Enabled	Enables/Disables Mode Persistence

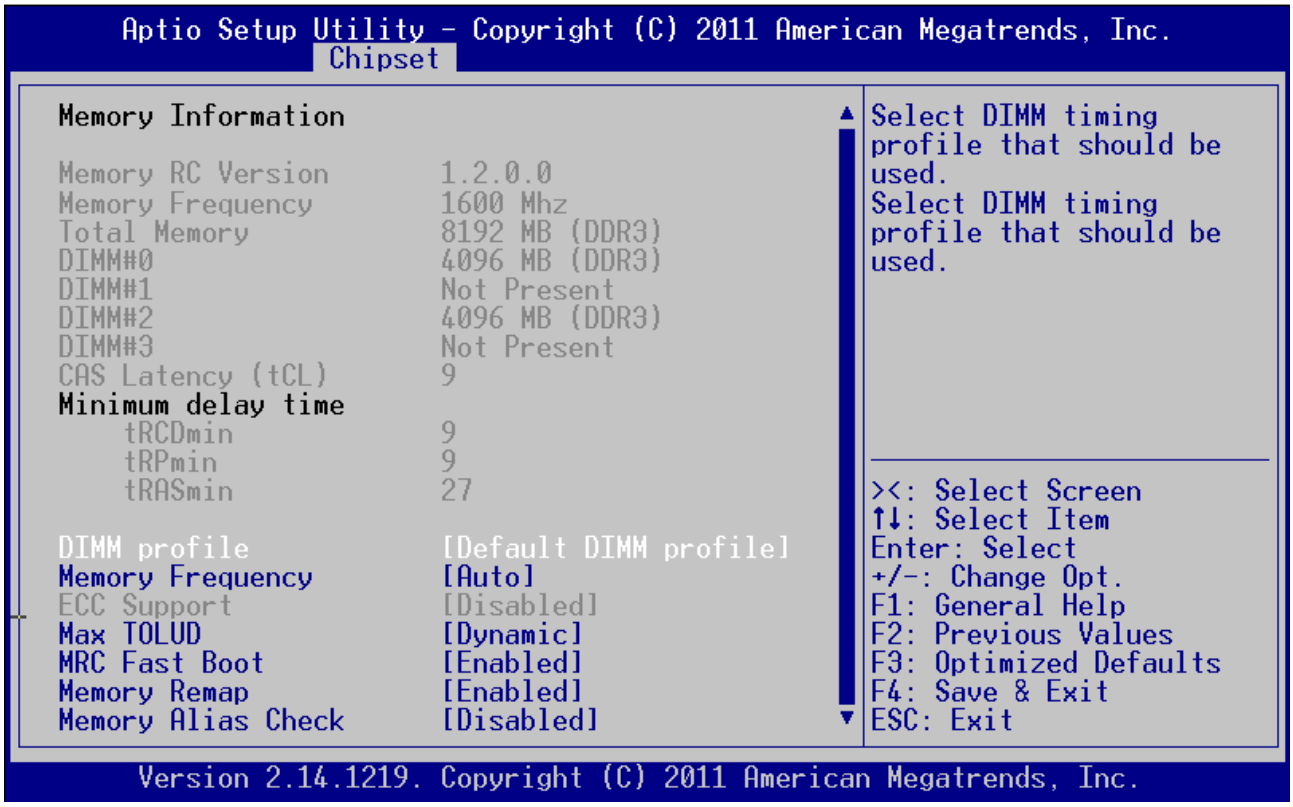
For SDVO2DVI solutions select 'SDVO - DVI 1.0' or 'SDVO - DVI-I'. For SDVO2CRT select 'SDVO - DVI-I'.

SystemAgent PCIe Configuration



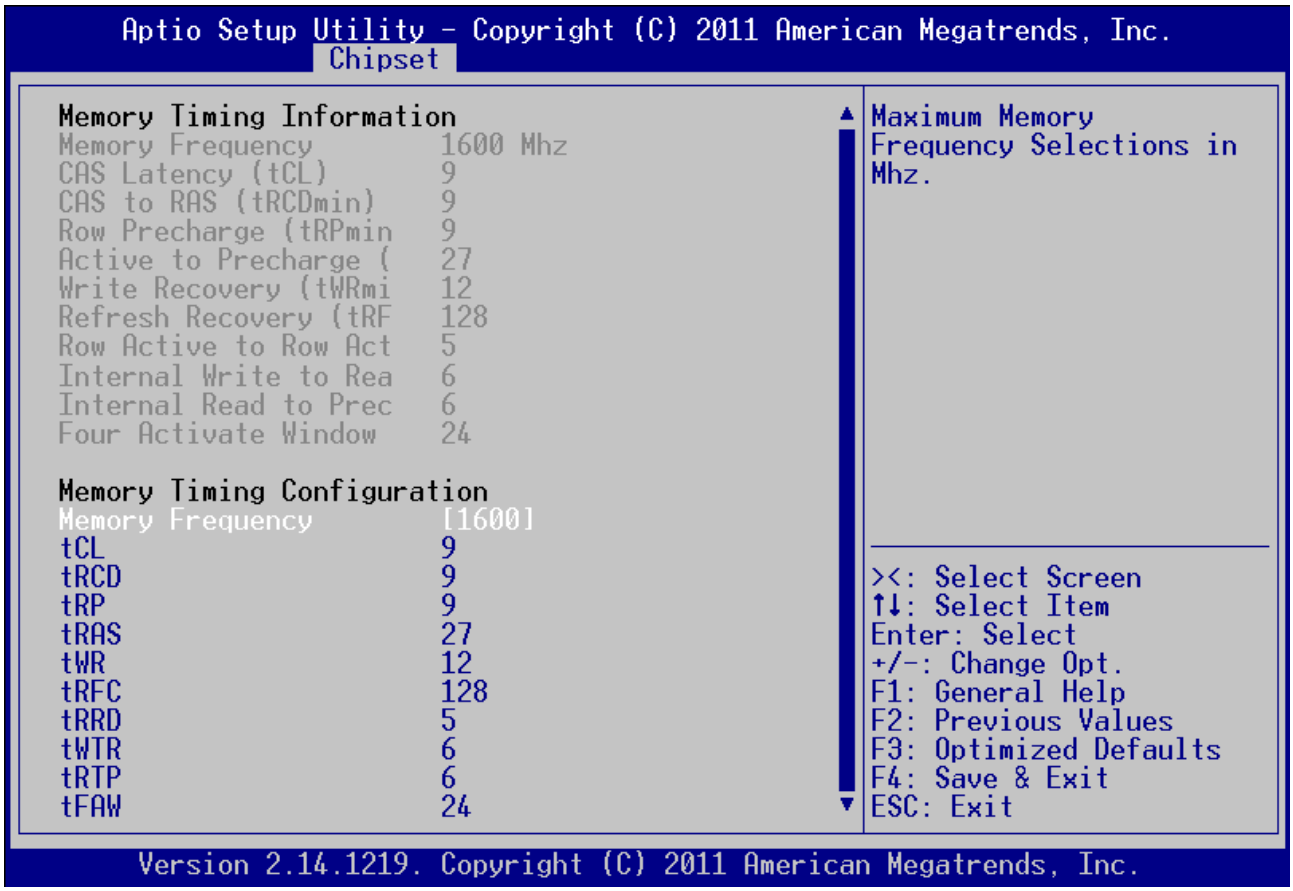
Feature	Options	Description
PEG0 - Gen X	Gen1 **Gen2**	Configure PEG0 B0:D1:F0
PEG ASPM	**Disabled** Auto ASPM L0s ASPM L1 ASPM L0sL1	Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device
ASPM L0s	Root Port Only Endpoint Port Only **Both Root and Endpoint Ports**	Enable PCIe ASPM L0s
PEG state	**HW Select** Disabled Enabled	Enable or disable the PEG slot. Option 'HW Select' controls PEG via PEG_ENABLE# signla
Detect Non-Compliance Device	**Disabled** Enabled	Detect Non-Compliance PCI Express Device in PEG
De-emphasis Control	-6 dB **-3.5 dB**	Configure the De-emphasis control on PEG
PEG Link Disabled	Enabled **Disabled**	Enable or disable PCIe link disable mechanism for additional power saving

Memory Configuration



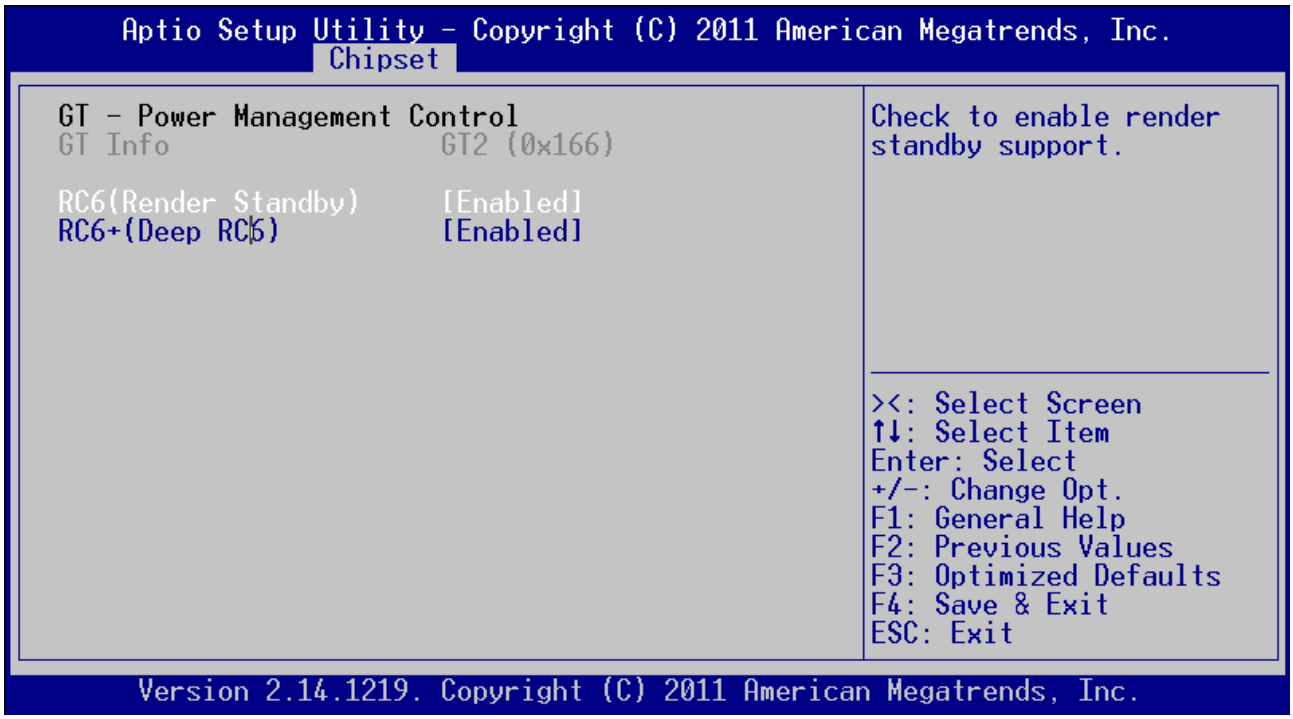
Feature	Options	Description
DIMM Profile	**Default DIMM profile** Custom Profile XMP profile 1 XMP Profile 2	Select DIMM timing profile that should be used
Memory Frequency	**Auto** 1067 1333 1600	Maximum Memory Frequency Selections in MHz
Max TOLUD	**Dynamic** 1 GB ... 3.25GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller. Manual TOLUD setting from 1GB to 3.25GB in 0.25GB steps
MRC FastBoot	Disabled **Enabled**	Enable/Disable MRC FastBoot
Memory Remap	Disabled **Enabled**	Enable/Disable Memory Remap above 4GB
Memory Alias Check	Enabled **Disabled**	Enable/Disable Memory Alias Check

Custom Memory Profile Control



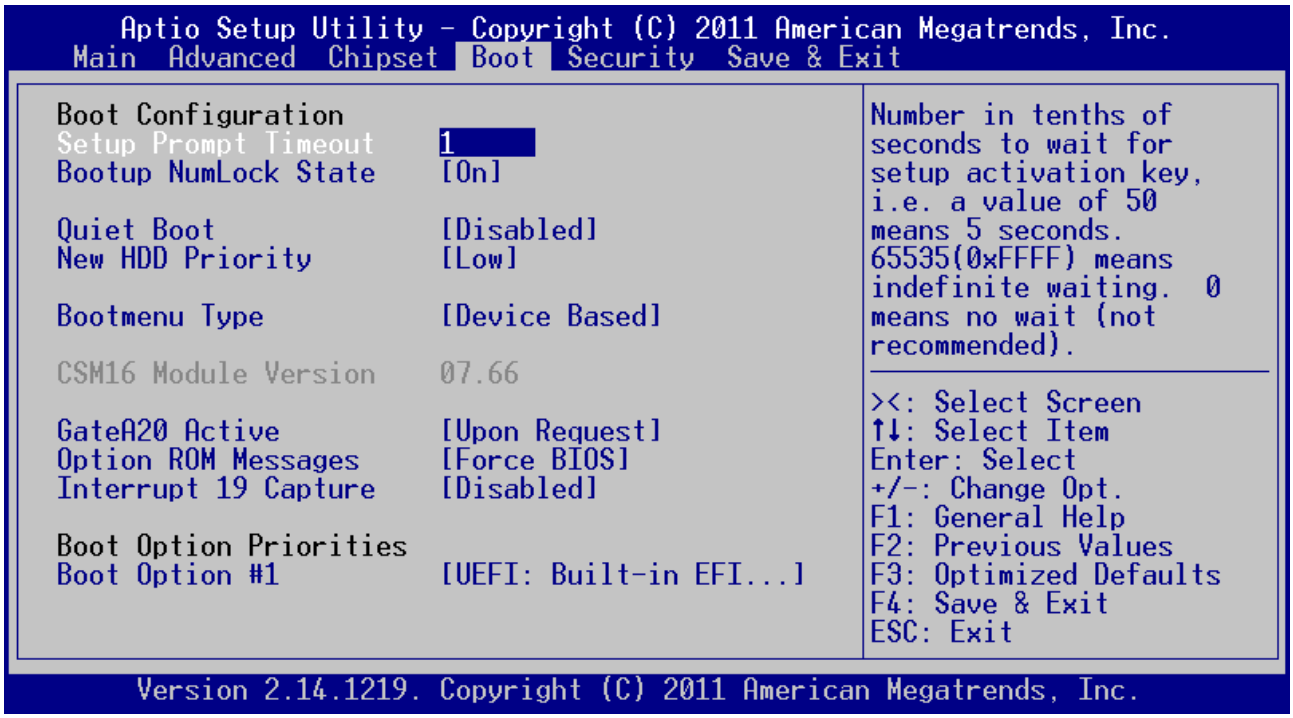
Feature	Options	Description
Memory Frequency	1067 1333 **1600** 1867 2133 2400 2667	Maximum Memory Frequency Selections in MHz
tCL	**9**	Cas Latency Range 4-18
tRCD	**9**	Row to Col Delay Range 1-38
tRP	**9**	Ras Precharge Range 1-38
tRAS	**27**	Ras Active Time 1-586
tWR	**12**	Min Write Recovery Time Range 1-38
tRFC	**128**	Min Refresh Recovery Delay Time 1-9363
tRRD	**5**	Min Row Active to Row Active Delay Time 1-38
tWTR	**6**	Min Internal Write to Read Command Delay Time 1-38
tRTP	**6**	Min Internal Read to Precharge Command Delay Time 1-38
tFAW	**24**	Min Four Activate Window Delay Time 1-586

GT - Power Management Control



Feature	Options	Description
RC6 (Render Standby)	Disabled **Enabled**	Check to enable render standby support
RC6+ (Deep RC6)	Disabled **Enabled**	Check to enable Deep RC6 (RC6+) support

8.5.4 Boot



Feature	Options	Description
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means idefinite waiting. 0 means no wait (not recommended)
Bootup NumLock State	**On** Off	Select the keyboard NumLock state
Quiet Boot	**Disabled** Enabled	Enables/Disables Quiet Boot option (Boot logo)
New HDD Priority	**Low** High	Boot priority for new connected HDD
Bootmenu Type	**Device Based** Port Based	Enables Device or Port based Bootmenu
Boot Port 1 ... 4	Disabled UEFI Shell SATA 0 ... 3 USB 0 ... 7 OPROM 1 OPROM2 **Any Device**	USB devices behind hubs are not supported by Port Based Bootmenu. Use Device Based Bootmenu for those devices
GateA20 Active	**Upon Request** Always	Upon Request: GA20 can be disabled using BIOS services. Always: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for Option ROM
Interrupt 19 Capture	**Disabled** Enabled	Enabled: Allows Option ROMs to trap INT19
Boot Option #1 Boot Option #2 Boot Option #3 ...	**Boot Device** Disabled	Set the system boot order by device group
Hard Drive BBS Priorities	-	Set the order of the legacy devices in this group
CD/DVD ROM Drive BBS Priorities	-	Set the order of the legacy devices in this group
Floppy Drive BBS Priorities	-	Set the order of the legacy devices in this group

Boot Option Priority

By default, AMI APTIO uses following boot priority if at least one device of a group is connected:

» Boot Option #1: Prio 1 Hard Disk

» Boot Option #2: Built-in EFI Shell

» Boot Option #3: Prio 1 HDD UEFI boot option

» Boot Option #4: Prio 1 CD/DVD ROM Drive

» Boot Option #5: Prio 1 Floppy UEFI boot option

» Boot Option #6: Prio 1 Floppy Drive

HDD and CD/DVD-ROM group internal drive priority

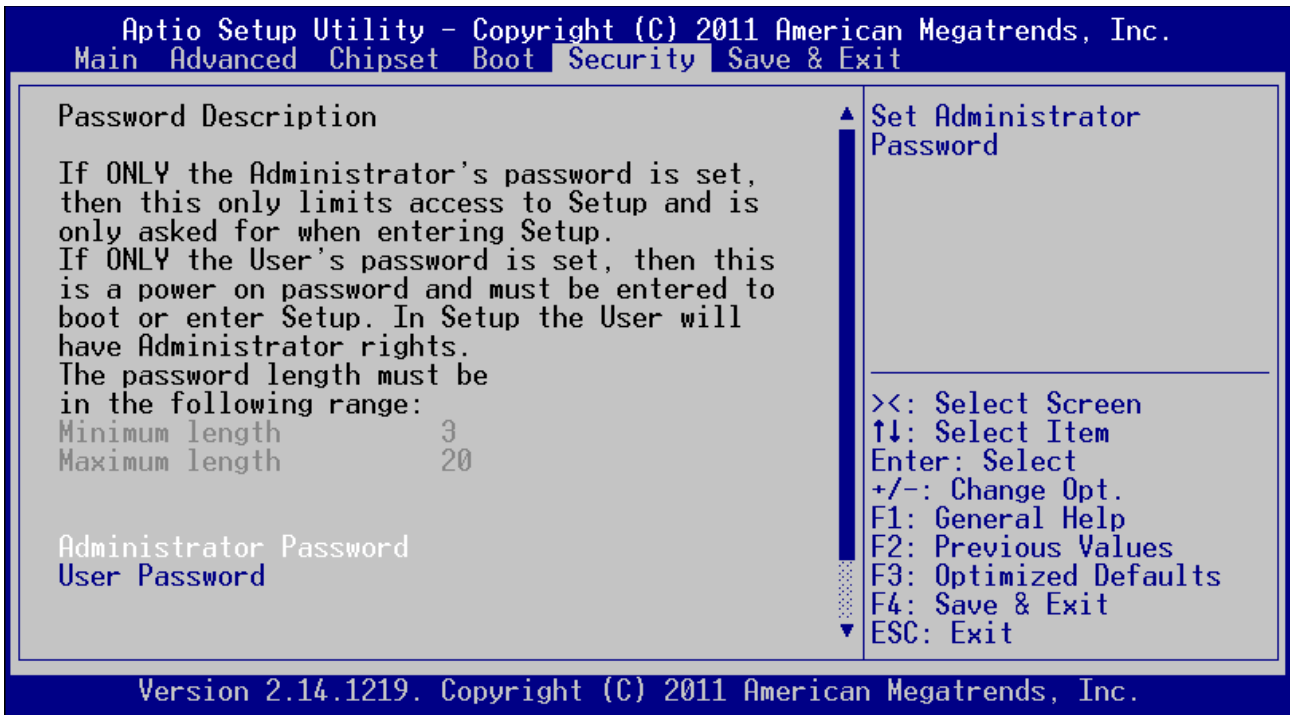
The internal device priority for Hard Disks and Optical drives is:

» 1. SATA #0-3

» 2. PATA

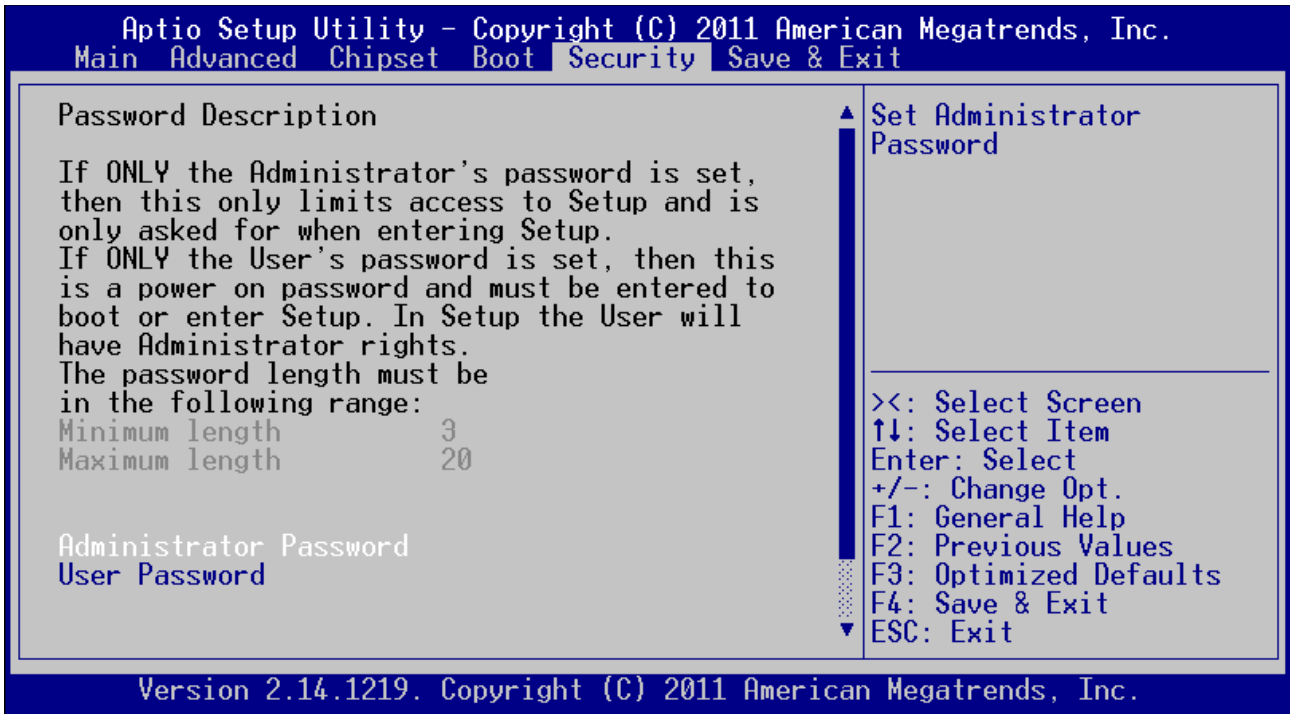
» 3. USB

8.5.5 Security



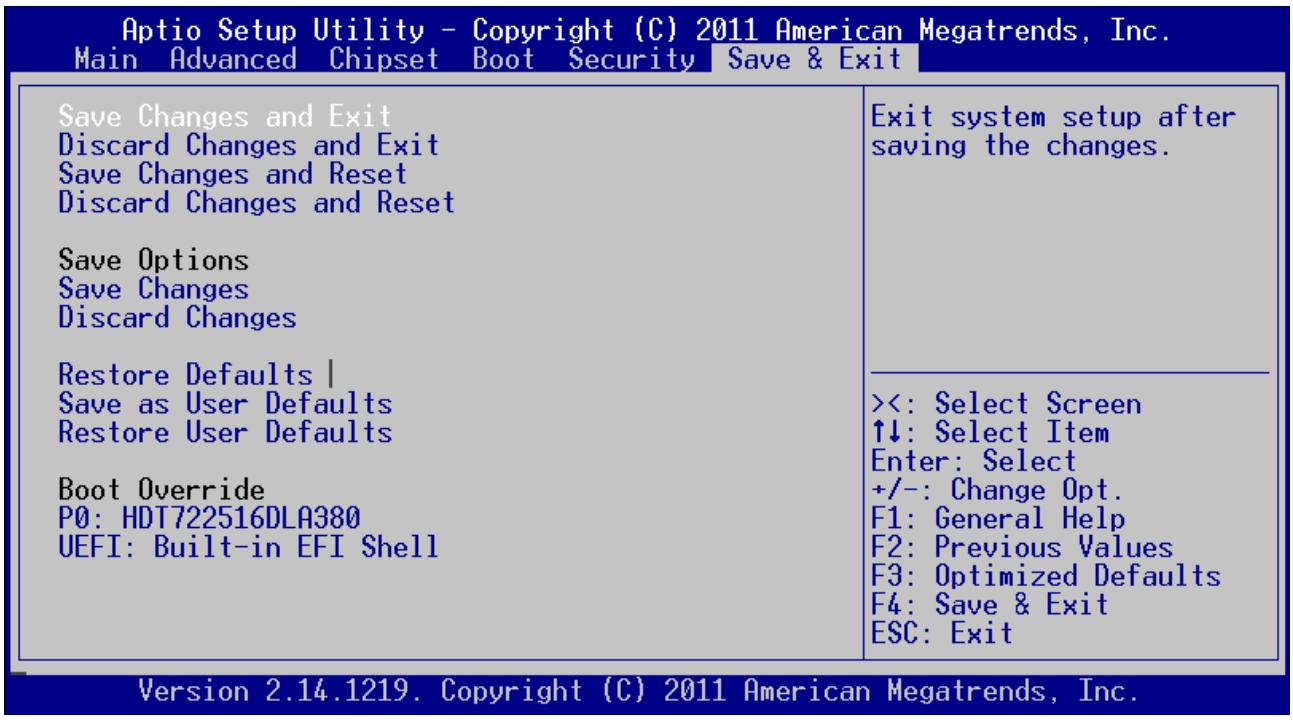
Feature	Options	Description
Set Administrator Password	-	Set the Administrator Password for Setup Access
User Password	-	Set User Password
HDDx	-	Set HDD Password

Set HDD Password



Feature	Options	Description
Set User Password	-	Set HDD User Password. Advisable to Power Cycle System after Setting Hard Disk Passwords
Set Master Password	-	Set HDD Master Password. Advisable to Power Cycle System after Setting Hard Disk Passwords

8.5.6 Save & Exit



Feature	Options	Description
Save Changes and Exit	-	Exit system setup after saving the changes
Discard Changes and Exit	-	Exit system setup without saving any changes
Save Changes and Reset	-	Reset system after saving the changes
Discard Changes and Reset	-	Reset system without saving any changes
Save Changes	-	Save changes made so far to any of the setup options
Discard Changes	-	Discard changes made so far to any of the setup options
Restore Defaults	-	Restore/Load Default values for all the setup options
Save as User Defaults	-	Save the changes made so far as User Defaults
Restore User Defaults	-	Restore the User Defaults to all the setup options
Boot Override	List of all boot options	Boot directly from selected device

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