JFLEX-SERIALGPIO1

Product Manual

Document Revision 2.1

Table of Contents

1 USER INFORMATION

1.1 About This Manual

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Products labeled and sold under the Kontron Embedded Modules name (formerly JUM*Pte*c) are now considered Kontron products for all practical purposes, including warranty and support.
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Kontron Embedded Modules is certified to ISO 9000 standards.

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This Kontron Embedded Modules product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules will at ist discretion decide to repair or replace defective products.
Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.
You may receive a bill for test costs if Kontron Embedded Modules finds no fault with the product. You also may receive a bill for repairs if a product's warranty has expired.
For warranty service or repair, return the product to a Kontron Embedded Modules service facility listed in the Technical Support section of this document.
The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.
Kontron Embedded Modules will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules that are caused by a faulty Kontron Embedded Modules product.

1.7 Technical Support

Technicians and engineers from Kontron Embedded Modules and/or ist subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems. Before contacting Kontron Embedded Modules technical support, please consult our **Web site** for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by email or telephone. The table below lists technical support contacts and service facilities for Kontron Embedded Modules.

Asia	Europe	North/South America
Kontron Asia	**Kontron Embedded Modules**	**Kontron Americas**
5F-1, 341, Sec 4 Chung Hsiao E. Road Taipei, Taiwan	Brunnwiesenstr. 16 94469 Deggendorf – Germany	3988 Trust Way Hayward, CA 94545
Tel: +886 2 2751 7192	Tel: +49 (0) 991-37024-0	Tel: 510-732-6900
Fax: +886 2 2772 0314	Fax: +49 (0) 991-37024-104	Fax: 510-732-7655
http://www.jumptec.com.tw/ http://www.kontron.com.tw/	http://www.jumptec.de/ http://www.kontron.de/	http://www.adastra.com/ http://www.kontron.com/
		techsupport@jumptec.com

2 INTRODUCTION

2.1 JFLEX-SERIALGPIO1

The JFLEX-SERIALGPIO1 is an extension board for Kontrons Jrex 3,5'' embedded line SBC family.

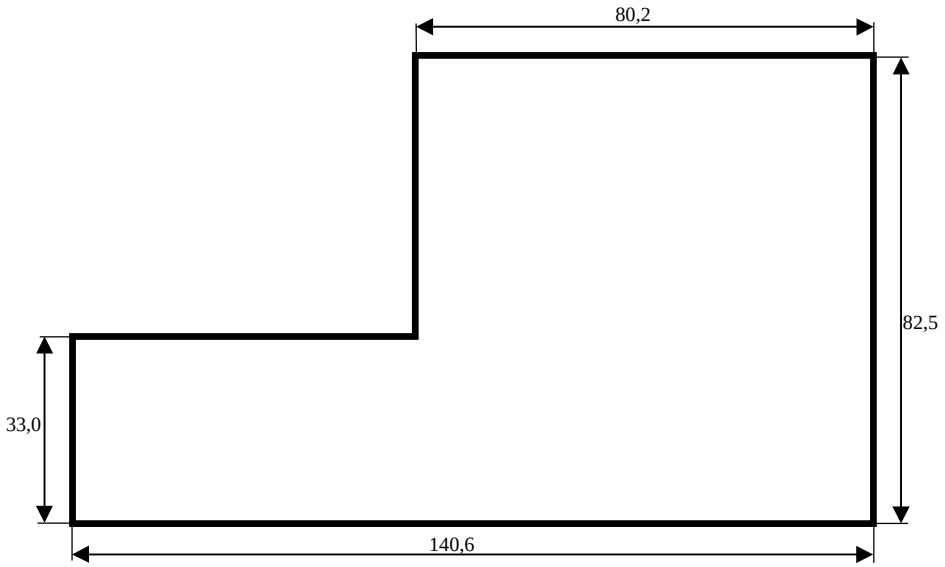
Following features are provided by the JFLEX-SERIALGPIO1:

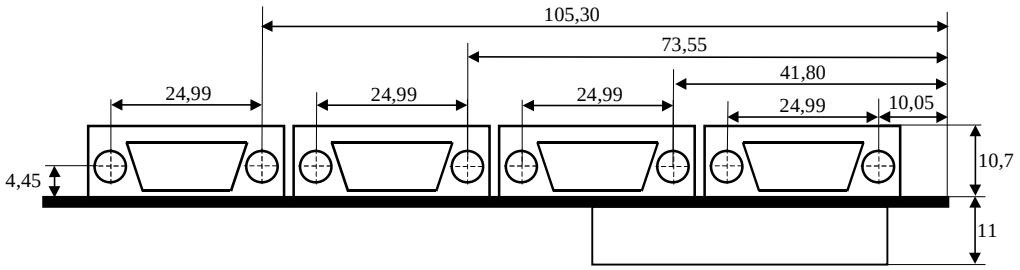
- 3 serial ports RS232 (optional TTL-Level signals)
- 1 serial port RS422/RS485
- 1 parallel port
- CAN port up to 1 Mbaud
- 4 x 8bit GPIO pins
- 2 USB ports

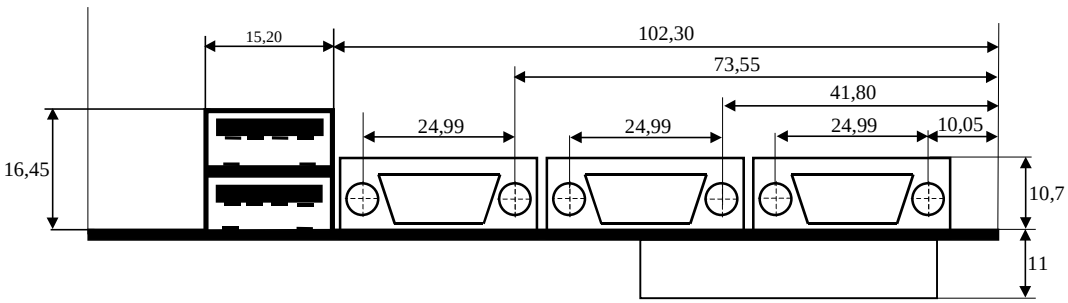
3 SPECIFICATIONS

3.1 Mechanical Specifications

- Mechanical: 140,6mm x 82,5mm L-shape







All dimensions are given in Millimeters [mm].

3.2 Electrical Specifications

3.2.1 Supply Voltage

- 5V DC +/- 5%
- 3,3V DC +/- 5%

3.2.2 Supply Voltage Ripple

- 100 mV peak to peak 0-20 MHz

1.1.1 Supply Current

- @ 3.3V max. 50mA
- @ 5V max. 200mA (without CAN)
- @ 5V max. 400mA (including CAN)

3.3 Environmental Specifications

3.3.1 Temperature

- Operating: 0 to + 60°C
- Storage: -10 to + 85 ° C

3.3.2 Humidity

- Operating: 10% to 90% (non condensing)
- Storage: 5% to 95% (non condensing)

To protect the external powerlines to peripheral devices the customer has to take care about:

- **The wires to the external device have the right diameter to withstand the max. available current.**
- **The housing of the external device fulfills the fire protecting requirements of IEC/EN 60950.**

4 MODULE FUNCTIONS

4.1 COM Ports A, B, C, D

The JFLEX-SERIALGPIO1 has four 16550-compatible serial ports:

- COM-A
- COM-B
- COM-C
- COM-D

Line drivers used for COMA through COMC conform to the IEEE RS-232C standard. COMD can be selected by jumper to work as RS422 transmitter or RS485 (default). RS485 can be 2-wire or 4-wire system.

4.1.1 Programming

When connected to a Jrex CPU module the COM ports can be activated and configured within the systems BIOS setup menu.

The configuration table can be found on I/O Device Configuration screen in the Advanced menu.

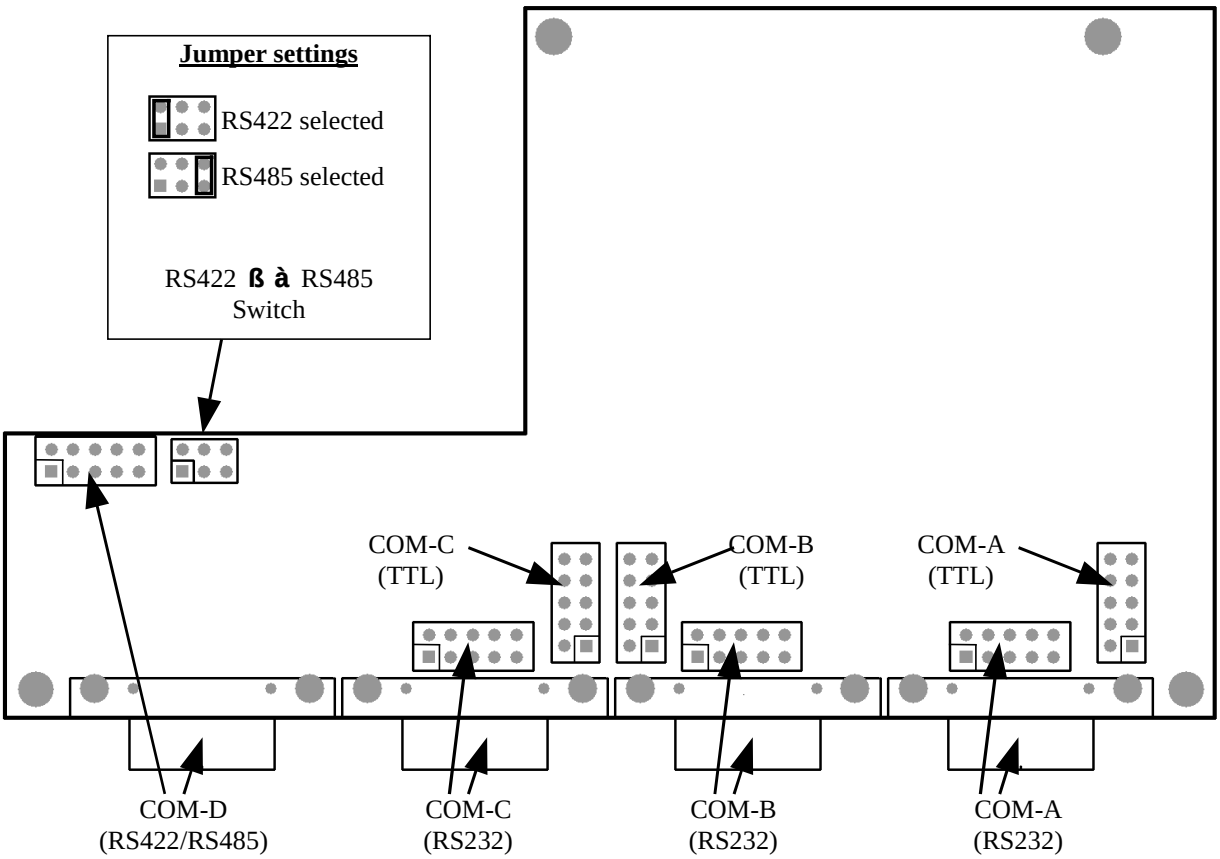
Note: The option "IrDA" in BIOS setup menu is not applicable to JFLEX-SERIALGPIO1. Do not enable this option for COM operation.

4.1.2 Connectors

RS232 devices at COM-A ...C can either be connected to the DSUB-9 connector at the front or internally at a 10-pin header. TTL-level based devices can be connected at COM-A ...C through an additional 10-pin header.

Only one device can be connected at an individual port at one time.

COM-D can be connected to an RS485 (or RS422) network either through the DSUB-9 connector at the front or the internal 10-pin header.



4.1.3 Connector Pinouts

COM-A, B, C (RS232 & TTL)			
Signalname	Direction	Pin Header	DSUB-9
RLSD (A, B, C)	In	1	1
DSR (A, B, C)	In	2	6
SIN (A, B, C)	In	3	2
RTS (A, B, C)	Out	4	7
SOUT (A, B, C)	Out	5	3
CTS (A, B, C)	In	6	8
DTR (A, B, C)	Out	7	4
RI (A, B, C)	In	8	9
GND	--	9	5
VCC5	--	10	--

COM-D (RS422 / RS485)			
Signalname	Direction	Pin Header	DSUB-9
TXD+	Out	1	1
RXD+ / TXD+	In / Out	2	6
--	--	3	--
--	--	4	--
TXD-	Out	5	3
RXD- / TXD-	In / Out	6	8
--	--	7	--
--	--	8	--
GND	--	9	5
VCC5	--	10	--

For signal description please refer to additional literature.

4.2 LPT Port

The JFLEX-SERIALGPIO1 supports one enhanced parallel port.

ECP and EPP modes are supported.

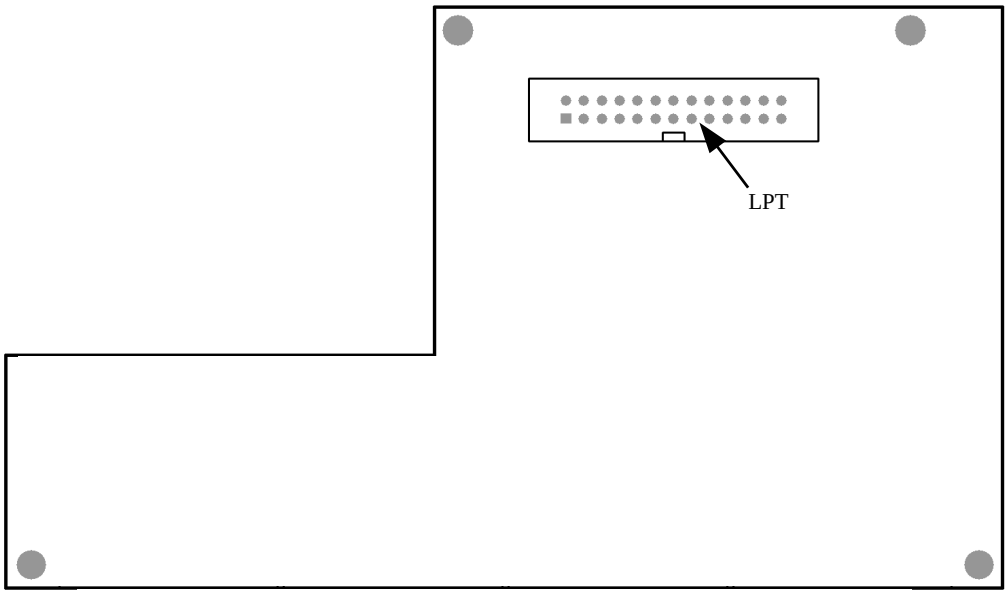
4.2.1 Programming

When connected to a Jrex CPU module the LPT port can be activated and configured within the systems BIOS setup menu.

The configuration table can be found on I/O Device Configuration screen in the Advanced menu.

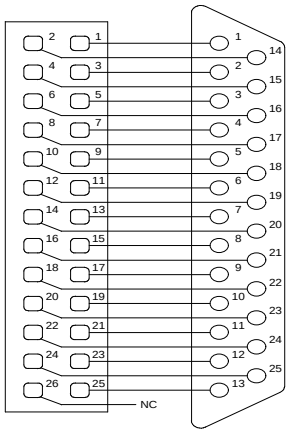
The parallel port is compatible with the parallel-port implementation used in the IBM PS-II-Parallel Adapter.

4.2.2 Connector



4.2.3 Adapter Cable

You can use an adapter cable to change from the 26-pin header style of the JFLEX-SERIALGPIO1 a more common 25-pin female D-sub.



26-pin Header to 25-pin D-Sub conversion

4.2.4 Connector Pinout

Pin	Signalname	In / Out	DSUB-25 (need Adapter)
1	STB#	Out	1
3	PD0	I/O	2
5	PD1	I/O	3
7	PD2	I/O	4
9	PD3	I/O	5
11	PD4	I/O	6
13	PD5	I/O	7
15	PD6	I/O	8
17	PD7	I/O	9
19	ACK#	in	10
21	BUSY#	in	11
23	PE	in	12
25	SLCT#	in	13
2	AFD#	out	14
4	ERR#	in	15
6	INIT#	out	16
8	SLIN#	out	17
26	VCC5	--	NC
10, 12, 14, 16, 18, 20, 22, 24	GND	--	18 – 25

For signal description please refer to additional literature.

4.3 CAN Interface

The JFLEX-SERIALGPIO1 board uses a Philips SJA1000 CAN Controller. This interface is capable of transmitting and receiving at a speed of 1 Mbaud.

The SJA1000 serial-communications controller performs serial communication, following the CAN protocol. The controller, with minimal interaction from the host microcontroller or CPU, performs all serial-communication functions such as:

- Transmitting and receiving messages
- Filtering messages
- Transmitting searches
- Interrupting searches

The Philips PCA82C250 universal CAN transceiver serves as the interface between the CAN protocol controller and the physical bus.

Two 6N137 optocouplers decouples both CAN lines from onboard electronics. When using optical decoupling the user must apply power for the line driver and optocoupler through the CAN connector.

Optical decoupling can be optionally overridden by two jumpers. Then the line driver is supplied from onboard power.

On the JFLEX-SERIALGPIO1 board, the CAN bus terminates with a 120 Ohm resistors across CAN_L and CAN_H. Depending on the network topology employed and the total bus length, a modified termination network may be desirable in some applications. Under those circumstances, contact Kontron technical support for assistance.

4.3.1 Configuration

The CAN controller uses the onboard parallel port to interface to the system.

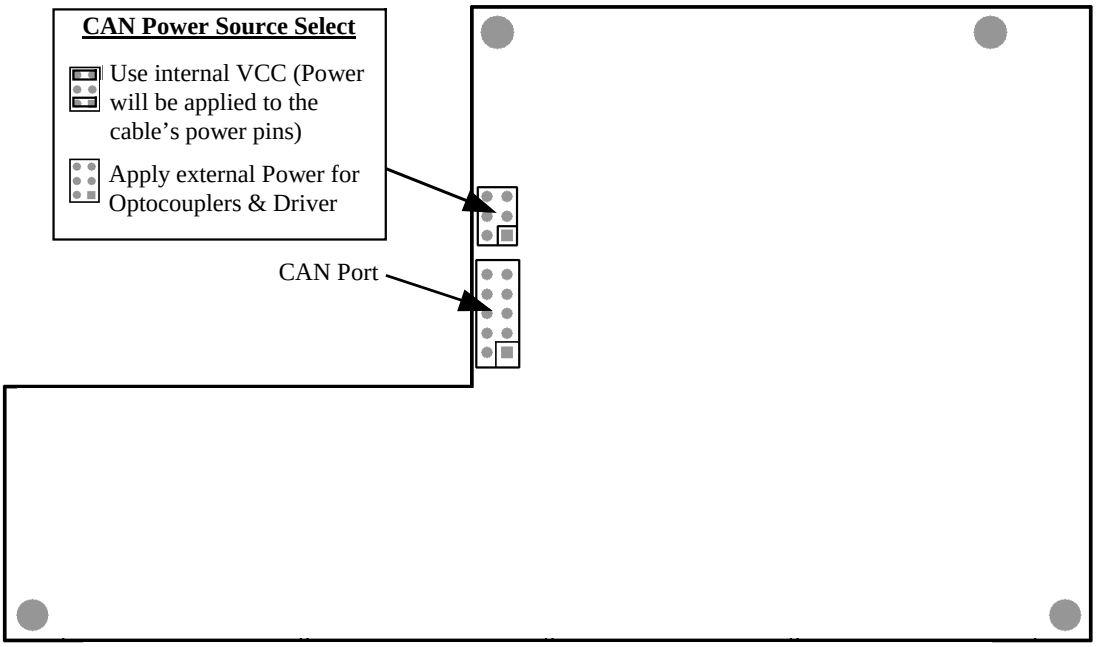
To activate the CAN interface enter BIOS setup and enable the external LPT.

Make sure the LPT port is configured as „Auto“, „EPP“

The configuration table can be found on I/O Device Configuration screen in the Advanced menu.

A driver for Windows operating systems is available.

4.3.2 Connector



4.3.3 Connector Pinout

Pin	Signalname	DSUB-9 (need Adapter)	notes
1	--	1	
2	GND	6	Connected to internal GND
3	CAN_L	2	Low Line of CAN Port
4	CAN_H	7	High Line of CAN Port
5	CANGND	3	Connect to external Power Supply GND
6	--	8	
7	--	4	
8	CANVCC	9	Connect to external Power Supply VCC
9	--	5	
10	--	--	

4.4 4 x 8-bit GPIO Ports

The JFLEX-SERIALGPIO1 Module provides 32 GPIO Pins arranged as 4 x 8-bit ports. Each pin is individually configurable as an input or Open-Drain output. When configured as output the user must provide a pullup resistor to the desired output voltage level. All output pins have 12mA drive strength. The output LowLevel is max. 0,4V.

4.4.1 Programming using 32-Bit Operating Systems

Also all GPIO pins can be read or written using JIDA32 protected mode functions. Additional information on how to use JIDA32 and sample code can be found on the Kontron web page.

4.4.2 Programming using 16-Bit Operating Systems

The W83697uf Super I/O controller consists of several logical devices, which correspond to individual functionality. Logical Device 9 reflect the GPIOs 2-4 and Logical Device 8 reflect the GPIO 5. Each Logical Device has it´s own configuration registers. The designer can access the desired configuration Registers by selecting a logical device through the Extended Functions Data Register (I/O port index address 4Eh and data address 4Fh).

Configuration Register Logical Device 9 (GPIO 2-4)

Index F0h: GPIO2 selection register. Default 0FFh
Index F3h: GPIO3 selection register. Default 0FFh
Index F6h: GPIO4 selection register. Default 0FFh
When set to a ‘1’ respective GPIO pin is programmed as an input port
When set to a ‘0’ respective GPIO pin is programmed as an output port

Index F1h: GPIO2 data register. Default 00h
Index F4h: GPIO3 data register. Default 00h
Index F7h: GPIO4 data register. Default 00h
If GPIO is programmed to be an output port, then the respective bit can be written, else if the GPIO is programmed as input port , then the respective bit can be read.

Configuration Register Logical Device 8 (GPIO 5)

Index F0h: GPIO5 selection register. Default 0FFh
When set to a ‘1’ respective GPIO pin is programmed as an input port
When set to a ‘0’ respective GPIO pin is programmed as an output port

Index F1h: GPIO5 data register. Default 00h
If GPIO is programmed to be an output port, then the respective bit can be written, else if the GPIO is programmed to be an input port , then the respective bit can be read.

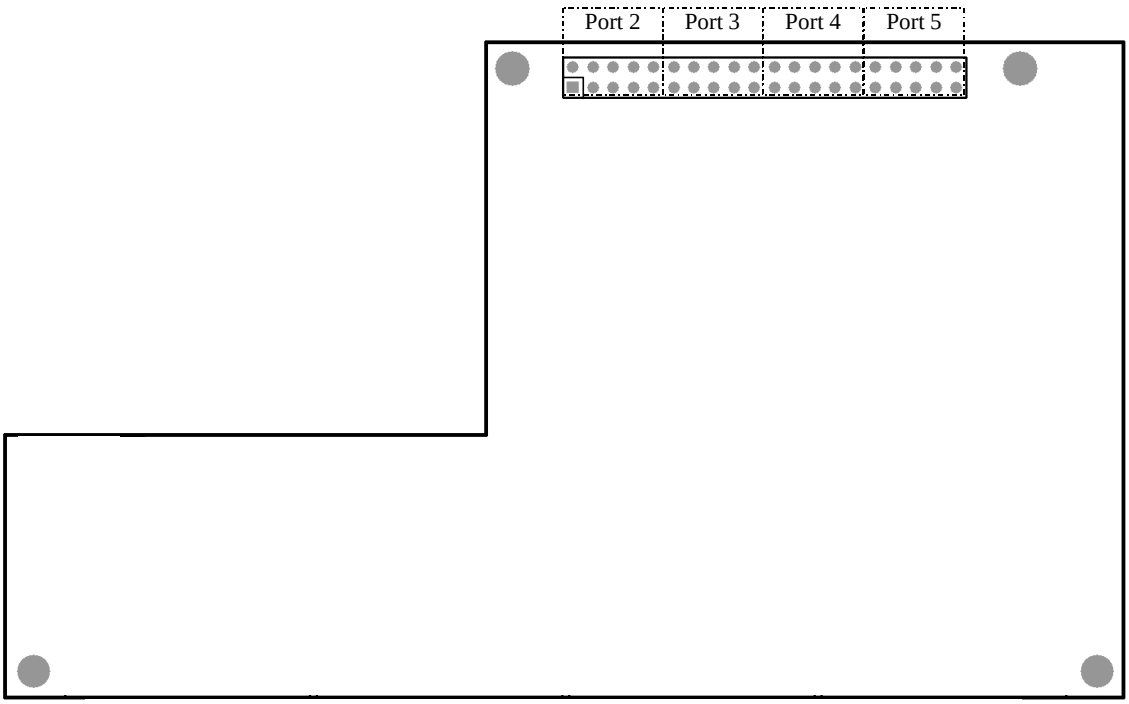
Programming example for GPIO3

```
W83697_IOBASE           EQU     04Eh          ;base address for index/data port
W83697_CONFIG_ENABLE    EQU     087h          ;data for unlock sequence
W83697_CONFIG_DISABLE   EQU     0Aah          ;data for lock sequence

;+-------------------------------------------------------------------------
;
; sioGpio3ReadData – read data from GPIO3
;
;       Entry:
;        None
;       Exit:
;        AH: input value
;
sioGpio3ReadData    PROC NEAR PUBLIC
      pushf                             ; no INTs while accessing
      cli                               ; W83697UF devices.

      Mov    al, 07h                    ; device selection register 07h
      mov    ah, 09h                    ; select logical device
      call   sioRegWrite8               ;(GPIO port 2-4).

      Mov    al, 0F3h                   ; GPIO3 selection register
      mov    ah, 0FFh                   ; set to be an input port
      call   sioRegWrite8

      mov    al, 0F4h                   ; GPIO3 data register
      call   sioRegRead8                ; read data from port

      popf
      ret
sioGpio3ReadData    ENDP

;+-------------------------------------------------------------------------
;
; sioGpio3WriteData – write data to GPIO3;
;       Entry:
;        AH: output value
;       Exit:
;        None
;
sioGpio3WriteData   PROC NEAR PUBLIC
      push   ax                         ; store output value
```

```
      pushf                             ; no INTs while accessing
      cli                               ; W83697UF devices.

      Mov    al, 07h                    ; device selection register 07h
      mov    ah, 09h                    ; select logical device 9
      call   sioRegWrite8               ;(GPIO port 2-4).

      Mov    al, 0F3h                   ; GPIO3 selection register
      mov    ah, 000h                   ; set to be an output port
      call   sioRegWrite8

      pop    ax                         ; restore output value
      mov    al, 0F4h                   ; GPIO3 data register
      call   sioRegWrite8               ; write data to port

      popf
      pop    ax
      ret
sioGpio3ReadData    ENDP


;+-------------------------------------------------------------------------
;
;       sioRegRead8 – reads an 8-bit SIO configuration register
;
;       Entry:
;        AL – register index
;
;       Exit:
;        AH – register value
;
sioRegRead8    PROC NEAR PUBLIC
      pushf                             ; no INTs while SIO configuration
      cli                               ; register access.
      Push   dx

      mov    ah, al                     ; save register index.

      Mov    dx, W83697_IOBASE          ; port 4Fh – perform unlock mechanism.
      Mov    al, W83697_CONFIG_ENABLE
      out    dx, al
      out    dx, al

      mov    al, ah                     ; write register index.
      Out    dx, al
      xchg   ah, al

      inc    dx                         ; port 4Fh – read register data .
      in     al, dx
      xchg   ah, al

      push    ax                        ; Save index and data.

      Dec    dx                         ; port 4Eh – perform lock mechanism.
      Mov    al, W83697_CONFIG_DISABLE
      out    dx, al

      pop     ax
      pop     dx
      popf
      ret
sioRegRead8    ENDP
```

```
;+-----------------------------------------------------------------------------
;
;       sioRegWrite8 – writes an 8-bit SIO configuration register
;
;       Entry:
;        AL – register index
;        AH – register value
;
;       Exit:
;        none
;
sioRegWrite8   PROC NEAR PUBLIC
      pushf                             ; no INTs while SIO2 configuration
      cli                               ; register access.
      Push   dx
      push   ax

      mov    dx, W83697_IOBASE          ; port 4Eh – perform unlock mechanism.
      Mov    al, W83697_CONFIG_ENABLE
      out    dx, al
      out    dx, al

      pop    ax                         ; port 4Eh – write register index.
      Push   ax
      out    dx, al

      mov    al, ah                     ; port 4Fh – write register data.
      Inc    dx
      out    dx, al

      dec    dx                         ; port 4Eh – perform lock mechanism.
      Mov    al, W83697_CONFIG_DISABLE
      out    dx, al

      pop    ax
      pop    dx
      popf
      ret
sioRegWrite8   ENDP
```

4.4.3 Connector



4.4.4 Connector Pinout

GPIO Port 2		GPIO Port 3		GPIO Port 4		GPIO Port 5	
Pin Nr.	Pin Name	Pin Nr.	Pin Name	Pin Nr.	Pin Name	Pin Nr.	Pin Name
1	GND	11	GND	21	GND	31	GND
2	VCC5	12	VCC5	22	VCC5	32	VCC5
3	GPIO_20	13	GPIO_30	23	GPIO_40	33	GPIO_50
4	GPIO_21	14	GPIO_31	24	GPIO_41	34	GPIO_51
5	GPIO_22	15	GPIO_32	25	GPIO_42	35	GPIO_52
6	GPIO_23	16	GPIO_33	26	GPIO_43	36	GPIO_53
7	GPIO_24	17	GPIO_34	27	GPIO_44	37	GPIO_54
8	GPIO_25	18	GPIO_35	28	GPIO_45	38	GPIO_55
9	GPIO_26	19	GPIO_36	29	GPIO_46	39	GPIO_56
10	GPIO_27	20	GPIO_37	30	GPIO_47	40	GPIO_57

4.5 USB Interface

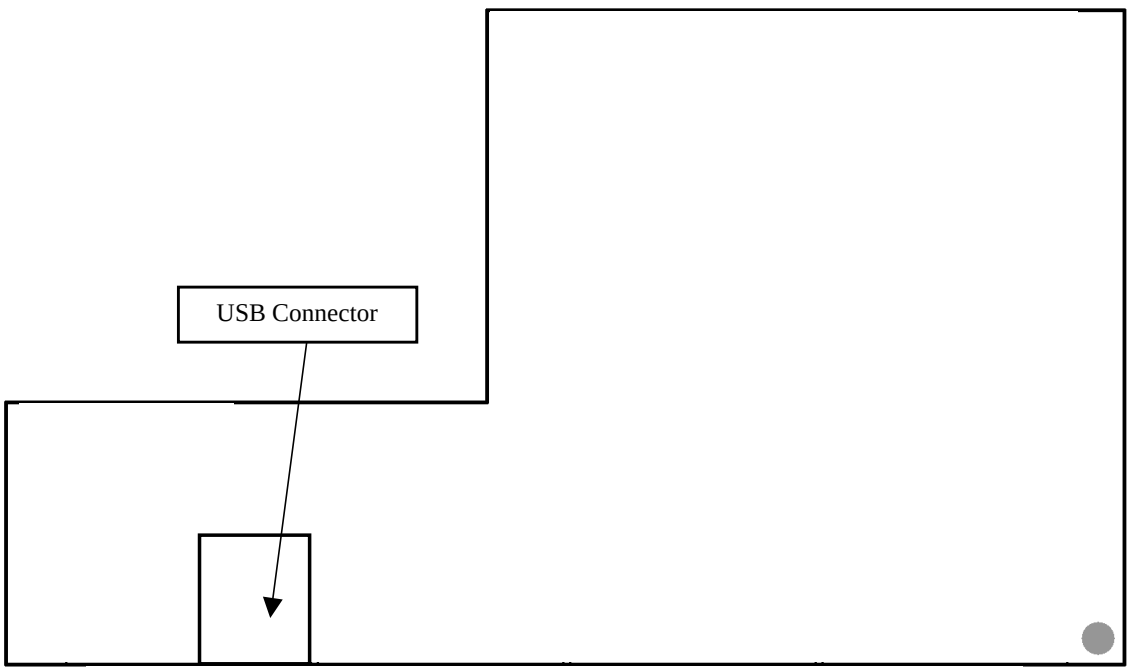
4.5.1 General description

The JFLEX-SERIALGPIO1 supports two USB ports. You can expand the USB ports by adding external hubs up to an amount of 127 USB peripherals per port.

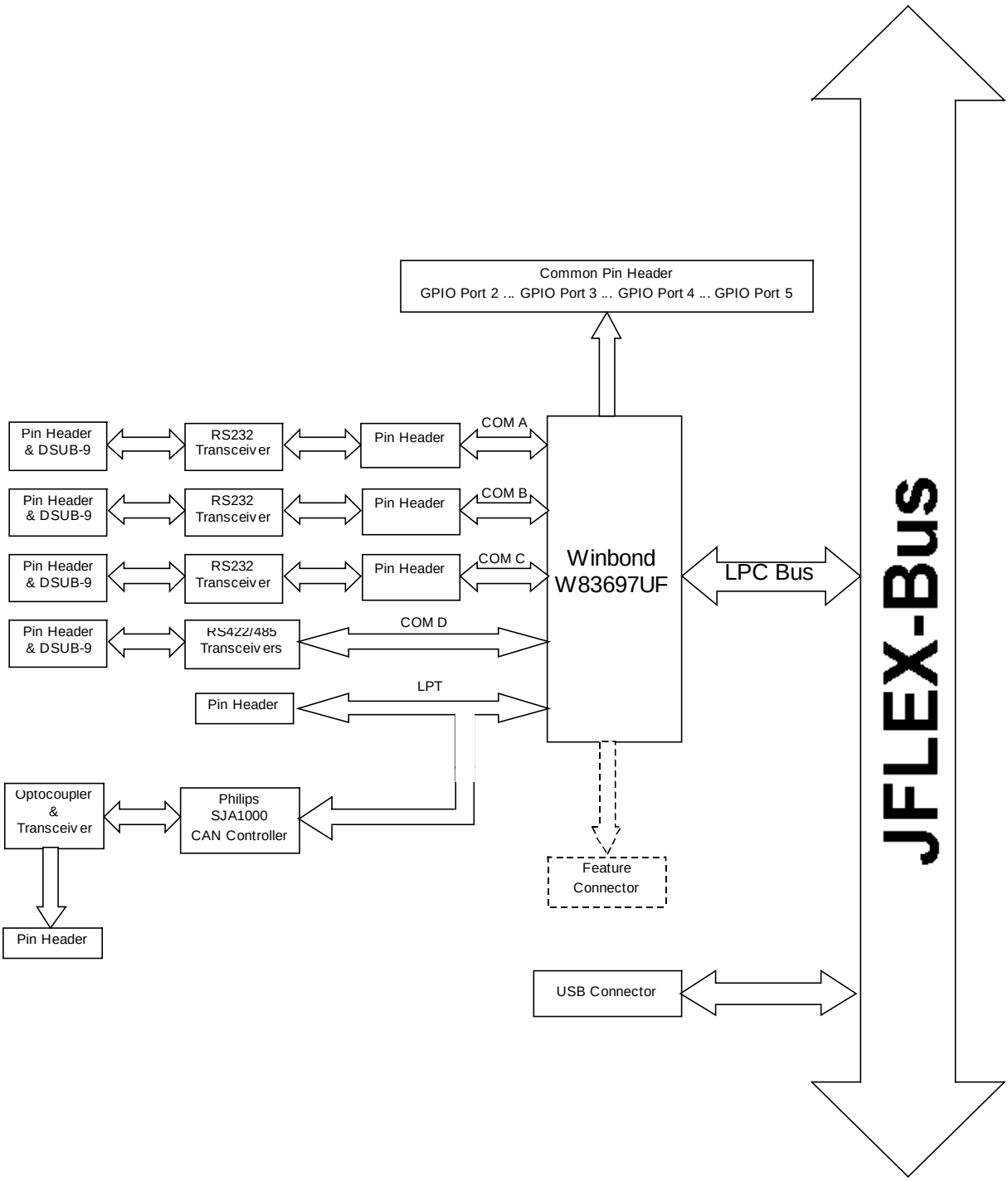
4.5.2 Connector Pinout

Pin	Function
1	USB1_+5V
2	USB1-
3	USB1+
4	USB1_GND
5	USB2_+5V
6	USB2-
7	USB2+
8	USB2_GND

4.5.3 Connector



5 APPENDIX A: BLOCK DIAGRAM



6 APPENDIX B: LITERATURE AND STANDARDS

Below is a list of information sources to help you to further understand PC architecture.

6.1 Buses and General PC Architetcure

6.1.1 PCI

PCI spec. @ http://www.pcisig.com/home/

- The PCI-SIG provides a forum for ist ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

6.1.2 USB

USB spec. @ http://www.usb.org/

USB Implementers Forum, Inc. Is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology.

6.1.3 AC ’97

AC ’97 spec. @ http://www.intel.com/labs/media/audio/

The specification defines the Audio Codec ’97 (AC ’97) Architecture and Digital Interface (AC-link) specifically designed for implementing audio and modem I/O functionality in PC systems. This specification does not explicitly define the companion AC ’97 Digital Controller component (sometimes referred to or abbreviated as DC ’97), which typically varies in features and implementation, but is AC ’97 compliant with this specification.

1.1.2 LPC

LPC spec. @ http://www.intel.com/design/chipsets/industry/lpc.htm

The Low Pin Count (LPC) Interface Specification for legacy I/O has facilitated the industry's transition toward ISA-less systems.

The LPC Interface allows the legacy I/O motherboard components, typically integrated in a Super I/O chip, to migrate from the ISA/X-bus to the LPC Interface, while retaining full software compatibility. The LPC Specification offers several key advantages over ISA/X-bus, such as reduced pin count for easier, more cost-effective design. The LPC Interface Specification is software transparent for I/O functions and compatible with existing peripheral devices and applications.

The LPC Interface Specification describes memory, I/O and DMA transactions. Unlike ISA, which runs at 8MHz, it will use the PCI 33MHz clock and will be compatible with more advanced silicon processes.

6.2 RS232C, RS485

- EIA-232-E Interface between data terminal equipment and date circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)

- National Semiconductor's Interface Data Book includes any applications notes. These notes are also available online at http://www.national.com/. A search engine is provided to search the text of the available application notes. Entering „232“ as search criteria to get a current list of related application notes.

- The link www.rs485.com provides detailed information about RS485 and RS422 interfaces.

7 APPENDIX C: DOCUMENT REVISION HISTORY

Version	Date	Edited by	Changes
0.1	16.10.2003	BAJ	preliminary manual created
0.2	23.10.2003	BAJ	minor changes
0.3	06.11.2003	BAJ	Added GPIO programming guidelines
1.0	10.11.2003	BAJ	First public release
1.1	27.02.2004	BAJ	Minor changes in CAN part
2.0	16.03.2004	AST	Added USB documentation
2.1	05.05.2004	TJO	Corrected some dimensions on page 7