BittWare’s T2-PMC (T2PM) DSP board features the ADSP-TS201 TigerSHARC processor from Analog Devices. To take full advantage of this high-performance DSP, this multiprocessor PCI Mezzanine Card (PMC) implements BittWare’s ATLANTiS (Advanced Transfer Link Architecture for New TigerSHARC) architecture, which combines robust TigerSHARC processing with the versatile Virtex-II Pro FPGA from Xilinx to offer ultra high performance and unprecedented I/O bandwidth.

The T2PM matches a cluster of four ADSP-TS201 TigerSHARCs with:
- High-bandwidth, low-latency off-board I/O, reconfigurable for nearly any application
- High-speed interprocessor communication network to facilitate scalability
- SharcFIN PCI-DSP bridge for integrating DSPs with PCI bus and other peripherals
- Comprehensive software for ease-of-use

The board also provides a large on-board bank of SDRAM and flash memory for hostless boot.

**High-Performance TigerSHARC Processing**

The T2PM features a cluster of four ADSP-TS201 TigerSHARC DSPs, which are interconnected by a 64-bit, 83.3 MHz cluster bus. The ADSP-TS201 processor operates at up to 600 MHz (500 MHz standard, 600 MHz special order), providing 3.6 GFLOPS of peak processing power. Because of its superscalar architecture, the ADSP-TS201 is also efficient at fixed-point processing, with each DSP supporting 14.4 BOPS of processing. Along with 24 Mbits of on-chip RAM, each DSP also boasts four high-speed LVDS link ports running at up to 1 GB/sec each. Two link ports from each DSP create an interprocessor communications ring, and the remaining two link ports are routed to the on-board FPGA.

**SharcFIN PCI-DSP Bridge**

The T2PM features a BittWare SharcFIN PCI-DSP bridge chip that gives the DSPs low-overhead access to the host via the 64-bit, 66 MHz PCI interface. The SharcFIN also provides a general purpose peripheral bus that allows the DSPs to access the Flash and the FPGA control registers. It also provides host access to the DSPs, on-board SDRAM, Flash, and FPGA control registers.

**Features**

- One cluster of four ADSP-TS201 DSPs @ up to 600 MHz
  - 14.4 GFLOPS per board (3.6 GFLOPS of floating-point power per DSP)
  - 57.5 BOPS per board (14.4 BOPS of 16-bit processing per DSP)
  - 24 Mbits of on-chip RAM per DSP
  - Static superscalar architecture
  - Xilinx Virtex-II Pro FPGA (XC2VP30) featuring 3 million gates
  - ATLANTiS architecture featuring 4 GB/sec of external I/O throughput via Virtex-II Pro routing
  - 8 link ports @ up to 500 MB/sec each
  - 64 high-performance DIO (single-ended and/or LVDS)
  - 8 channels RocketIO™ high-speed serial transceivers
  - PMC form factor with BittWare’s PMC+ I/O extensions (64 DIO to FPGA)
  - Up to 256 MB of on-board SDRAM
  - 64-bit, 66 MHz PCI interface via BittWare’s SharcFIN PCI-DSP bridge
  - 8 MB of Flash memory
  - Two link ports per DSP dedicated for interprocessor communications
  - Complete software support, including remote control and debug, support for multiple run-time and host operating systems, and optimized function libraries
High-Bandwidth, Low-Latency Off-Board I/O
The T2PM boasts a tremendous amount of I/O bandwidth and options, including eight LVDS link ports, PMC interface with BittWare’s PMC+ I/O extensions, and eight RocketIO high-speed serial transceivers. Total potential I/O bandwidth is greater than 6 GB/sec.

Xilinx Virtex-II Pro FPGA
A Xilinx Virtex-II Pro (XC2VP30) FPGA adds tremendous flexibility to the board and is useful for routing communications, translating protocols, and implementing algorithms. It is used to implement eight on-board TigerSHARC link ports and supports a variety of external digital I/O (DIO), flags, and interrupts. 64 digital I/O pins are brought to the FPGA from the PMC user connector (PMC+). The Virtex-II Pro's eight RocketIO high-speed serial transceivers, which are brought off-board, provide additional external communications.

ATLANTIS: A Superior Architecture for a Superior Processor
To facilitate off-board I/O and provide communications routing and processing, the T2PM features BittWare’s ATLANTIS architecture, which is implemented in the Xilinx Virtex-II Pro FPGA. All off-board I/O for the board is routed through the FPGA, which can support a throughput of 4 GB/sec. By tightly integrating the DSPs, PCI bridge, PMC interface, and I/O peripherals with the on-board FPGA, ATLANTIS gives designers nearly infinite options for configuring and routing the I/O. The eight bi-directional TigerSHARC link ports routed to the ATLANTIS FPGA provide 4 GB/sec of data transfer between the DSP cluster and the FPGA. Using its eight RocketIO high-speed serial transceiver channels and the 64 pins of digital I/O available via the PMC user connector (PMC+), the FPGA can communicate off-board at greater than 4.8 GB/sec. It can be configured to connect the I/Os to each other or to the ADSP-TS201 link ports, allowing any combination of inputs and outputs to be routed together. Each digital I/O signal can also be individually configured as single-ended or LVDS.

ATLANTIS adds tremendous flexibility to the DSP subsystem, allowing system designers to route the link ports and digital I/O blocks as their specific applications require.

T2 Board Family
The T2PM is part of BittWare’s T2 board family, which features the ADSP-TS201 TigerSHARC DSP on a variety of platforms. The boards all feature a common, scalable architecture - ATLANTIS - and are available in PCI-X plug-in, PMC, VME, and 6U CompactPCI form factors.

T2PM Architectural Block Diagram
BittWare offers a complete suite of software development tools to make developing and debugging applications for the T2 family of DSP boards easy and efficient.

### BittWorks Software Tools

#### BittWorks Host Interface and Debugging Tools

BittWare’s BittWorks software tools provide host interface libraries and a wide variety of diagnostic utilities and configuration tools. This tool set is comprised of BittWare’s DSP21k Toolkit, DSP21k Porting Kit, BittWare Target, Remote Toolkit and Target, TS-Lib, and TigerSHARC BSP for Gedae.

#### DSP21k Toolkit

The DSP21k Toolkit is a collection of libraries, applications, and diagnostics that helps users to easily integrate their applications with BittWare hardware. Components of the Toolkit include:

- **Host Interface Library (HIL):** provides a mature and stable API that is compatible with all of BittWare’s boards. It makes communication and control easy between the host and DSP by matching addresses supplied to the HIL to the DSP memory map addresses. It is also easily portable, written entirely in C, the same source code compiles for Windows, Linux and Vx Works.

- **BittWare configuration manager:** provides an easy-to-use interface for finding, tracking and displaying information for all BittWare devices in a system.

- **Diag21k:** an interactive diagnostic utility that provides a powerful scripting language for exercising HIL functions without writing a program using the HIL. It also allows users to load programs and examine DSP memory and provides an assembly level single processor software debugger.

- **BitLoader:** a utility for loading new code into an FPGA or EPROM without any special cables, making hardware updates easier.

- **DspTest/DspBAD:** automated diagnostics for testing board functionality, including PCI interface, DSP, and onboard memory tests.

#### DSP21k Porting Kit

The DSP21k Porting Kit contains the source code for the DSP21k Toolkit to allow designers to port the Toolkit to the operating system of their choice. The Porting Kit provides Project and Makefiles for Windows, VxWorks, and Linux and is written mostly in C for portability.

#### BittWare Target for VisualDSP++

The BittWare Target is a software debug target for Analog Devices’ VisualDSP++ development environment. The BittWare Target has much of the capability of a hardware emulator but provides the extra benefits of a faster code-loading time and easier installation and setup. It allows users to combine any number of processors from multiple DSP boards into a single debugging session. The Target also supports remote debugging sessions for systems that have no direct access to the hardware, using remote access software.

#### Real-Time Operating Systems

BittWare’s T2 family of boards supports the following real-time operating systems (RTOS): Analog Devices’ VisualDSP Kernel (VDX) and Enea’s OSEck RTEOS.

#### Remote Toolkit and Target

The Remote Toolkit contains all of the DSP21k Toolkit programs but allows users to access BittWare hardware on a remote machine as if it were in a local machine. The Remote Target makes all of the features of the BittWare Target for VisualDSP available from a remote machine.

#### BittWare’s TigerSHARC BSP for Gedae

The TigerSHARC Board Support Package (BSP) for Gedae allows system designers to develop their code in Gedae's easy-to-use graphical environment and then port their designs directly to any of BittWare’s ADSP- TS201 or ADSP-TS101 TigerSHARC boards.

#### Code Development Tools, Operating Systems, and Libraries

In addition to its BittWorks software, BittWare also supports a range of host software and third party tools from industry leading companies.

- **Analog Devices’ VisualDSP++:** VisualDSP++ is an integrated development environment for the ADSP-TS201 consisting of a C++ compiler, source level multiprocessor debugger, and project management utilities.

- **SDL’s DSPdeveloper:** DSPdeveloper from SDL works with The MathWorks’ MATLAB®, Simulink®, Stateflow®, and Real-Time Workshop® to allow users to prototype and test DSP applications on their BittWare SHARC DSP boards.
# T2-PMC Technical Specifications

## BOARD ARCHITECTURE

### Processors
- 4 Analog Devices ADSP-TS201S TigerSHARC DSPs
- 600 MHz, 1.67 ns instruction rate DSP core
- 3.6 GFLOPS (32-bit floating point) or 14.4 GOPS (16-bit fixed point) per DSP
- Native support for 32-bit floating point operations or for 1, 8, 16, and 32-bit fixed point operations
- 24 Mbits of on-chip RAM per DSP
- Integrated I/O processor with fourteen-channel DMA controller and four 1 GByte/sec LVDS link ports

### DSP Cluster Shared Memory
- 256 MB SDRAM available to the ADSP-TS201S DSPs
- 8 MB Flash memory for hostless boot

### PMC+ Interface
- Standard PMC interface (J1-J3)
- Additional connector (J4) provides 64 signals to Virtex-II FPGA (can be used as 32 differential pairs)

### Link Ports
- 8 link ports extend from the ADSP-TS201S DSPs (2 links from each) to the Virtex-II FPGA
- 8 link ports (2 per DSP) dedicated for interprocessor communication

### Xilinx Virtex-II Pro (XC2VP30) FPGA
- 3 million system gates
- 8 TigerSHARC link ports 500 MB/sec
- Supports various external DIO, flags, and interrupts
- 8 RocketIO™ high-speed serial transceivers, brought off-board

### External Connectors
- 8 RocketIO connected via 2x Infiniband®-type connectors

### Power
- 20 W typical (500 MHz)
- 30W worst case sustainable (500 MHz)

### Size
- 149mm × 74mm (5.9” × 2.9”)

## SOFTWARE SUPPORT

### Host Interface
- BittWare’s software development kit for Windows® and Linux contains C-callable libraries for board control and communications routines
- Porting kit available for other operating system platforms

### Development Tools
- Analog Devices’ VisualDSP tools: kernel (VDK), C compiler, assembler, linker, simulator, and debugger
- BittWare VisualDSP Target for on-board debugging from host without an ICE
- BittWare’s TS-Lib optimized function libraries for TigerSHARC
- BittWare’s TigerSHARC Board Support Package for Geode
- Analog Devices in-circuit emulators
- Enea’s OSEck RTOS
- SDL’s DSPdeveloper for BittWare: interface to MATLAB, Simulink®, and Real-Time Workshop®

## Ordering Information

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<thead>
<tr>
<th>Code</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2PM-XYY-ZZA-BCDE</td>
<td>X: Processors</td>
<td>4= 4 TS201S DSPs</td>
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<tr>
<td></td>
<td>YY: Processor Speed</td>
<td>50= 500 MHz (default) 60= 600 MHz*</td>
</tr>
<tr>
<td></td>
<td>ZZ: FPGA Size</td>
<td>90= XC2VP20 30= XC2VP30 (default)</td>
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<td>A: FPGA Speed</td>
<td>6= Xilinx speed grade 6 (default) 7= Xilinx speed grade 7</td>
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<tr>
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<td>E: SDRAM</td>
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<td></td>
<td>D: JTAG</td>
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<tr>
<td></td>
<td>C: PMC+ J4 Connector</td>
<td>0= Not populated 1= Populated (default)</td>
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<tr>
<td></td>
<td>B: I/O Configuration</td>
<td>1= Digital I/O connectors populated (front of board)</td>
</tr>
</tbody>
</table>

* Contact BittWare. Special order only.
** Violates PMC height specification