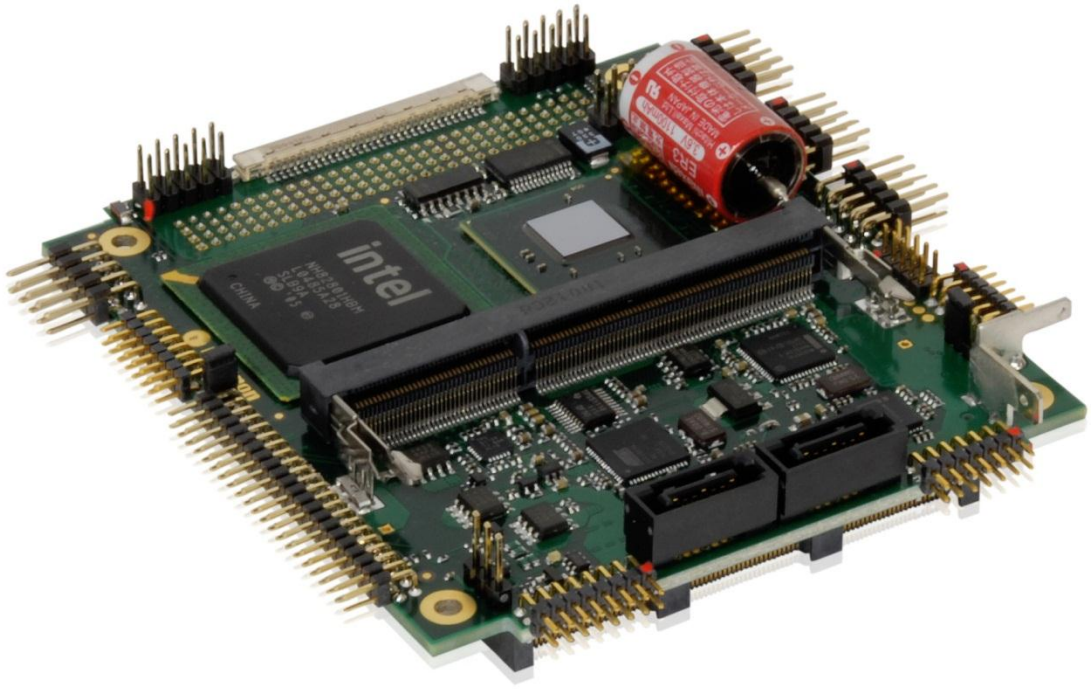
» Kontron User's Guide «



MSM-LP

Document Revision 105

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1 User Information

1.1 About this Document

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1.4 Standards

Kontron Europe GmbH is certified to ISO 9000 standards.

1.5 Warranty

For this Kontron Europe GmbH product warranty for defects in material and workmanship exists as long as the warranty period, beginning with the date of shipment, lasts. During the warranty period, Kontron Europe GmbH will decide on its discretion if defective products are to be repaired or replaced.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

Warranty does not apply for defects arising/resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, as well as the operation outside of the product´s environmental specifications and improper installation and maintenance.

Kontron Europe GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Europe GmbH that are caused by a faulty Kontron Europe GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Europe GmbH and/or its subsidiaries are available for technical support. We are committed to make our product easy to use and will help you use our products in your systems.

Please consult our Website at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications, Board Support Packages, DemoImages, 3D drawings and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Specification

2.1 Available Products

Part No.	Article	Intel® CPU	Remarks
802360	MSM-LP-D425	D425	PC/104 SBC with single-core Intel D425 processor
802350	MSM-LP-D525	D525	PC/104 SBC with dual-core Intel D525 processor
802361	MSM-LP-D425-sys	D425	PC/104 System with single-core Intel D425 processor
802351	MSM-LP-D525-sys	D525	PC/104 System with dual-core Intel D525 processor

2.2 Available Options

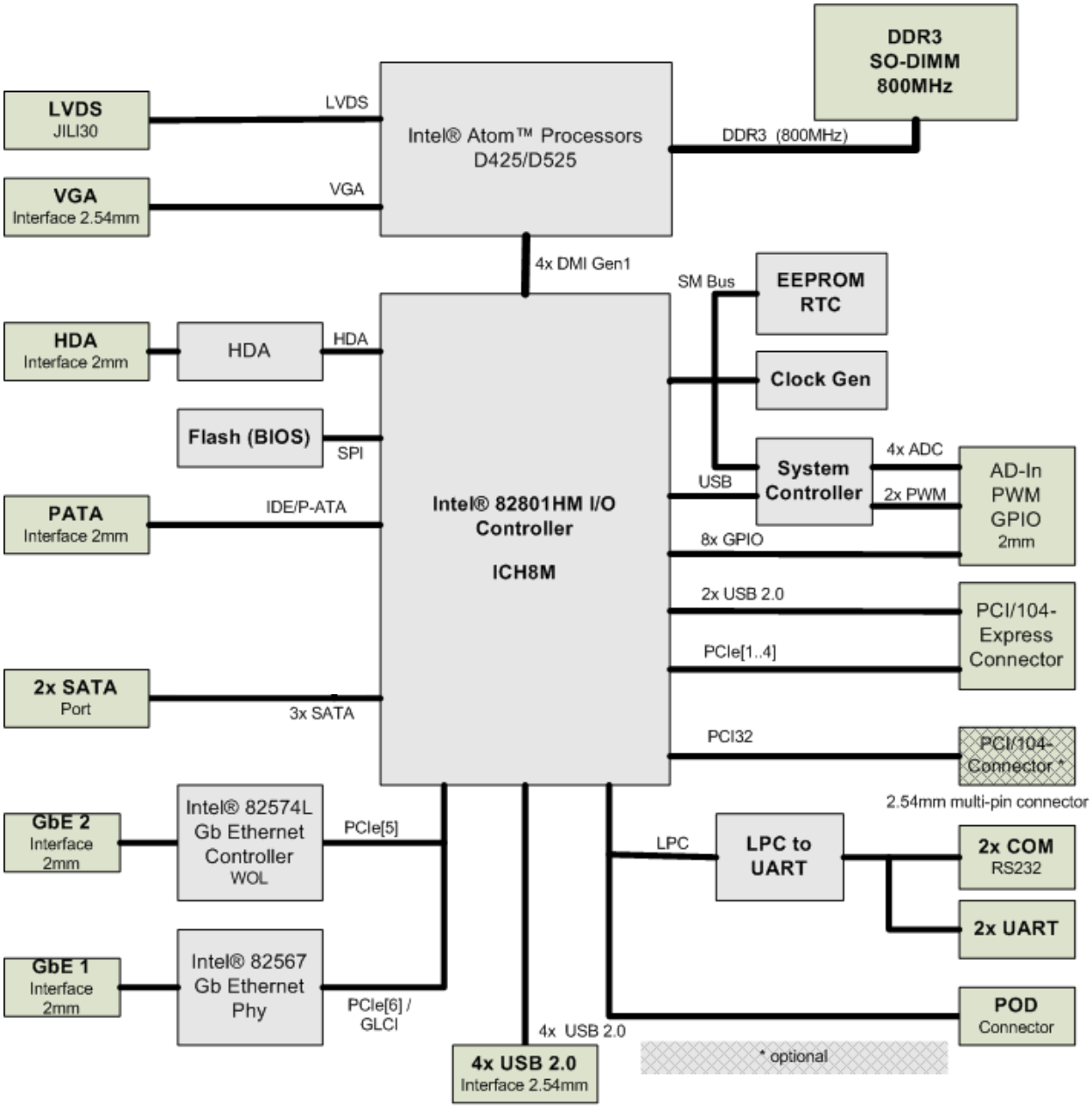
Part No.	Article	Remarks
802365	RAM 1GB DDR3 SODIMM	
802366	RAM 2GB DDR3 SODIMM	
802367	RAM 4GB DDR3 SODIMM	
802313	PCI104 Connector	
802358	MSM-LP Heat Spreader Kit	Heat spreader, screw set included.
802314	MSM-PC104 Passive Cooler Kit	Passive cooler including assembly material.
802316	MSM-PC104 Active Cooler Kit	Heat sink and fan including assembly material.
802040	MSM-PC104 CK	Cablekit including: Interfaces: DVI, Line-In/out or Mic-In, S/PDIF, 1Gb Ethernet Cables: USB, VGA, COM single, SATA, LAN, audio, IDE Warning: Do not use with system boards The pin out is mirrored due to assembling of connectors on the bottom side!

2.3 Evaluation Kit

This kit is used for the evaluation of the MSM-LP product family and is ready-to-use.

Part No.	Article	Remarks
802359	MSM-LP-Evalkit	Ready to Run package including: MSM-LP-D525, MSM-LP Heat Spreader Kit, MSM-PC104 Active Cooler, MSM-PC104 CK, PCI-104 Connector, 2GB SODIMM DDR3, Power supply 250GB 2.5" SATA hard disk with: Dual boot system Win XPe (Evaluation Version), Linux Fedora Board Support Package Test GUI for Win XPe, Linux Documentation

2.4 Block Diagram



2.5 Functional Specification

Processor

- » CPU: Intel® D425 / D525
- » Speed: 1.8GHz

Video

- » Controller: Integrated graphics controller (CPU) multi-display support
- » Memory: Up to 256MB (UMA)
- » Drivers: Intel GMA® driver

Display Interfaces

- » CRT Interface: Up to 2048 x 1536 @ 60Hz
- » LCD Interface: Up to 1366 x 768, 18bpp

Interfaces

- » 2x SATA
- » PATA
- » 2x Gbit LAN
- » 4x USB 2.0
- » 4x COM
- » GPIO/ADC/PWM
- » Audio
- » PCI optional
- » PCIexpress

Power Management

- » S-States: S0, S3, S4, S5, S5eco

2.6 Mechanical Specifications

- » 90.0mm x 102.0mm
- » Height approx. 15.5mm

2.7 Electrical Specifications

2.7.1 Supply Voltage

» 5VDC ± 5%

2.7.2 Supply Current (Windows XP SP3)

The tested boards were mounted on a carrier board; a mouse and a keyboard were connected. The power-consumption tests were executed under Windows XP SP3 by using a tool to stress the CPU (INTEL® Thermal Analysis Tool at 100 % load). The power measurement values were acquired after 15 minutes at full load and a stable CPU die temperature. To ensure a stable die temperature, a corresponding heat sink was used to hold the temperature under the critical trip point.

MSM-LP-D425/D525

Mode	[A] 5V	[W]
Full load	2.8	14

average values

2.8 MSM-LP Environmental Specifications

Temperature

Operating with Kontron Compact Computers AG cooling solution:

» Standard operating temperature: 0 to +70°C

» Extended operating temperature: -40 to +85°C

» Storage temperature: -40 to +85°C

Note: In any case, the maximum operating temperature should never be exceeded!

Humidity

» Operating: 5% to 90% (non-condensing)

2.9 External Real-Time Clock Battery

» Nominal voltage: 3.6V

» Capacity: 1100mAh

Lithium Battery Precautions:

CAUTION! Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.	VORSICHT! Explosionsgefahr bei unsachgemässem Austausch der Batterie. Ersatz nur durch denselben oder einem vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.	PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING! Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3 MSM-LP Connectors & Jumpers

3.1 Top

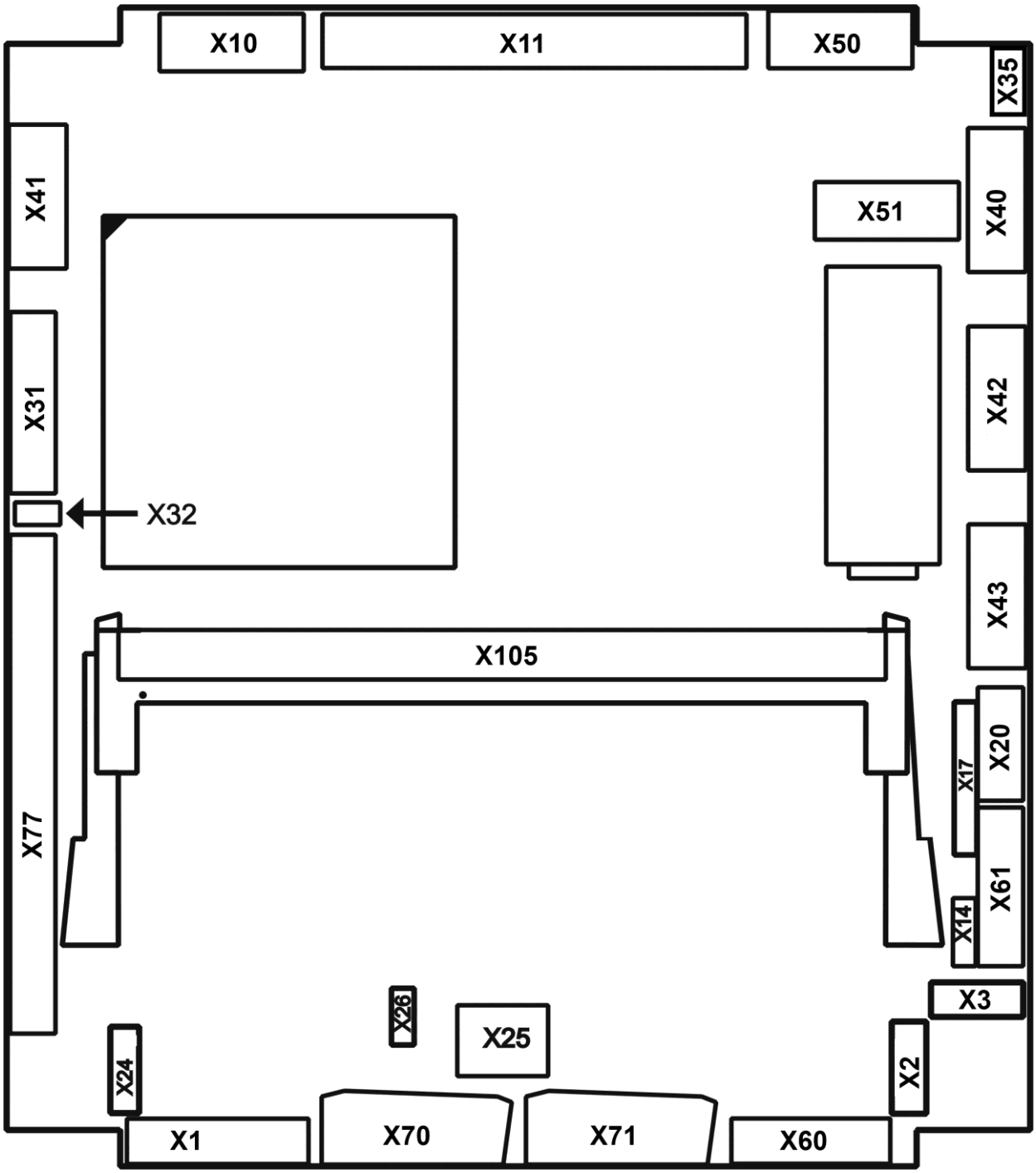
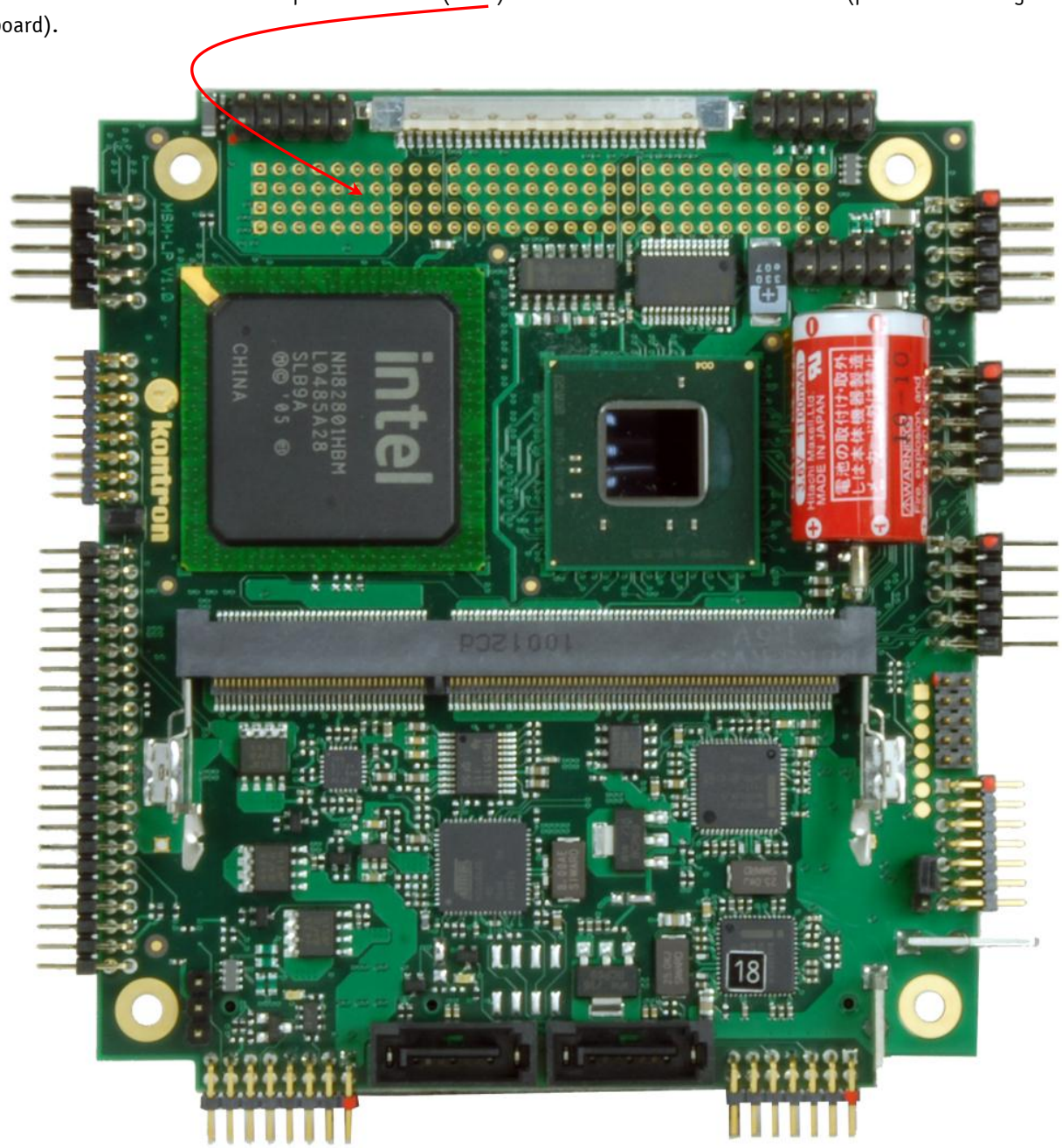


Photo of an MSM-LP board with optional PCI-104 (X101) connector assembled on the bottom (pins visible through the board).

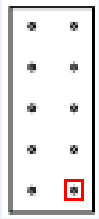


3.2 Connector Descriptions – Top

Warning: On system boards the pin out is mirrored due to assembling of connectors on bottom side! The description is applicable on view from top, if system pin headers are viewed from bottom; even and odd pin numbers must be swapped 1<->2, 3<->4, 5<->6, 7<->8, 9<->10, 11<->12, 13<->14, 15<->16.

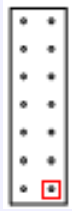
3.2.1 CRT Interface – X50

The board provides an onboard analogue CRT interface.

Header	Pin	Signal Name	Function
2.54mm grid 	1	GND	Ground
	2	RED	Red video signal
	3	NC	Not connected
	4	GREEN	Green video signal
	5	NC	Not connected
	6	BLUE	Blue video signal
	7	CRT_DDATA	DDC data
	8	CRT_HSYNC	Horizontal sync
	9	CRT_VSYNC	Vertical sync
	10	CRT_DCLK	DDC clock

3.2.2 SATA Interface – X70/X71

The board layout supports two SATA 300 interfaces. It is not intended that the standard SATA connectors are assembled from the bottom side. Any connections to a baseboard or to a system I/O must be done with standard cables.

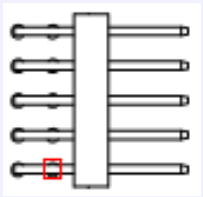
Header	Pin	Signal Name	SATA Connector Pin	Function
1.27mm grid 	1	GND		Ground
	2	GND	1	Ground
	3	SATAx_TXP	2	Data transmit positive
	4	NC		NC
	5	SATAx_TXN	3	Data transmit negative
	6	NC		NC
	7	GND		Ground
	8	GND	4	Ground
	9	SATAx_RXN	5	Data receive negative
	10	NC		NC
	11	SATAx_RXP	6	Data receive positive
	12	NC		NC
	13	GND		Ground
	14	GND	7	Ground
x is the number of the SATA port (SATA1: x -> 1)				

3.2.3 Serial Port Interfaces – X40/X41/X42/X43

Four serial ports for asynchronous serial communication are defined. X40, X41 support RS-232 level and X42, X43 support TTL level. An external conversion to RS-232 and RS-422/485 is possible for all ports.

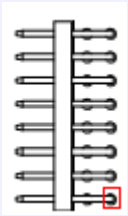
Note:	External converters to RS-232 or RS-422/485 with galvanic separation are available. All four ports can bypass the level-shifters to support TTL levels (OEM high volume placement option).

On system board all four serial ports support TTL level!

Header	Pin	Signal Name	Function	DSUB9
2.54mm grid 	1	DCDXx#	Data carrier detect	1
	2	DSRXx#	Data set ready	6
	3	RXDXx#	Receive data	2
	4	RTSXx#	Request to send	7
	5	TXDXx#	Transmit data	3
	6	CTSXx#	Clear to send	8
	7	DTRXx#	Data terminal ready	4
	8	RIXx#	Ring indicator	9
	9	GND	Ground	5
	10	V5.0_SO	Power +5V	-
x is the number of the COM port (COM1: x -> 1)				

3.2.4 GPIO and AD/DA Interface – X31

The board has a GPIO header interface with additional AD/DA channels. Any filtering must be done externally.

Header	Pin	Signal Name	Function
2.00mm grid 	1	GPIO0	General purpose I/O
	2	GPIO1	General purpose I/O
	3	GPIO2	General purpose I/O
	4	GPIO3	General purpose I/O
	5	GPIO4	General purpose I/O
	6	GPIO5	General purpose I/O
	7	GPIO6	General purpose I/O
	8	GPIO7	General purpose I/O
	9	PWM_OUT0	D/A output
	10	PWM_OUT1	D/A output
	11	ADC_IN0	A/D input (0-10.3V) *)
	12	ADC_IN1	A/D input (0-10.3V) *)
	13	ADC_IN2	A/D input (0-10.3V) *)
	14	ADC_IN3	A/D input (0-10.3V) *)
	15	GND	Ground
	16	+V3.3_S5	Power +3.3V

*) A/D input (0-4.88V) on system board

3.2.5 Power Supply – X1

A power connector for the main power supply is provided. The SBCs function with a single +5V power supply. Additional voltages for PC/104 peripherals (+12V, -5V, -12V) must be generated externally.

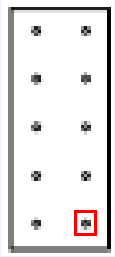
Header	Pin	Signal Name	Function
2.00mm grid	1	+12V_IN	Power +12V
	2*)	PSON#	ATX power on (Power LED)
	3	+5V_IN	Power +5V
	4	+5V_IN	Power +5V
	5	GND	Ground
	6	GND	Ground
	7	GND	Ground
	8	GND	Ground
	9	POWER_BTN#	External main button
	10	RESET_BTN#	External reset button
	11*)	IGNITION#	Ignition input
	12	HDD_ACT#	HDD activity LED
	13	VBAT	RTC battery input
	14	SMB_ALERT#	System management alert
	15	SMB_DAT	System management bus data
	16	SMB_CLK	System management bus clock

*) Warning: On system board the pin out changes!

Pin 2 PSON# is the SLP_S5# 3.3 Volt output and Pin 11 EC_IGNITION# is the SLP_S3# 3.3 Volt output.

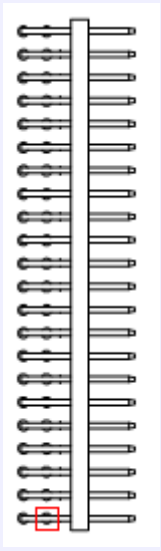
3.2.6 USB Interfaces – X50/X51

The board is populated with four USB interfaces. Two connectors with 2 USB ports each are defined. Further USB ports are accessible over the PCIe/104 extension connector.

Header	Pin	Signal Name	Function
2.54mm grid 	1	USBxVCC	Power +5V
	2	USByVCC	Power +5V
	3	USBxN	USBx data negative
	4	USByN	USBy data negative
	5	USBxP	USBx data positive
	6	USByP	USBy data positive
	7	GND	Ground
	8	GND	Ground
	9	SHD	Shield
	10	SHD	Shield
x (y) is the number of the USB port (USB1: x -> 1)			

3.2.7 IDE Interface (P-ATA) – X77

The design supports one IDE interface that can drive up to two hard disks. When two devices share a single adapter, they must be connected in a master-slave, daisy-chain configuration.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
2.54mm grid 	1	IDE_RST#	Reset	2	GND	Ground
	3	IDE_D7	Data 7	4	IDE_D8	Data
	5	IDE_D6	Data 6	6	IDE_D9	Data
	7	IDE_D5	Data 5	8	IDE_D10	Data
	9	IDE_D4	Data 4	10	IDE_D11	Data
	11	IDE_D3	Data 3	12	IDE_D12	Data
	13	IDE_D2	Data 2	14	IDE_D13	Data
	15	IDE_D1	Data 1	16	IDE_D14	Data
	17	IDE_D0	Data 0	18	IDE_D15	Data
	19	GND	Ground	20	Key (NC)	Key pin
	21	IDE_DRQ	DMA request	22	GND	Ground
	23	IDE_IOW#	I/O write	24	GND	Ground
	25	IDE_IOR#	I/O read	26	GND	Ground
	27	IDE_IOCHRDY	I/O channel ready	28	IDE_CSEL	Cable select
	29	IDE_DACK#	DMA acknowledge	30	GND	Ground
	31	IDE_IRQ	Interrupt request	32	NC	Not connected
	33	IDE_SA1	Address 1	34	IDE_ATAD	UDMA detection
	35	IDE_SA0	Address 0	36	IDE_SA2	Address 2
	37	IDE_CS1#	Chip select 1	38	IDE_CS3#	Chip select 3
	39	NC	Not connected	40	GND	Ground
	41	VCC	Power +5V	42	VCC	Power +5V
	43	GND	Ground	44	NC	Not connected

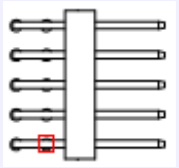
X77 not equipped on system board.

3.2.8 Fan Connector – X24

Header	Pin	Signal Name	Function
2.00mm	1	Speed frequency signal	
	2	+5V	Power +5V
	3	GND	Ground

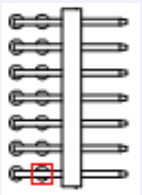
3.2.9 Audio Interface – X20

The audio interface provides stereo analogue and digital audio signals.

Header	Pin	Signal Name	Function
2.00mm grid 	1	LINE_R	Line right
	2	GND_A	Analogue ground
	3	LINE_L	Line left
	4	MIC_R	Mic right
	5	GND_A	Analogue ground
	6	MIC_L	Mic left
	7	V5	Power +5V
	8	SPDIF_IN	Digital audio input
	9	GND	Ground
	10	SPDIF_OUT	Digital audio output

3.2.10 LAN Interface – X60/X61

Two Gbit Ethernet ports are defined. Suitable transformers must be provided externally.

Header	Pin	Signal Name	Function
2.00mm grid 	1	GbEx_MDI0N	Bidirectional pair 0 negative
	2	GbEx_MDI0P	Bidirectional pair 0 positive
	3	GbEx_MDI1N	Bidirectional pair 1 negative
	4	GbEx_MDI1P	Bidirectional pair 1 positive
	5	GbEx_LED0	LED Link
	6	V1.8	Center voltage
	7	GND	Ground
	8	V3.3	Power +3.3V
	9	GbEx_LED1	LED activity
	10	GbEx_LED2	LED link 100
	11	GbEx_MDI2N	Bidirectional pair 2 negative
	12	GbEx_MDI2P	Bidirectional pair 2 positive
	13	GbEx_MDI3N	Bidirectional pair 3 negative
	14	GbEx_MDI3P	Bidirectional pair 3 positive
x is the number of the GbE port (GbE1: x -> 1)			

3.2.11 AMP Power Input – X2/X3

The AMP power inputs are always connected on the top side of the board.

Header	Nr.	Signal Name	Function
AMP 2.8mm	X3	V5.0_IN	5 Volt power IN

Header	Nr.	Signal Name	Function
AMP 4.75mm	X2	GND	Ground

X2 and X3 not equipped on system board.

3.2.12 LVDS Interface

The LVDS implementation complies with the JILI specification of Kontron (JILI30). When using an LCD, additional voltages may be required to drive the display logic and supply the backlight converter therefore an additional connector for supply voltages is provided.

The FPC connector is only mounted on the top side. The corresponding backlight connector is assembled on the opposite side.

FPC Connector – X11

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	FPC_AN	First channel data out A	16	NC	Not connected
	2	FPC_AP	First channel data out A	17	GND	Ground
	3	FPC_BN	First channel data out B	18	NC	Not connected
	4	FPC_BP	First channel data out B	19	NC	Not connected
	5	FPC_CN	First channel data out C	20	NC	Not connected
	6	FPC_CP	First channel data out C	21	NC	Not connected
	7	GND	Ground	22	NC	Not connected
	8	FPC_CLKN	First channel clock	23	NC	Not connected
	9	FPC_CLKP	First channel clock	24	GND	Ground
	10	FPC_DN	First channel data out D	25	SDA	I2C data line
	11	FPC_DP	First channel data out D	26	DATAENA	Panel power output
	12	NC	Not connected	27	SCL	I2C clock line
	13	NC	Not connected	28	VCC	+3.3V power *)
	14	GND	Ground	29	VCC	+3.3V power *)
	15	NC	Not connected	30	VCC	+3.3V power *)

*) Panel power can be set to +5V by assembly option.

3.3 Bottom

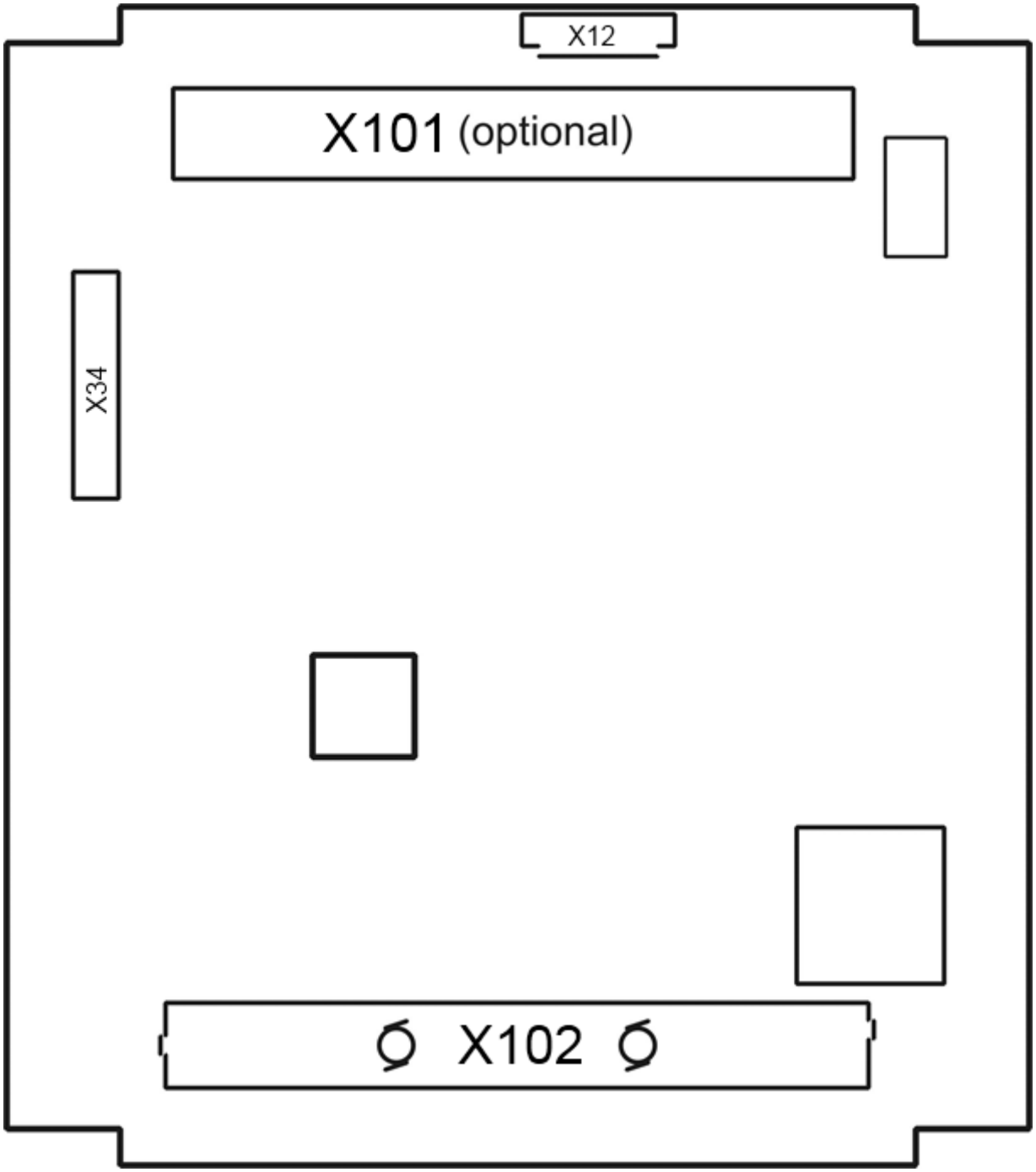
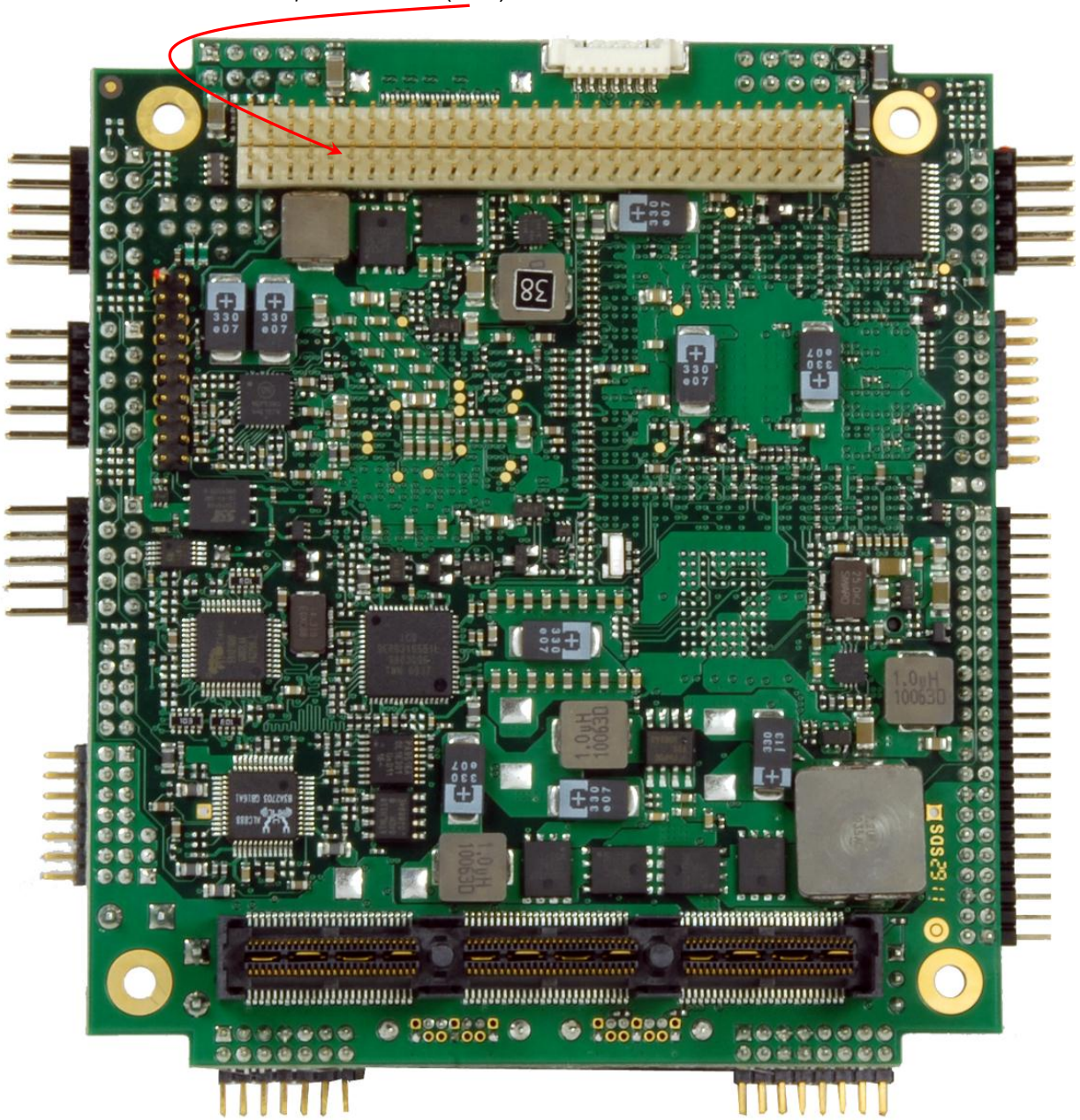


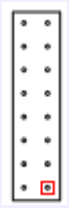
Photo of an MSM-LP board with optional PCI-104 (X101) connector assembled.



3.4 Connector Descriptions – Bottom

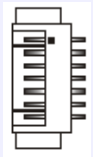
3.4.1 LPC/POD Interface – X34

This is a connector for additional LPC devices such as POD, SuperIO or TPM. It can also be used for a second BIOS flash interface (SPI or LPC)

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
2.00mm grid 	1	V3.3_S0	Power	2	LPC_LDA0	Data
	3	LFRAME#	LPC frame	4	LPC_LDA1	Data
	5	PLT_RST#	Reset OUT	6	LPC_LDA2	Data
	7	V3.3_S0	Power	8	LPC_LDA3	Data
	9	V5.0_S0	Power	10	PLT_RST#	Reset OUT
	11	CLK	Clock	12	BIOS_EN	BIOS selection
	13	GND	Ground	14	RESET_IN#	Reset IN
	15	V3.3_SPI_PROG	Power IN	16	SERIRQ	
	17	SPI_CS#		18	SPI_CLK	
	19	SPI_MISO		20	SPI_MOSI	

3.4.2 Backlight Connector – X12

The backlight connector is always mounted on the bottom side, opposite of the LVDS FPC Connector .

Header	Pin	Signal Name	Function
	1	NC	Not connected
	2	BKLTADJ	Brightness control (PWM 3.3 V)
	3	GND	Ground
	4	NC	Backlight power +5V *)
	5	NC	Backlight power +5V *)
	6	GND	Ground
	7	BKLTON	Backlight on/off

*) Backlight power can be set to +12V by assembly option (needs +12V on pin 1 of supply connector X1).

3.5 Other Connectors

Connector	Structure	Pins	Remarks
X101	PCI-104	4x30	Bottom, 2mm (optional)
X17	JTAG G-LAN1	1x7	Top, 2mm
X105	SODIMM DDR3	204	Top, 0.6mm
X25	AVR programming	2x4	Top, 2mm
X102	PC104e	156	Bottom, 0.635mm

3.6 Jumpers

3.6.1 THT Jumpers – Top

Settings written in bold are defaults!

Assembly Defaults			Description		
Reference	Sort	Position	Signal Name	Open / Position 1-2	Closed / Position 2-3
X14 *)	3-way 2.0 mm	2-3	V3.3_82574	WOL *)	**No WOL**
X32	2-way 2.0 mm	Closed	Auto-start	No auto-start	**Auto-start**
X35	2-way 2.0 mm	open	BIOS_Default	**Normal BIOS startup**	Recovery BIOS settings

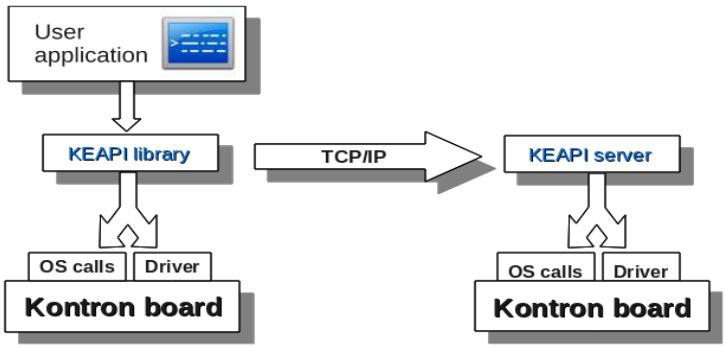
*) On system board WOL is always active, X14 is not equipped.

4 Special Features

4.1 KeAPI

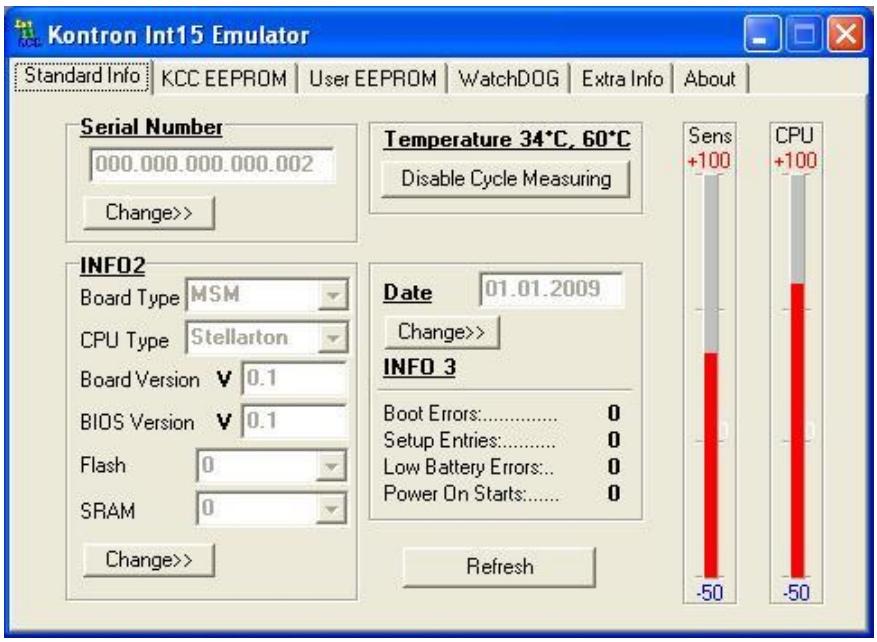
The Kontron embedded API (KeAPI) is an extension of the PICMG EAPI mainly with additional remote functionality. It consists of hardware drivers providing access to features like Watchdog, I2C Bus or GPIO and a QT based user interface KEAPI GUI. KeAPI is part of standard BSPs.

Please refer to EMD Customer Section for detailed documentation and downloads.



4.2 INT15 Support

The INT15 SFR (Special Function Register) functions support access to an I2C EEPROM. Addresses 0h-3FFh are reserved for manufacturer information and counters; addresses 400h-7FFh are for customer purposes. INT15 SFR is supported under DOS and Windows (over 32/64 bits driver).



Driver Installer
kontron
OS Detected:
Windows-XP 32-bits
KCC INT15 functions emulator v3.9(PIIX4,ICH4,5,6,7,9,SCH,LX800,MSMST) Driver
This software will help you to install a proper driver
This may take up to 5 minutes.
It will try to install driver automatically, otherwice, please follow
the instuction of the operating system .
Supported OS's: Windows XP, Windows Vista, Windows-7,
Windows XP x64, Windows Vista x64, Windows-7 x64.
1. Please, close all documents and unnecessary applications.
2. Connect your interface and click "Next" button.
Or press "Skip" to skip driver installation.
Next >>
Cancel

4.3 System Controller USB Serial Commands

Note: "System Controller USB" function must be enabled in the BIOS setup for using the ADC and PWM functions.

MSM-LP on-board 4-channel ADC and 2-channel PWM are accessible over a USB-serial port interface.

- In the Windows Device Manager it is represented as "KCC ADC/PWM Control Serial Interface". For a driver installation under Windows, the "KCCUSBserial.inf" file is required.
- For Linux this interface does not require any drivers and is listed in the system as the "ttyACM0" serial port.
- Communication with ADC/PWM can be organized over the standard serial asynchronous protocol.
- Every control request consists of a 4 Byte package, with the leading (synch) Byte always 0x15.
- The number of Bytes in the answer is variable and depends on the request.

4.3.1 I/O Control Requests/Answers:

4 Byte Command	Parameters	Description
'\x15','a','c',N {0x15,0x61,0x63,N}	N-channels mask N=0 – stop measurement N=0x01…0x0F define which channels 0…3 will be measured	Start cyclic ADC measurement when ADC measures all channels defined in the mask field, the controller sends an answer: '\x15','D',VS…VE {0x15,0x44,VS…VE} , where VS is the Byte value of the first defined channel and VE is the Byte value of the last defined channel. The measurement/answer will repeat until the controller receives a stop command ('\x15','a','c',0). The number of received Bytes defined by the channels mask. Example: mask N=0x05, ADC will measure on Channels 0 and 2 and send a 4 Byte answer '\x15','D',V0,V2, where V0 and V2 are results of the measurement on the appropriate channels.
'\x15','a','s',N {0x15,0x61,0x73,N}	N-channels mask N=0 – stop measurement N=0x01…0x0F define which channels 0…3 will be measured	Start single shot ADC measurement when ADC measures all channels defined in the mask field, the controller sends an answer: '\x15','D',NS…NE {0x15,0x44,VS…VE} where VS is the Byte value of the first defined channel and VE is the Byte value of the last defined channel. A non-cycled variant of the command above. The number of received Bytes defined by the channels mask.
'\x15','p','a','e' {0x15,0x70,0x61,0x65}		Enable PWM Channel A.
'\x15','p','a','d' {0x15,0x70,0x61,0x64}		Disable PWM Channel A.
'\x15','p','b','e' {0x15,0x70,0x62,0x65}		Enable PWM Channel B.
'\x15','p','b','d' {0x15,0x70,0x62,0x64}		Disable PWM Channel B.
'\x15','w','a',N {0x15,0x77,0x61,N}	N – PWM value	Set PWM value on Channel A (PWM must be enabled).
'\x15','w','b',N {0x15,0x77,0x62,N}	N – PWM value	Set PWM value on Channel B (PWM must be enabled).
'\x15','f','v','r' {0x15,0x66,0x76,0x72}		Get firmware version. Answer: '\x15','V','M','S','M','L','P','_','0','6',0 The answer is always 11 Bytes, '\x15','V' - answer prefix, 8 Bytes of the firmware version and a final Byte 0.

4.4 Digital I/O Ports/Operations

The MSM-LP board has 8 digital inputs/outputs accessible over system port I/O operations.

The base address for I/O operations can be obtained as a WORD value from the PCI config space.

Bus:0, Dev:0x1F, Fun:0, Offset :0x48. Default base address is 0x0480.

4.4.1 I/O Control Access

Access to digital inputs/outputs, i.e. settings of I/O direction and logical level control can be provided over Kontron embedded API functions.

4.5 Watchdog Function

The MSM-LP provides a watchdog function which resets the system when a specific amount of time has elapsed without watchdog reset activity. The watchdog is highly configurable and the timeout time can be set between two seconds and 65,535 seconds. The watchdog output is connected to the system controller.

4.5.1 BIOS Setup

With this setting, the watchdog timer of the MSM-LP can be enabled and the time until a reset is asserted can be selected. The watchdog timer is part of F81216 chip and can be reset by directly accessing the F81216.

See Section **Fehler! Verweisquelle konnte nicht gefunden werden.** on how to access the F81216 watchdog.

Set Watchdog timeout:

- Disabled: The watchdog timer is disabled
- 1 / 5 / 15min: The watchdog timer resets the board after this amount of time.
- **Default value:** Disabled.

Warning: If this setting is enabled without a working watchdog reset in your program, your computer will reset after the time set in the BIOS setup.

4.5.2 Watchdog Hardware Access

The watchdog registers of the F81216 chip are accessible over I/O mapped registers with indexed access. The following table shows the addresses used. The F81216 chip has few devices and the watchdog is device number 8.

Address	Name	Type	Description
0x4E	IND	RW	Indexed register access number
0x4F	DAT	RW	Indexed register content

Indexed Register Map of Watchdog Device 08h

Index	Bit	Name	Access	Function
0x30	0	WDT_EN	RW	Watchdog device enable register: 0=disable,1=enable
0x30	1-7		RsvdP	Reserved
0xF0	0	WDT_EVENT	RO	0: no time out has occurred 1: time out has occurred Writing "1" to this bit will clear the status
0xF0	1-2	WDT_UNIT	RW	00: Timer Unit is 10ms 01: Timer Unit is 1 second 10: Timer Unit is 1 minute 11: reserved
0xF0	3-7		RsvdP	Reserved
0xF1	7-0	WDT_CNT	RW	The number of time units for the watchdog timer. Write the same non-zero value twice to enable the timer; otherwise the timer is disabled.

Register Attributes

Attribute	Description
RsvdP	RESERVED AND PRESERVED Reserved for future RW implementations. Registers are Read-only and the software must preserve the value for writes to this bit.
RW	READ-WRITE REGISTER Register bits are Read-Write and can be set or cleared by software.
RO	READ-ONLY Register bits are Read-only and can not be altered by software.
WO	WRITE-ONLY Register bits can only be Written. Reading returns indeterminable data.

Example: Enable/Retrigger Watchdog

```
; Watchdog device activation
mov dx, 4Eh             ; Store port in dx for in/out instruction
mov al, 77h             ; Configuration mode value
out dx, al              ; Output 2 times to enter config mode
out dx, al              ;
mov al, 07h             ; Device number register
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register = 0x4F
mov al, 08h             ; Device number 8 - watchdog
out dx, al              ; Set DAT register
dec dx                  ; Decrement dx to IND register
mov al, 30h             ; Activation register address = 0x30
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register
mov al, 01h             ; Activation value WDT_EN = 1
out dx, al              ; Set DAT register – enable watchdog device
dec dx                  ; Decrement dx to IND register to 0x4E address
mov al, 0F0h            ; WDT_UNIT register
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register to 0x4F address
mov al, 02h             ; Set Timer Unit is 1 second, WD_UNIT = 01
out dx, al              ; Set DAT register
dec dx                  ; Decrement dx to IND register to 0x4E address
mov al, 0F1h            ; WDT_CNT register
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register 0x4F address
mov al, 10              ; Set Timer to 10 second interval
out dx, al              ; Set DAT register 2 times
out dx, al              ;
dec dx                  ; Decrement dx to IND register to 0x4E address
mov al, 0AAh            ; Leave configuration mode
out dx, al              ; Move value to IND register
```

In C language:

```
outportb(0x4E,0x77);    //output 2 times to enter configuration mode
outportb(0x4E,0x77);
outportb(0x4E,0x7);     //device index
outportb(0x4F,0x8);     //device number 8
outportb(0x4E,0x30);    //activation register
outportb(0x4F,0x01);    //activate watchdog WDT_EN = 1
outportb(0x4E,0xF0);    //WDT_UNIT register
outportb(0x4F,0x02);    //set timer unit is 1 second, WD_UNIT = 01
outportb(0x4E,0xF1);    //WDT_CNT register
outportb(0x4F,10);      // Set Timer to 10 second interval, 2 times
outportb(0x4F,10);      //
outportb(0x4E,0xAA);    //Leave configuration mode
```

Example: Disable Watchdog

```
; Watchdog device activation
mov dx, 4Eh             ; Store port in dx for in/out instruction
mov al, 77h             ; Configuration mode value
out dx, al              ; Output 2 times to enter config mode
out dx, al              ;
mov al, 07h             ; Device number register
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register = 0x4F
mov al, 08h             ; Device number 8 - watchdog
out dx, al              ; Set DAT register
dec dx                  ; Decrement dx to IND register
mov al, 0F1h            ; WDT_CNT register
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register 0x4F address
mov al, 0               ; Set Timer to 10 second interval
out dx, al              ; Set DAT register 2 times to disable watchdog
out dx, al              ;
dec dx                  ; Decrement dx to IND register
mov al, 30h             ; Activation register address = 0x30
out dx, al              ; Move value to IND register
inc dx                  ; Increment dx to DAT register
mov al, 0h              ; Deactivation value WDT_EN = 0
out dx, al              ; Set DAT register – enable watchdog device
dec dx                  ; Decrement dx to IND register to 0x4E address
mov al, 0AAh            ; Leave configuration mode
out dx, al              ; Move value to IND register
```

In C language:

```
outportb(0x4E,0x77);    //output 2 times to enter configuration mode
outportb(0x4E,0x77);
outportb(0x4E,0x7);     //device index
outportb(0x4F,0x8);     //device number 8
outportb(0x4E,0xF1);    //WDT_CNT register
outportb(0x4F,0);       // Set Timer to 0, 2 times
outportb(0x4F,0);       //
outportb(0x4E,0x30);    //activation register
outportb(0x4F,0x00);    //deactivate watchdog WDT_EN = 0
outportb(0x4E,0xAA);    //Leave configuration mode
```

5 Design Considerations

5.1 Board Drill-Hole Dimensions

The MSM-LP board follows the PCIe/104™ specification. For more information see the PCI/104-Express™ & PCIe/104™ specifications.

5.2 Thermal Management

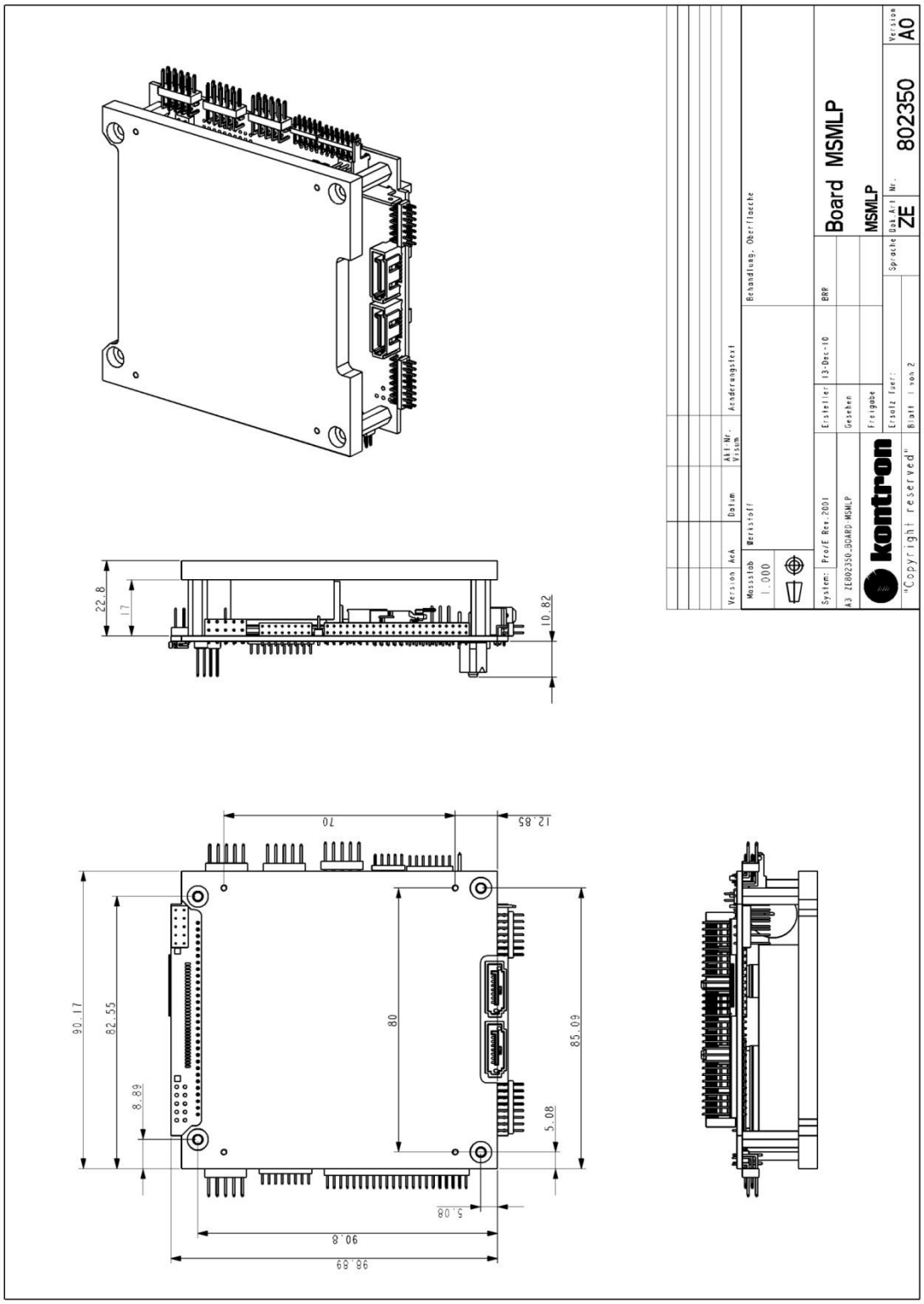
The heat spreader plate assembly is delivered by Kontron Compact Computers AG for the MSM-LP. The heat spreader plate on top of this assembly is ***not*** a heat sink. It works as a standard thermal interface to be used with a heat sink or other cooling device.

External cooling must be provided to maintain the heat spreader plate at proper operating temperatures. Under worst case conditions, the cooling mechanism must maintain an ambient air and heat spreader plate temperature of 85°C or less.

The aluminum blocks and thermal pads on the underside of the heat spreader assembly serve to provide thermal interfaces between the heat spreader plate and the major heat-generating components on the MSM-LP.

5.3 Heat Spreader Dimensions

Figures: heat spreader plate showing the pads for the heat-generating components of the MSM-LP boards.



6 BIOS Operation

The module is equipped with the AMI Aptio® BIOS located in an onboard SPI serial flash memory. The BIOS can be updated using a flash utility.

6.1 Determining the BIOS Version

The AMI Aptio® BIOS version can be determined on the BIOS setup screen.

6.2 Setup Guide

System behavior can be modified by changing the BIOS configuration.

Note:	Selecting incorrect values may cause system boot failure. To recover, press <**F3**> to load setup default values.

6.2.1 Start the AMI Aptio® BIOS Setup Utility

To start the AMI Aptio® BIOS setup utility, press <**DEL**> during boot-up.
Press <DEL> to enter setup.
The Main Menu then appears.
The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Bottom right	Lists Setup navigation keys.
Item-Specific Help Window	Top right	Help for the selected item.
Menu Window	Center left	Selection fields for the current menu.

Temporary Boot Menu

By pressing the <**F7**> key at the beginning of the startup process the temporary boot menu will appear.

Menu Bar

The menu bar at the top of the window lists the different menus. Use the left/right arrow keys to make a selection.

Legend for Menu Bar

Key	Function
→ or ← Arrow key	Select Screen
↑ or ↓ Arrow key	Select Item
Enter	Select
+/-	Change Option
<F1>	General Help
<F2>	Previous Values
<F3>	Optimized Defaults
<F4>	Save and Exit
<F7>	Temporary Boot Menu
<ESC>	Exit

Selecting an Item

Use the ↑ or ↓ key to move. Use the + and – keys to select a value.

Displaying Submenus

Use the ↑ or ↓ key to move the cursor to the submenu then press <**Enter**>. The pointer (▸) marks all the submenus.

Item-Specific Help Window

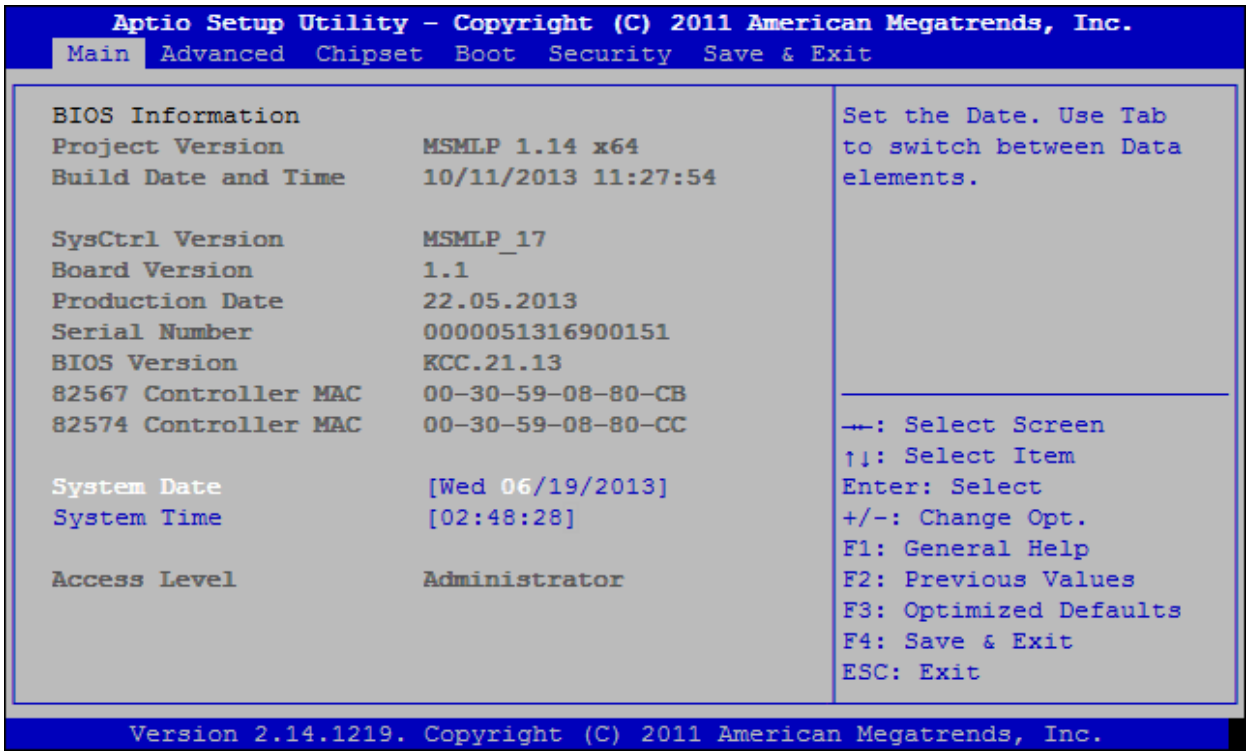
The Help window on the right side of each menu displays the Help text for the selected item.

General Help Window

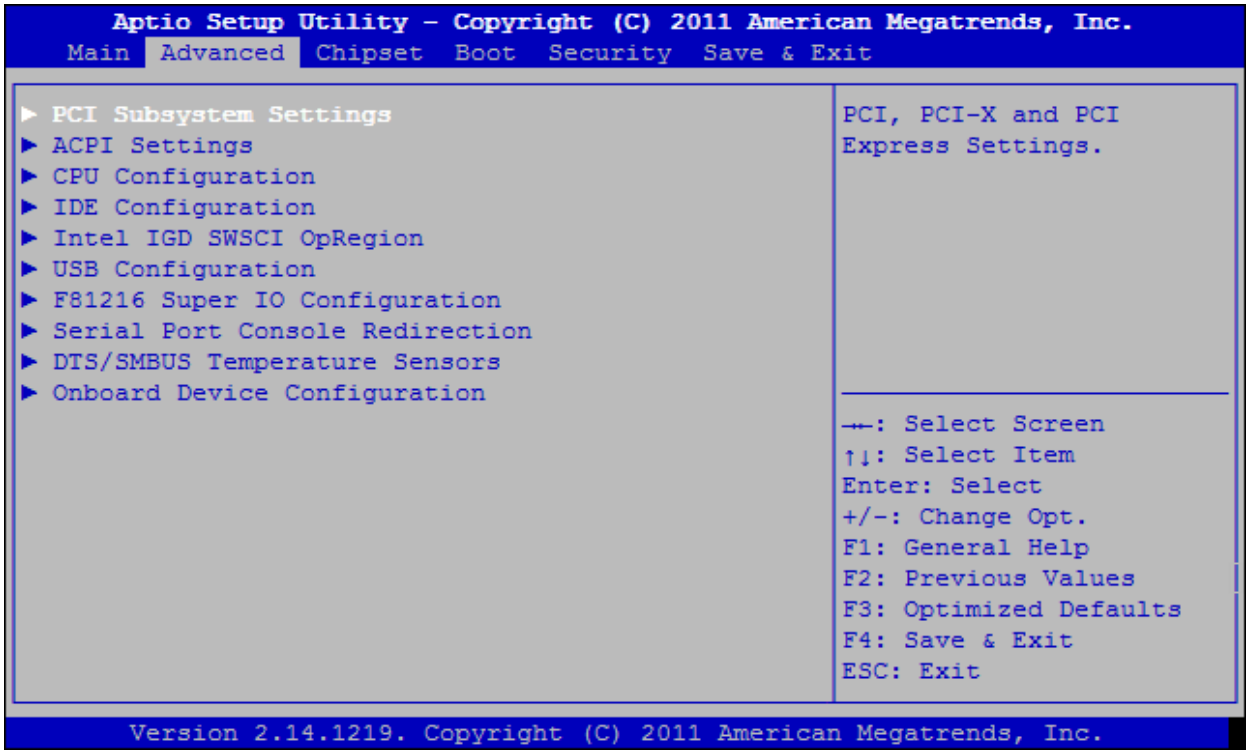
Pressing <**F1**> on a menu brings up the general Help. Press <**Esc**> to exit.

6.3 BIOS Setup

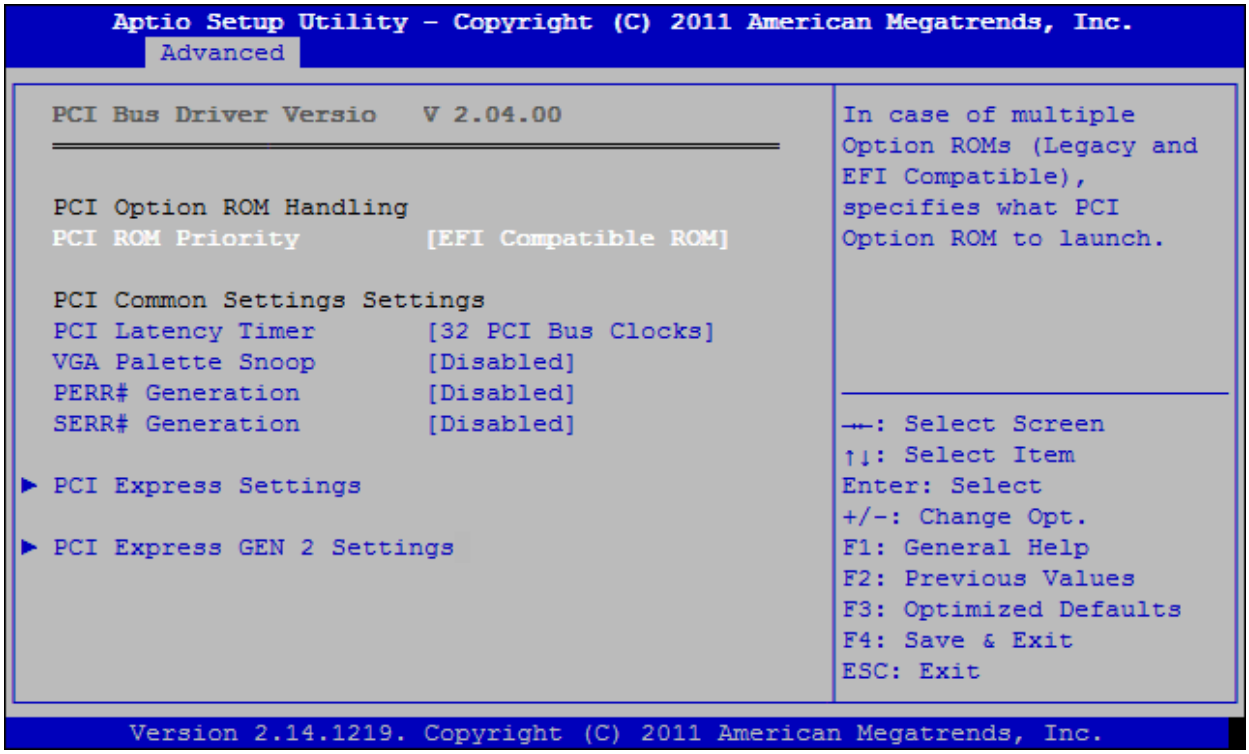
6.3.1 Main Menu



6.3.2 Advanced Menu

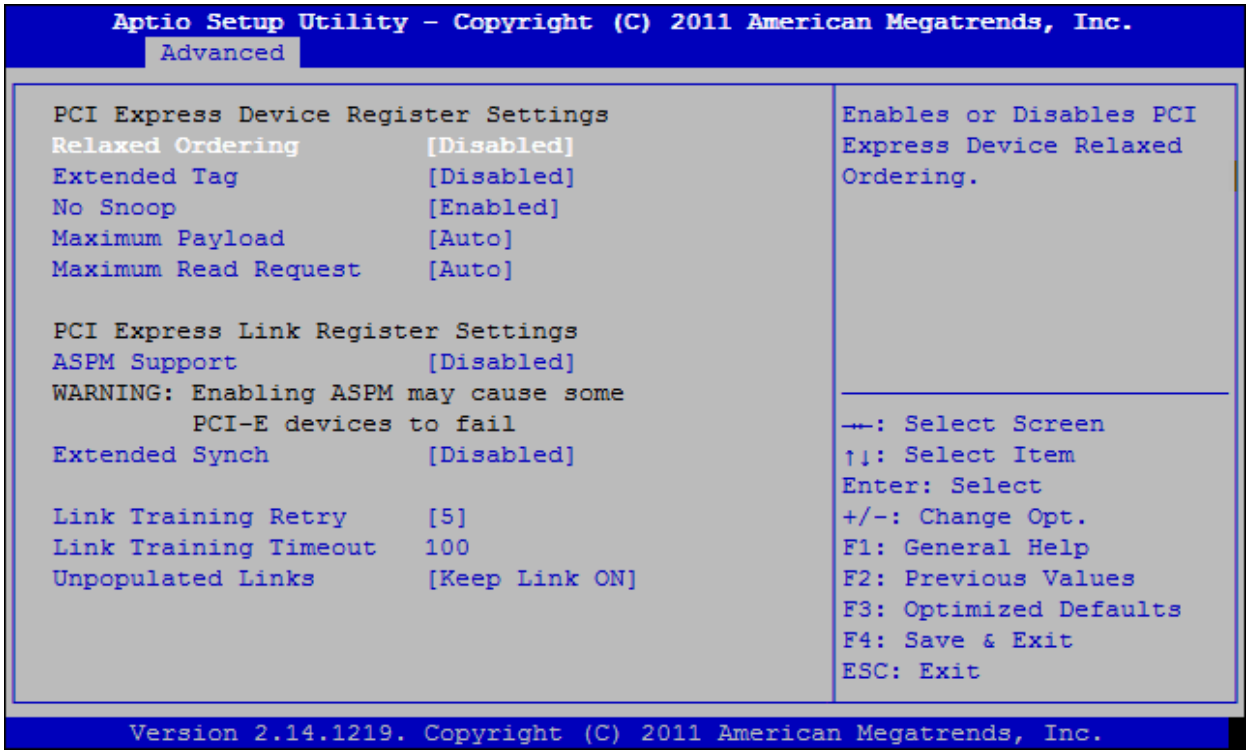


PCI Subsystem Settings Menu



Feature	Options	Description
PCI ROM Priority	Legacy ROM **EFI Compativle ROM**	In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.
PCI Latency Timer	**32 PCI Bus Clocks** 64 PCI Bus Clocks 96 PCI Bus Clocks ... 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA Palette Register Snooping.
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate PERR#.
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate SERR#.

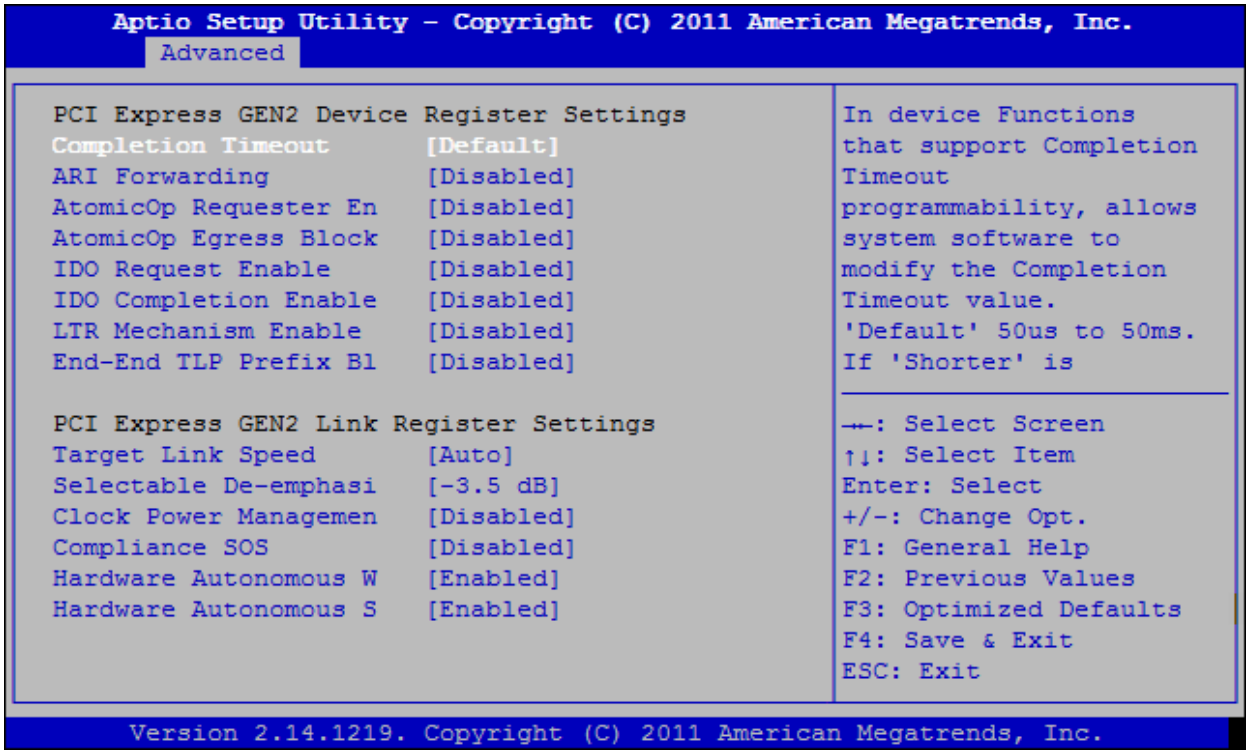
PCI Express Settings



Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express Device Relaxed Ordering.
Extended Tag	**Disabled** Enabled	If Enabled allows Device to use 8-bit Tag field as a requester.
No Snoop	Disabled **Enabled**	Enables or Disables PCI Express Device No Snoop Option.
Maximum Payload	**Auto** 128 Bytes ... 4096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes ... 4096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.
ASPM Support	**Disabled** Auto Force LOs	Force LOs: Force all Links to LOs State Auto: BIOS Auto function Disabled: Disable ASPM
Extended Synch	**Disabled** Enabled	If Enabled allows generation of Extended Synchronization patterns.
Link Training Retry	Disabled 2 3	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

	5	
Link Training Timout	[1...**100**]	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register.
Unpopulated Links	**Keep Link ON** Disable Link	In order so save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

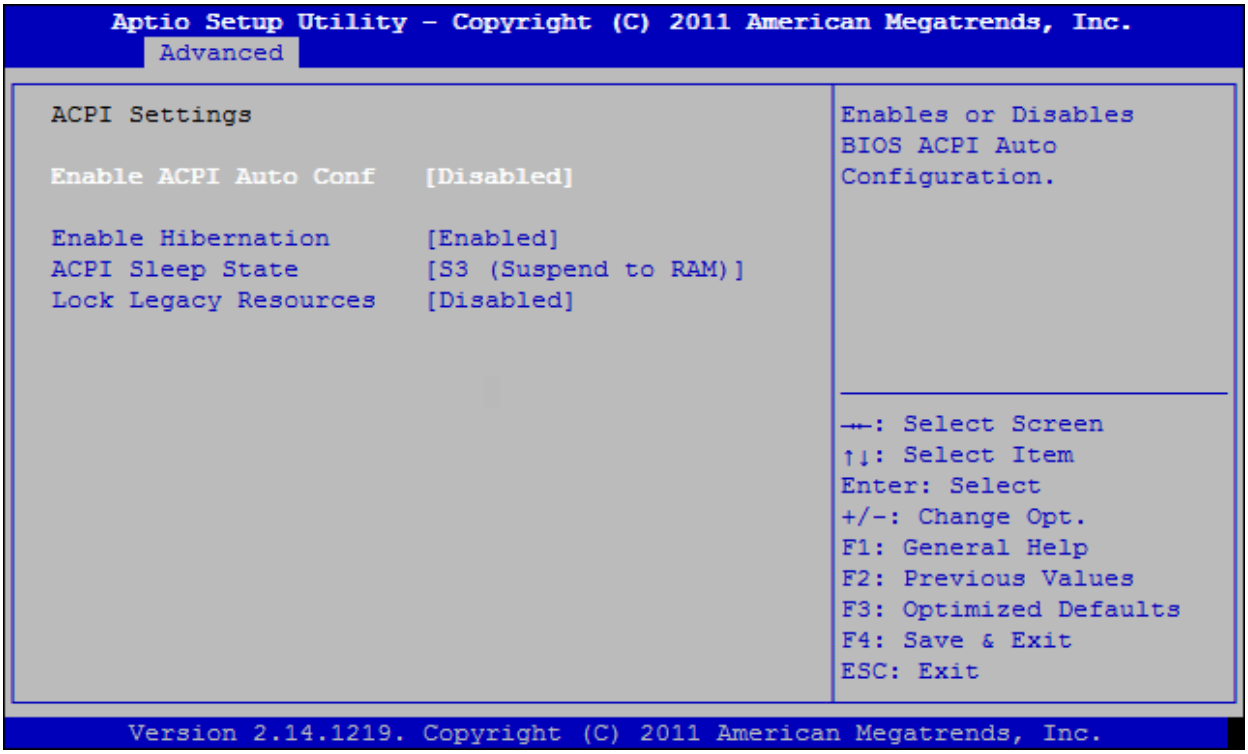
PCI Express Gen2 Settings



Feature	Options	Description
Completion Timeout	**Default** Shorter Longer Disabled	In device Functions that support Completion Timeout programmablitity, allows system software to modify the Completion Timeout value.
ARI Forwarding	**Disabled** Enabled	Enables or Disables ARI Forwarding.
AtomicOp Requester En	**Disabled** Enabled	Enables or Disables AtomicOP Requests.
AtomicOp Egress Block	**Disabled** Enabled	Enables or Disables AtomicOP Requests via Egress Block.
IDO Reuqest Enable	**Disabled** Enabled	If set to 'Enabled', this permits setting the number of ID_Based Ordering (IDO) bit requests to be initiated.
IDO Completion Enable	**Disabled** Enabled	If set to 'Enabled', this permits setting the number of ID_Based Ordering (IDO) bit requests to be initiated.
LTR Mechanism Enable	**Disabled** Enabled	If set to 'Enabled', this enables the Latency Tolernace Reporting Mechanism.
End-End TLP Prefix B1	**Disabled** Enabled	If set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP prefixes.
Target Link Speed	**Auto** Force to 2.5 GT/s	'Force to 2.5 GT/s' limits the maximum speed to GEN1 speed.
Selectable De-emphasis	**-3.5 dB**	If supported by hardware, this will control transmission de-

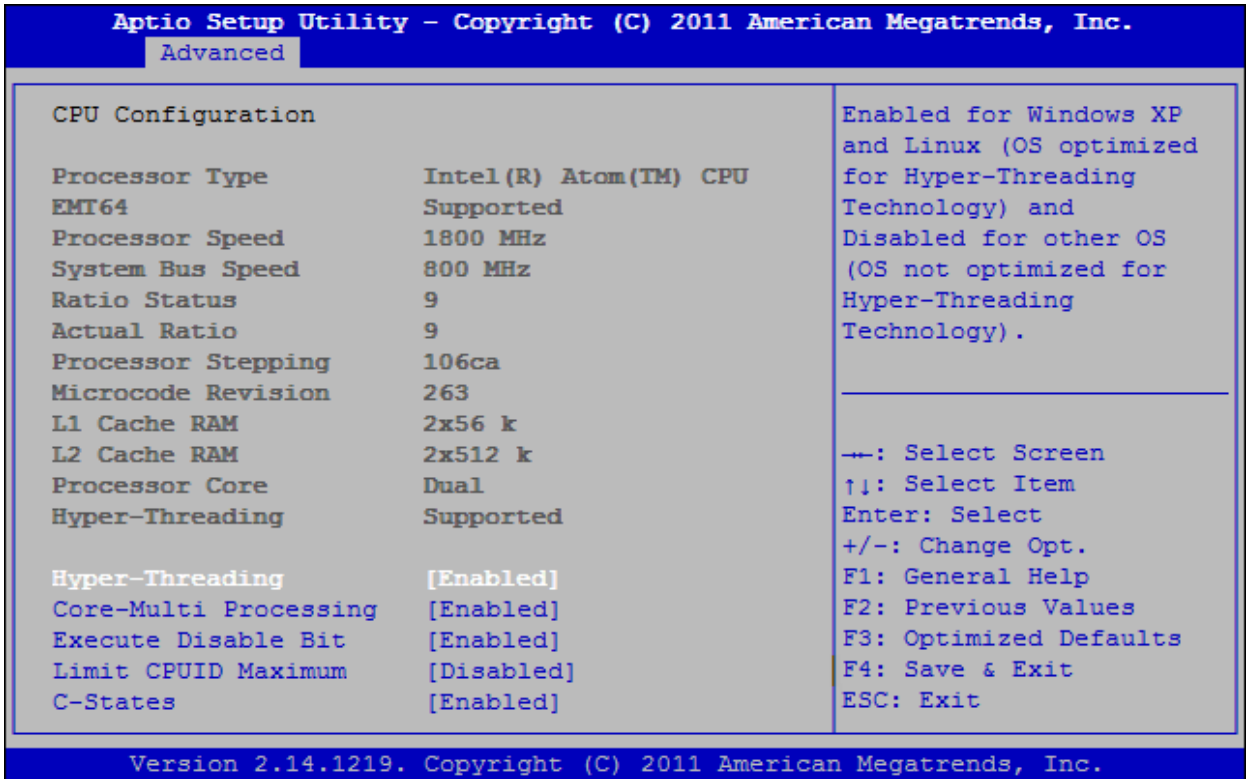
	-6.0 db	emphasis of target link when operating at 5.0 GT/s.
Clock Power Management	**Disabled** Enabled	If set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of Link clock.
Compliance SOS	**Disabled** Enabled	If set to 'Enabled', this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern.
Hardware Autonomous W	Disabled **Enabled**	If set to 'Enabled', this will disable the hardware's ability to change link width except width size reduction for the purpose of correcting unstable link operation.
Hardware Autonomous S	Disabled **Enabled**	If set to 'Enabled', this will disable the hardware's ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation.

ACPI Settings



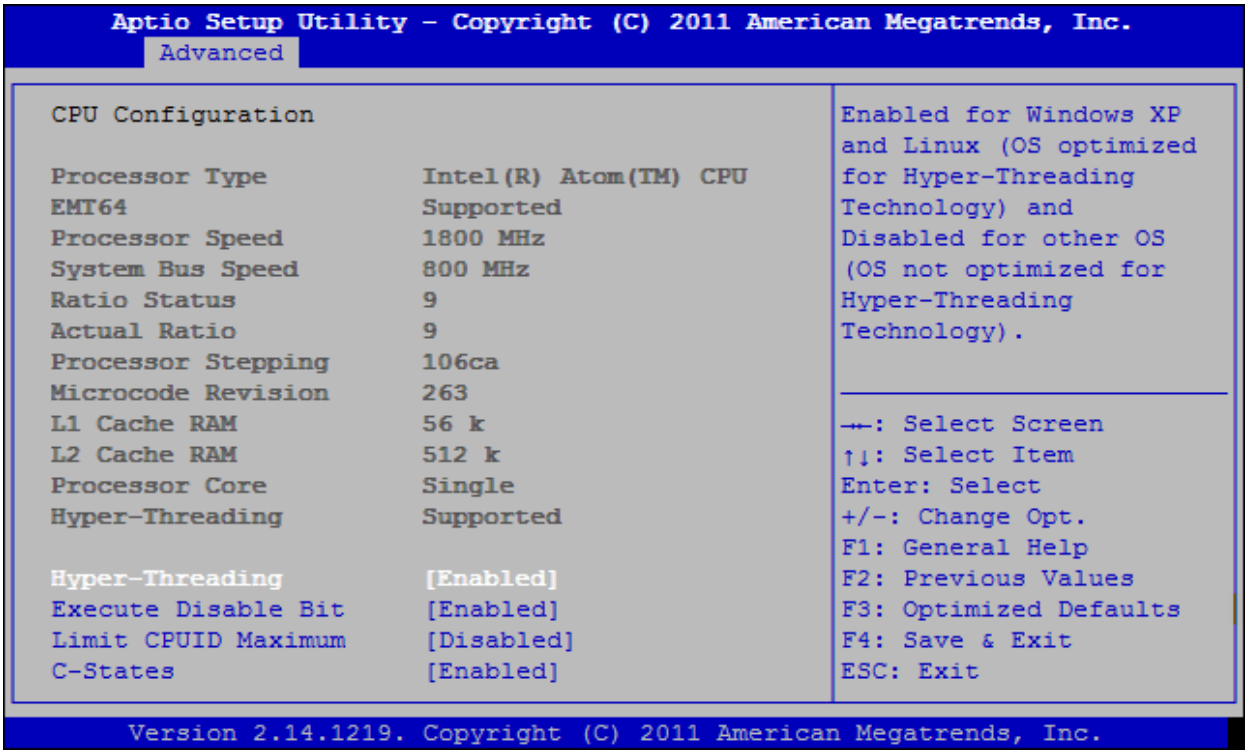
Feature	Options	Description
Enable ACPI Auto Conf	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S1 (CPU Stop Clock) **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources.

CPU Configuration (system)



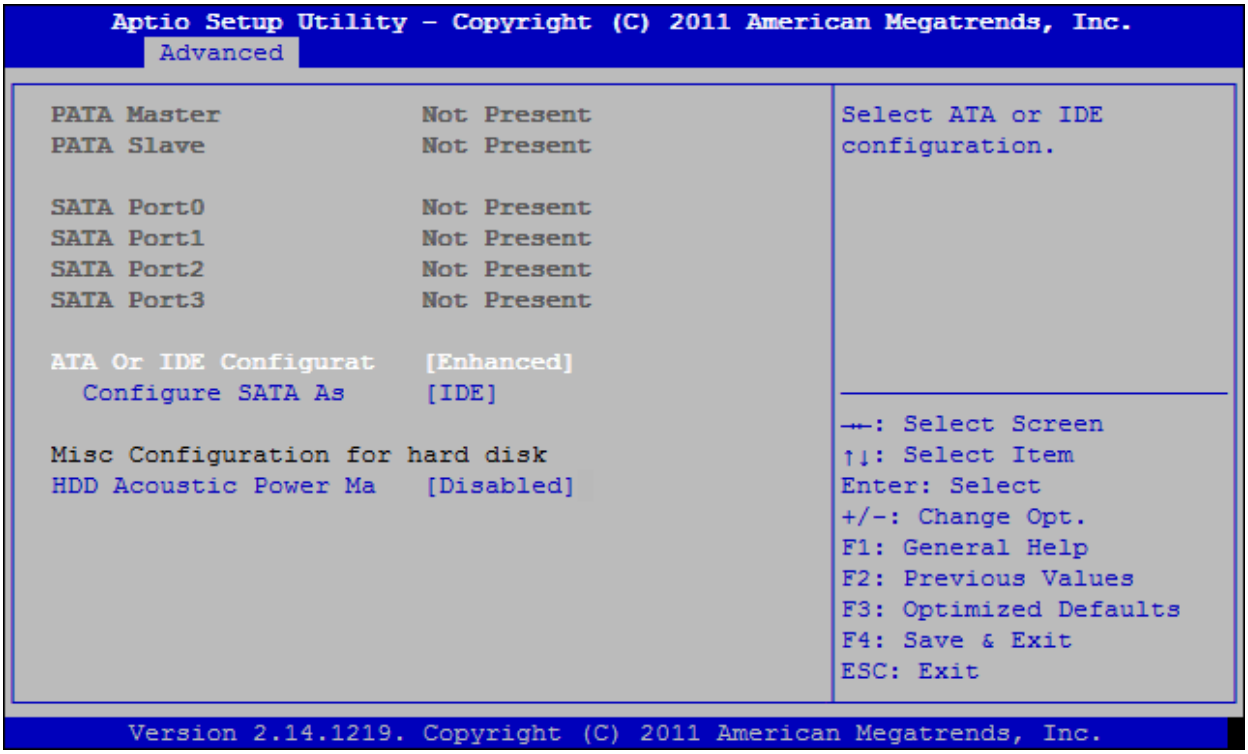
Feature	Options	Description
Hyper-Threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized of Hyper-Threading Technology).
Core-Multi Processing	Disabled **Enabled**	Enable or Disable Core-Multi Processing mode.
Execute Disable Bit	Disabled **Enabled**	XD can preven certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3)
Limit CPUID Maximum	**Disabled** Enabled	Disabled for Windows XP
C-States	Disabled **Enabled**	Enable or Disable C2 and above

CPU Configuration (board)



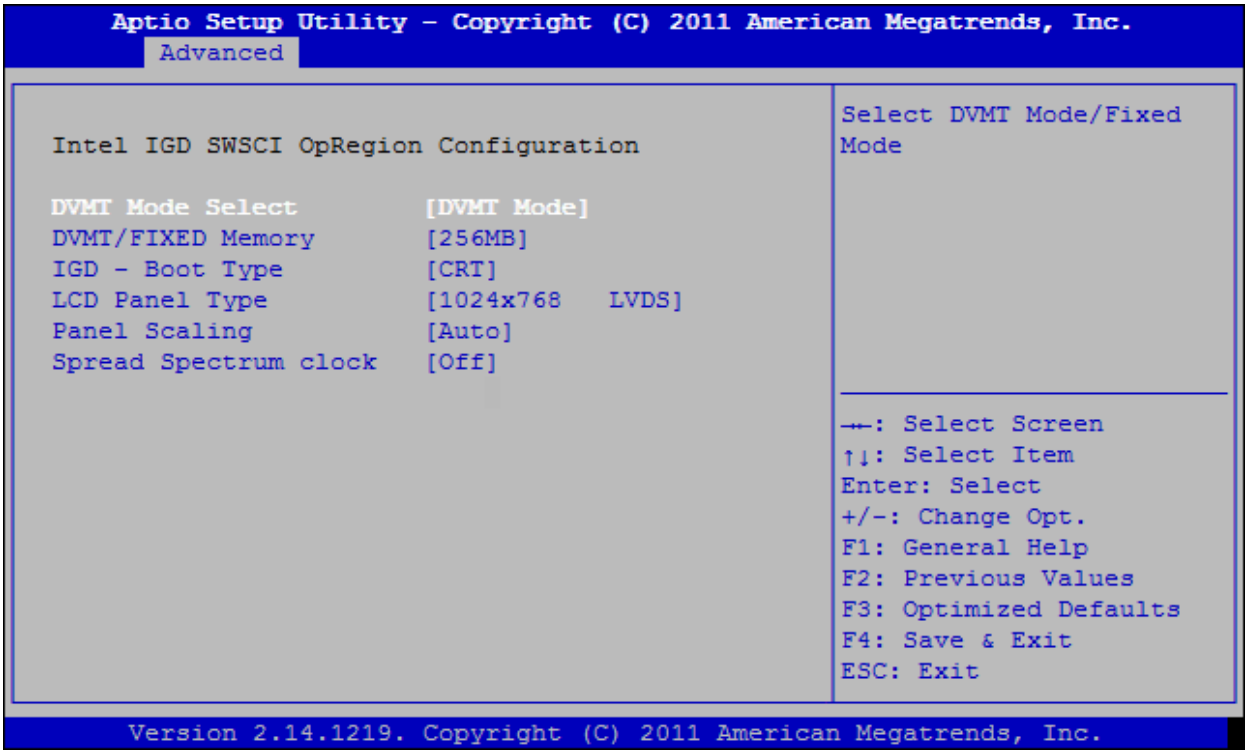
Feature	Options	Description
Hyper-Threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized of Hyper-Threading Technology).
Execute Disable Bit	Disabled **Enabled**	XD can preven certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3)
Limit CPUID Maximum	**Disabled** Enabled	Disabled for Windows XP
C-States	Disabled **Enabled**	Enable or Disable C2 and above

IDE Configuration



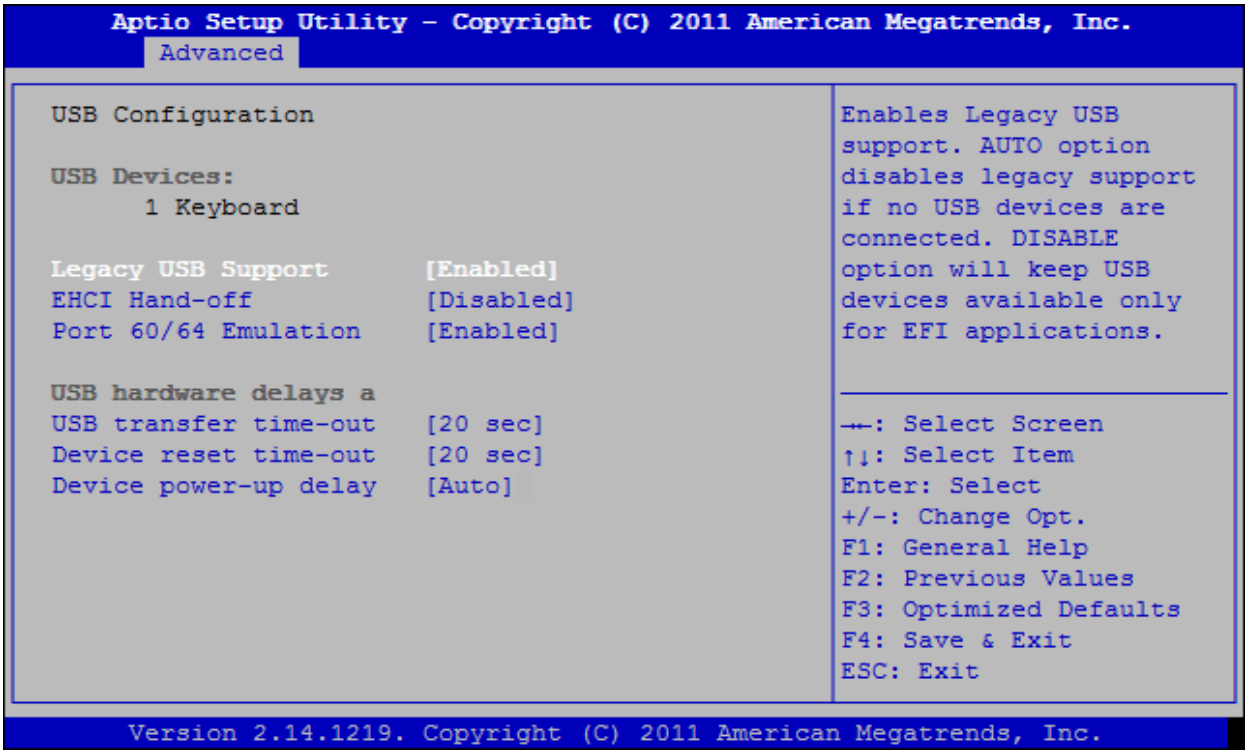
Feature	Options	Description
ATA Or IDE Configurate	Disabled Compatible **Enhanced**	Select ATA or IDE configuration.
Configure SATA As	**IDE** AHCI	Select a configuration for SATA controller.
HDD Acoustic Power Management	**Disabled** Enabled	Option to enable or disable HDD Acoustic Power Management.

Intel IGD SWSCI OpRegion Configuration



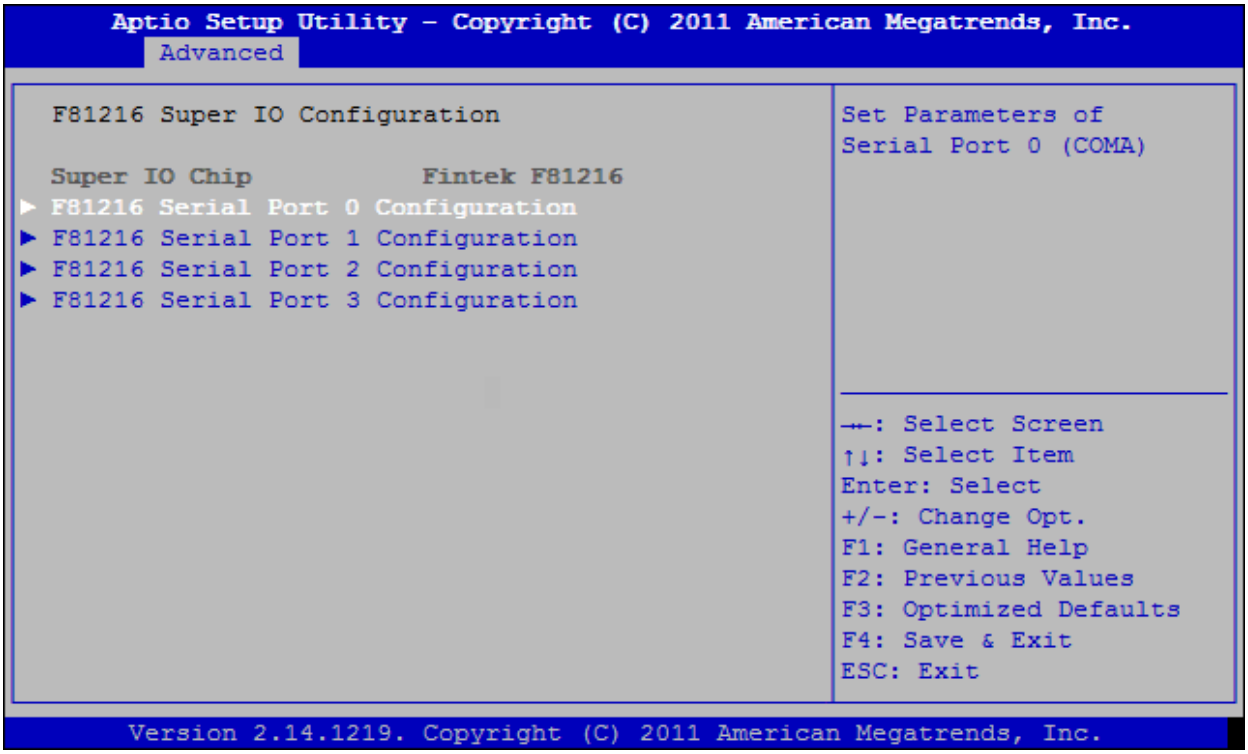
Feature	Options	Description
DVMT Mode Select	Fixed Mode **DVMT Mode**	Select DVMT Mode/Fixed Mode
DVMT/FIXED Memory	128MB **256MB** Maximum	Select DVMT Mode/FIXED Mode Memory size used by International Graphic Device
IGD – Boot Type	VBIOS Default **CRT** LFP CRT + LFP	Select the Video Device which will be activated during POST. This has no effect if external graphics present.
LCD Panel Type	640x480 LVDS 800x600 LVDS **1024x768 LVDS** 1280x768 LVDS 1280x800 LVDS 1280x600 LVDS	Select LCD panel used by International Graphics Device by selecting the appropriate setup item.
Panel Scaling	**Auto** Force Scaling Off Maintain Aspect Ratio	Select the LCD panel scaling option used by the International Graphics Device.
Spread Spectrum clock	**Off** Hardware Software	>> Hardware: Spread it controlled by chip >> Software: Spread it controlled by BIOS

USB Configuration

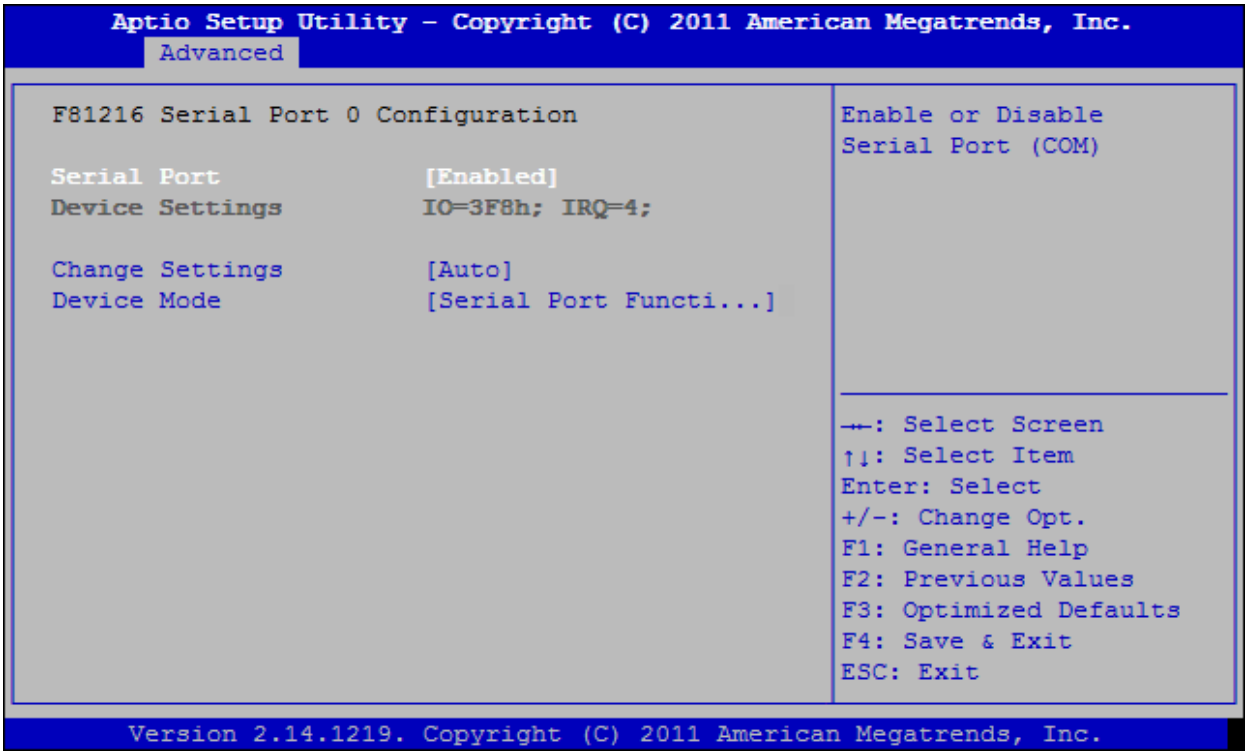


Feature	Options	Description
Legacy USB Support	**Enabled** Disabled Auto	Enabled Legacy USB support. Auto option disables Legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
EHCI Hand-off	Enabled **Disabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
Port 60/64 Emulation	**Enabled** Disabled	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OEes.
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manuel	Maximum time the device will take before it properly reports itself to the Host Controller. “Auto” uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub description.

F81216 Super IO Configuration



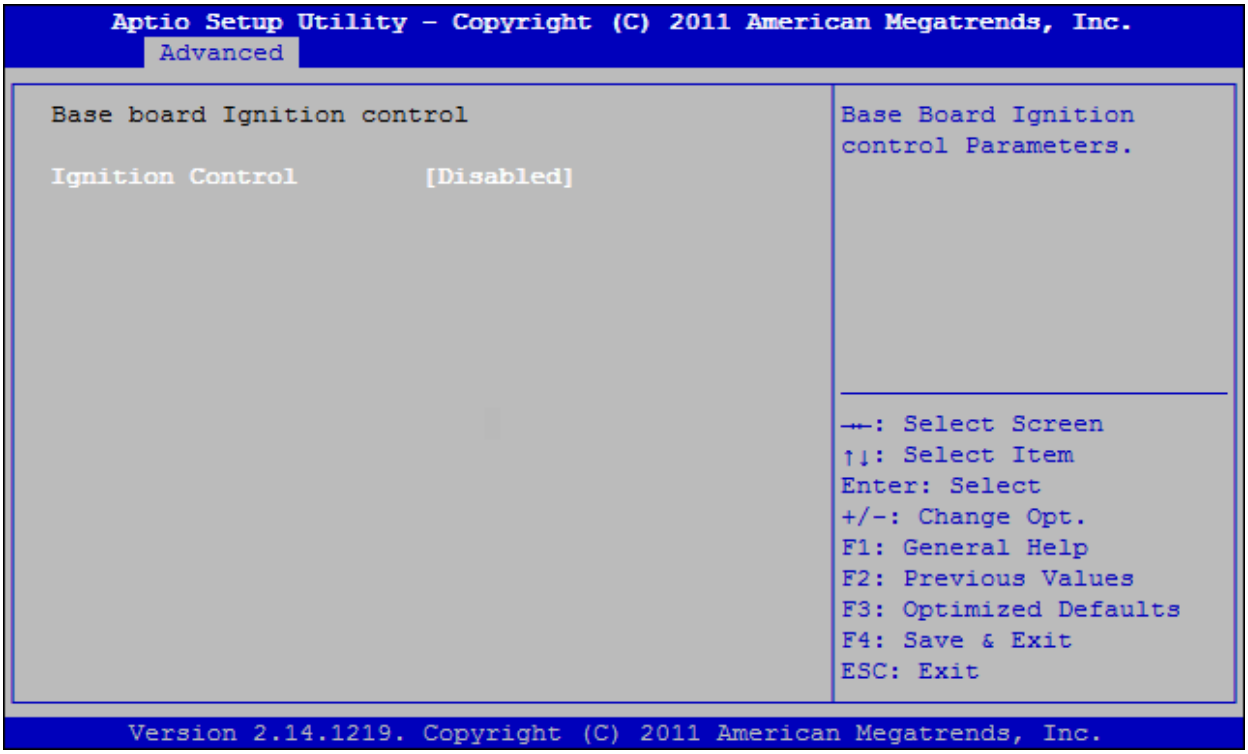
F81216 Serial Port X Configuration



Feature	Options	Description
Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM).
Change Settings	**Auto** IO=3F8h; IRQ=4; IO=3F8h; IRQ= 3, 4, 5, 6, 7, 10, 11, 12; IO=2F8h; IRQ=3, 4, 5, 6, 7, 10, 11, 12; IO=3E8h; IRQ= 3, 4, 5, 6, 7, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6 , 7, 10, 11, 12;	Select an optimal Setting for Super IO device.
Device Mode	**Serial Port Funktion Mode** IR Mode, Pusle 1.6 us, Full Duplex IR Mode, Pusle 1.6 us, Half Duplex IR Mode, Pusle 3/16 Bit Time, Full Duplex IR Mode, Pusle 3/16 Bit Time, Half Duplex	Change the Serial Port mode.

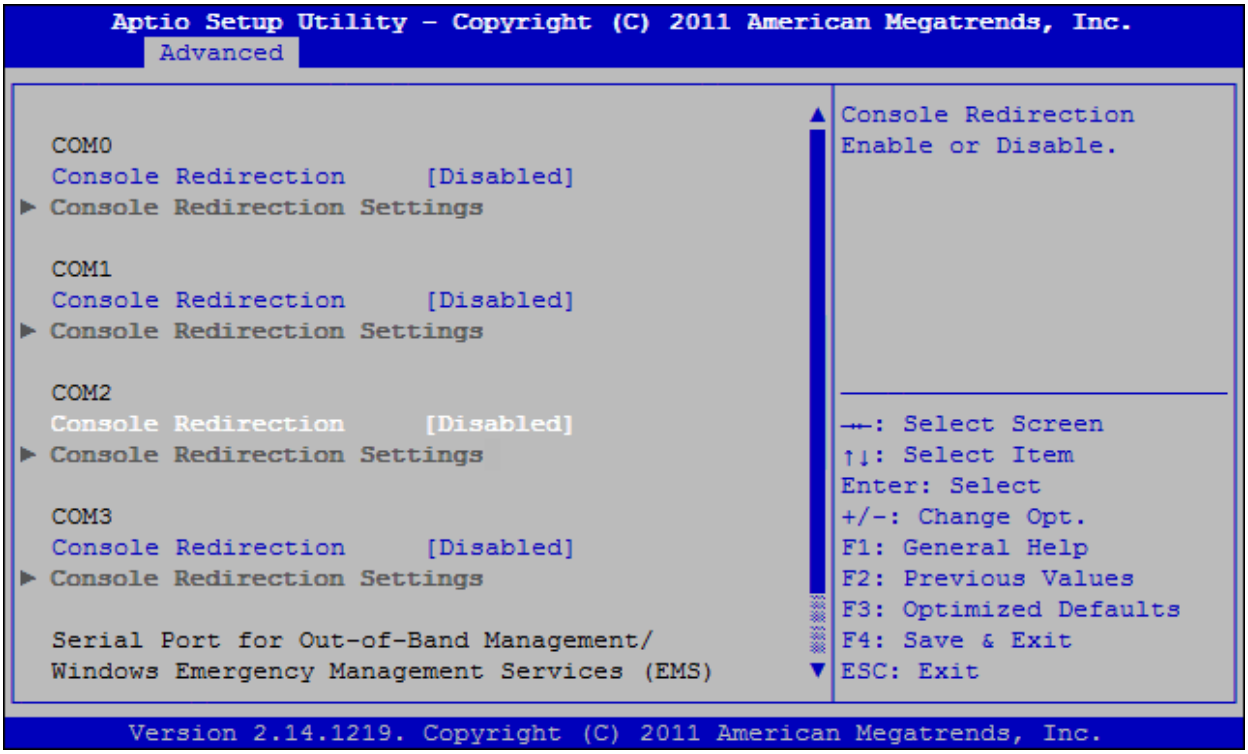
Interface Mode	**RS232** RS422 RS485	Choose interface mode.

Base board Ignition control



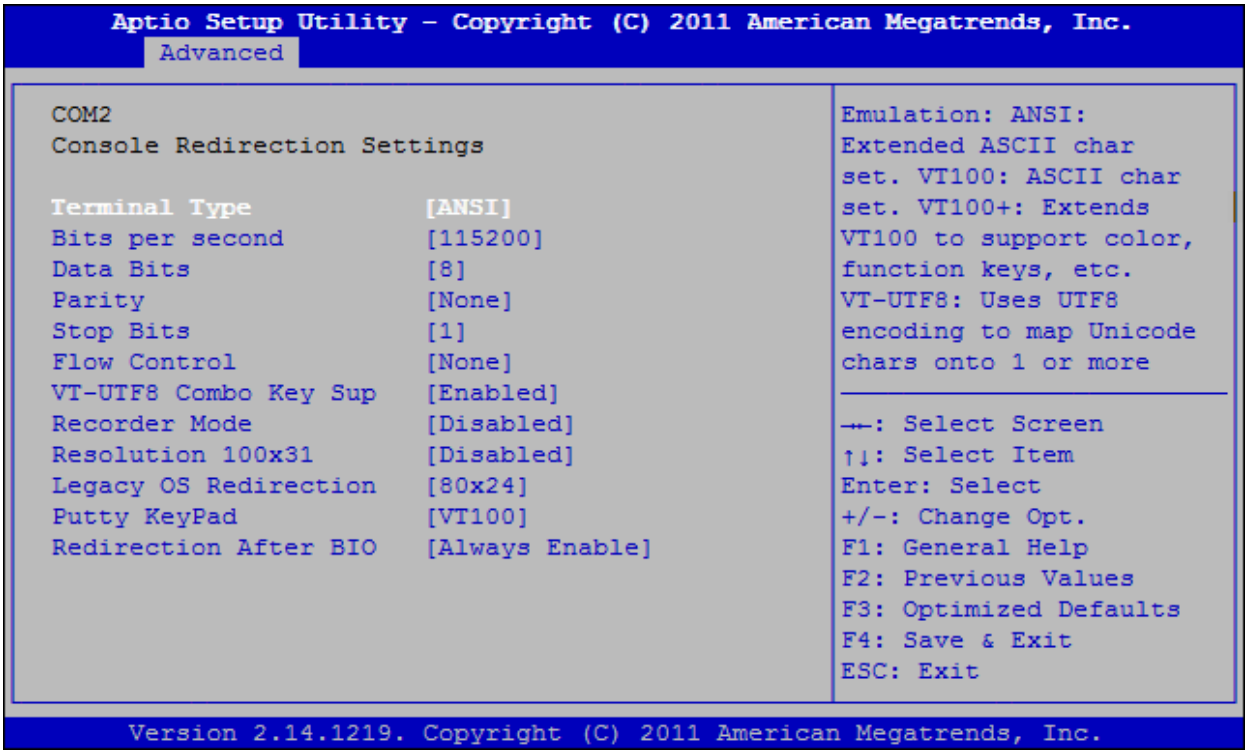
Feature	Options	Description
Ignition Control	Enabled **Disabled**	Base Board Ignition control Parameters

Serial Port Console Redirection



Feature	Options	Description
COM0 Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
COM1 Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
COM2 Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
COM3 Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.

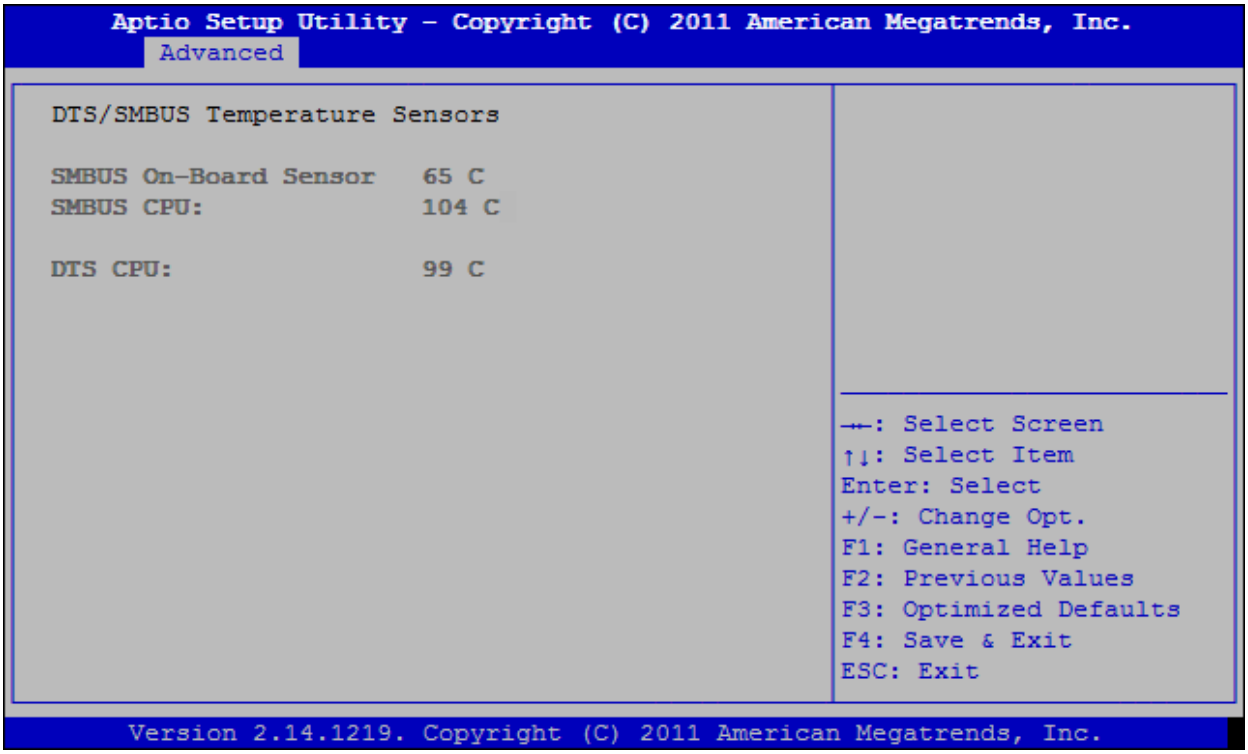
COMX Console Redirection Settings



Feature	Options	Description
Terminal Type	VT100 VT100+ **VT-UTF8** ANSI	Emulation: ANSI: Extendet ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines ma require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss form buffer overflow. When sending data, if the receiving buffers are full, a “stop”

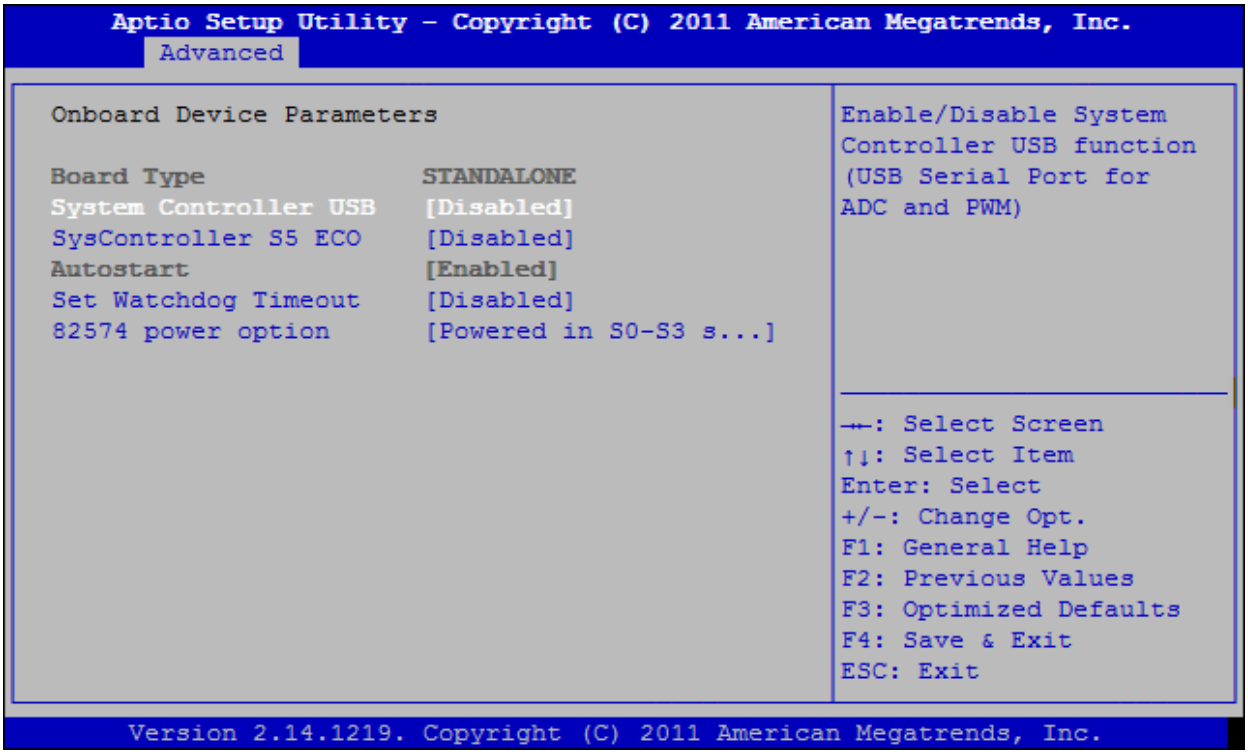
		signal can be sent to stop the data flow.
VT-UTF8 Combo Key Sup	Disabled **Enabled**	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder mMode	**Disabled** Enabled	On this mode enabled only text will be send. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty
Redirection After BIO	**Always Enable** BootLoader	The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS.

DTS/SMBUS Temperature Sensors



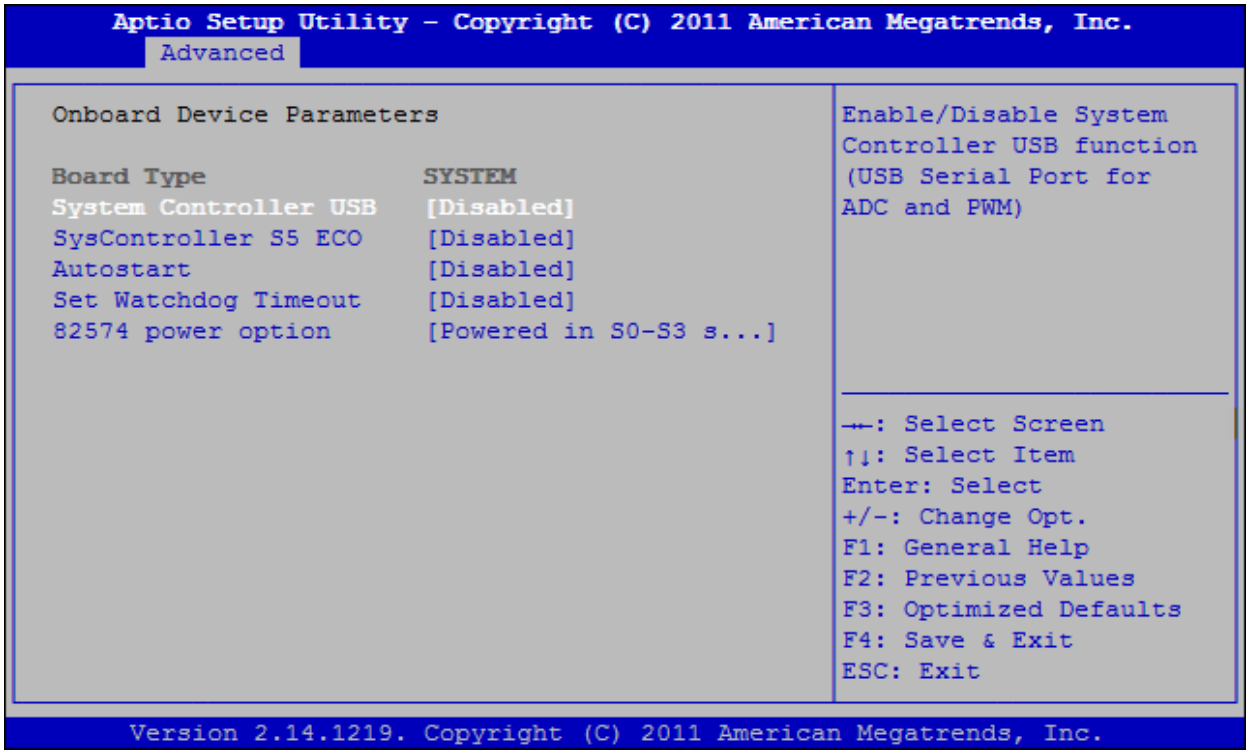
Feature	Options	Description
		Show CPU and Board Temperature

Onboard Device Parameters (board)



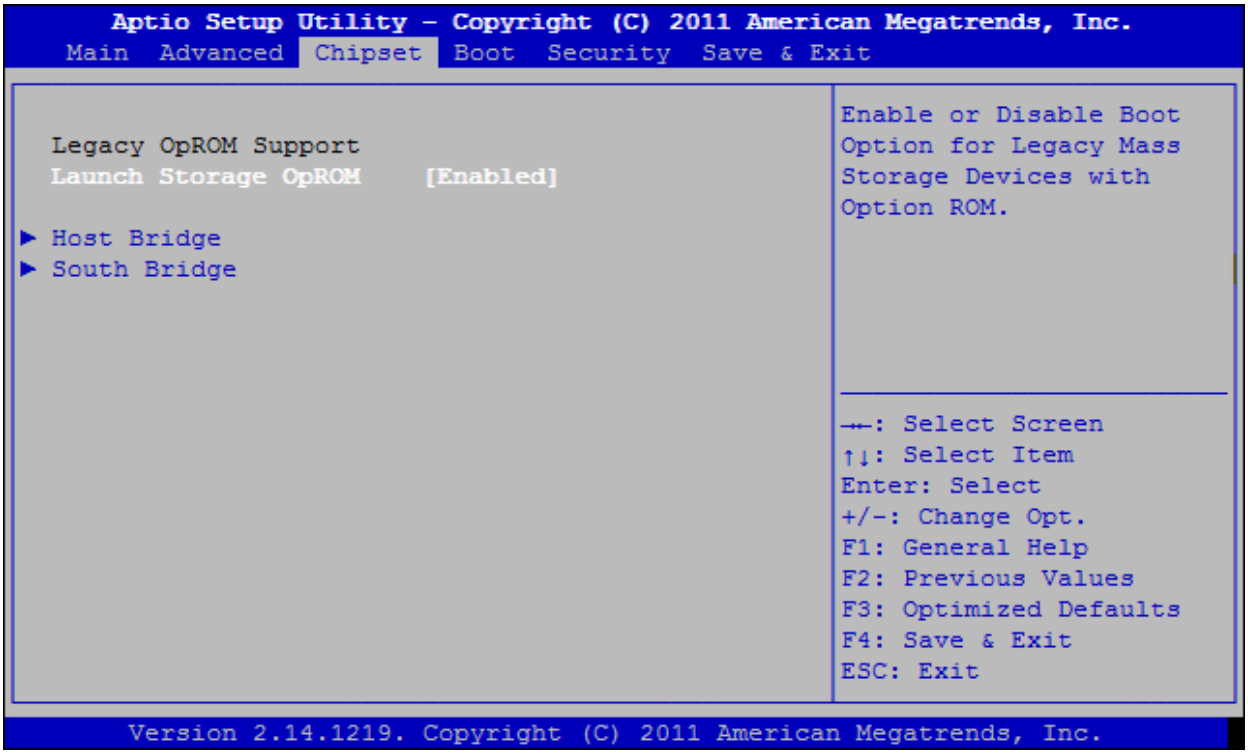
Feature	Options	Description
System Controller USB	Enabled **Disabled**	Enable/Disable System Controller USB function (USB Serial Port for ADC and PWM)
SysController S5 ECO	Enabled **Disabled**	Enable/Disable System Controller minimize power in off state (when enabled, start is allowed only form POWER BUTTON)
Set Watchdog Timeout	**Disabled** 5 Minutes 15 Minutes	Enable/Disable Watchdog Timer while Boot
82574 power option	Powered in S0 state **Powered in S0-S3 state** Powered in S0-S5 state Always Off	Enable Interface Power in S0/S3/S5 state, valid during start after shutdown to S5 (not to ECO mode)

Onboard Device Parameters (system)



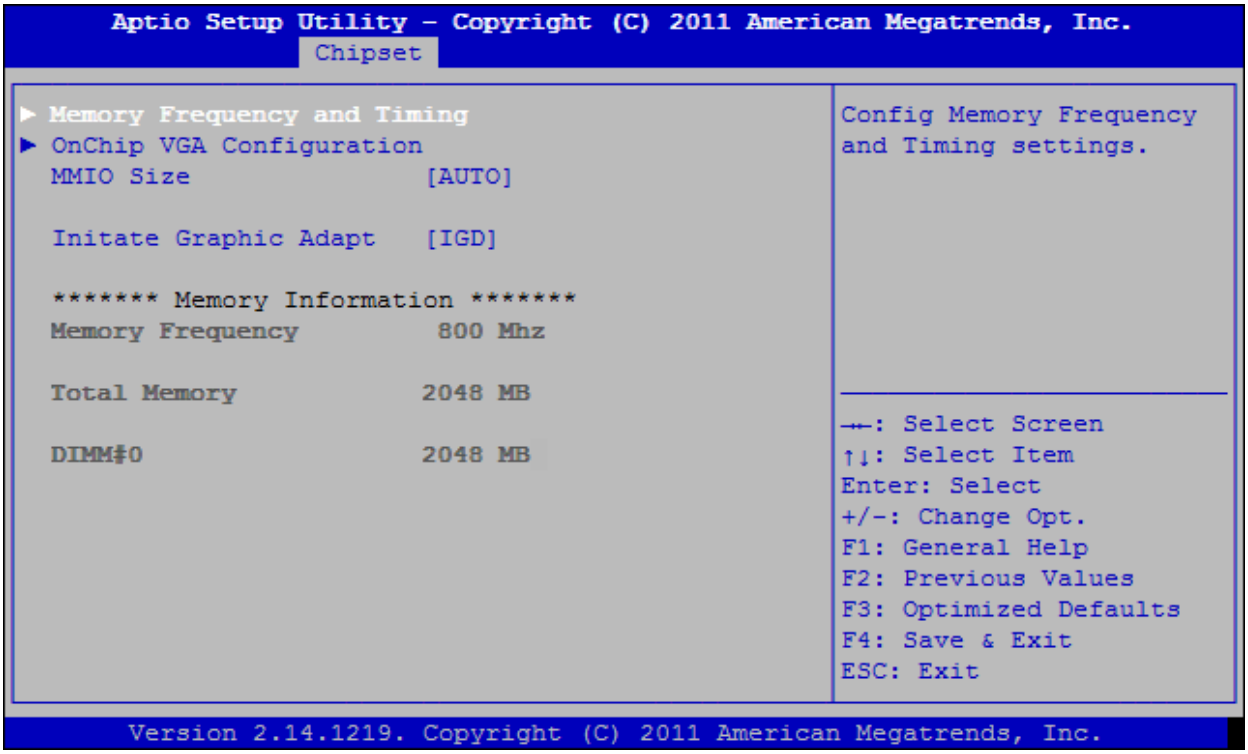
Feature	Options	Description
System Controller USB	Enabled **Disabled**	Enable/Disable System Controller USB function (USB Serial Port for ADC and PWM)
SysController S5 ECO	Enabled **Disabled**	Enable/Disable System Controller minimize power in off state (when enabled, start is allowed only form POWER BUTTON)
Autostart	Enabled **Disabled**	Enable/Disable Autostart Function
Set Watchdog Timeout	**Disabled** 5 Minutes 15 Minutes	Enable/Disable Watchdog Timer while Boot
82574 power option	Powered in S0 state **Powered in S0-S3 state** Powered in S0-S5 state Always Off	Enable Interface Power in S0/S3/S5 state, valid during start after shutdown to S5 (not to ECO mode)

6.3.3 Chipset Menu



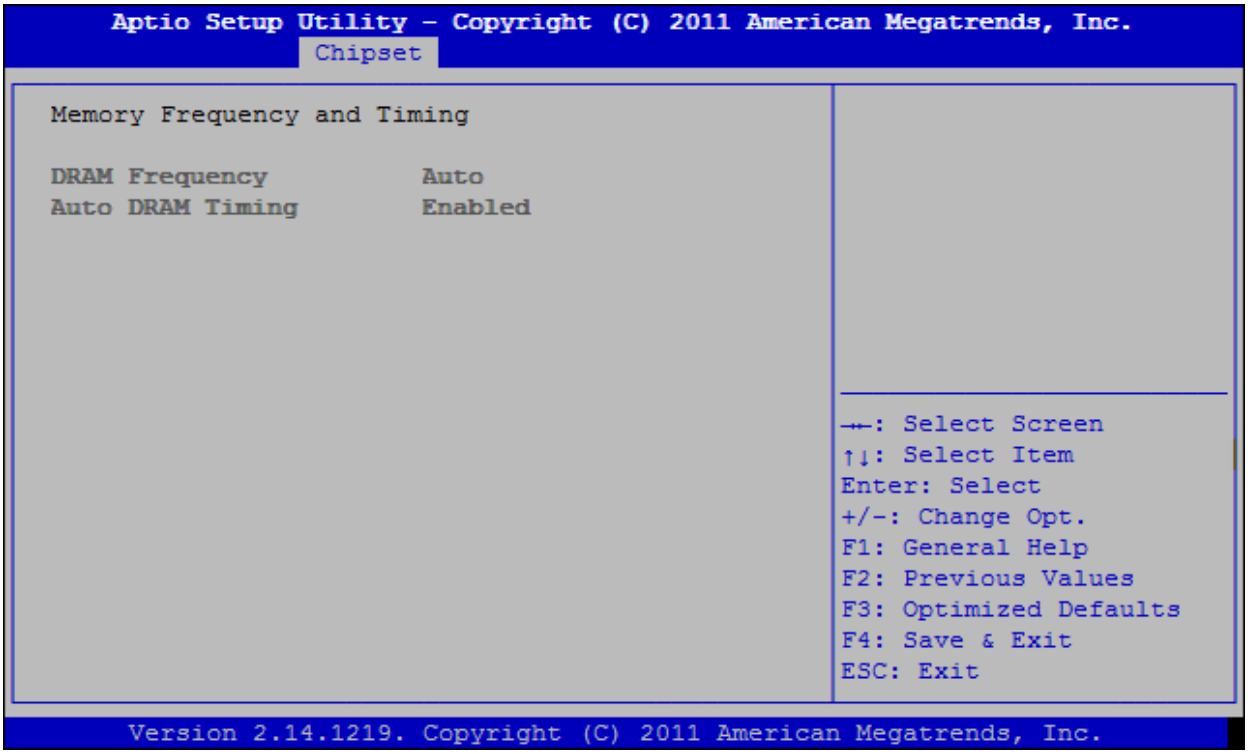
Feature	Options	Description
Launch Storage OpROM	**Enabled** Disabled	Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

Host Bridge

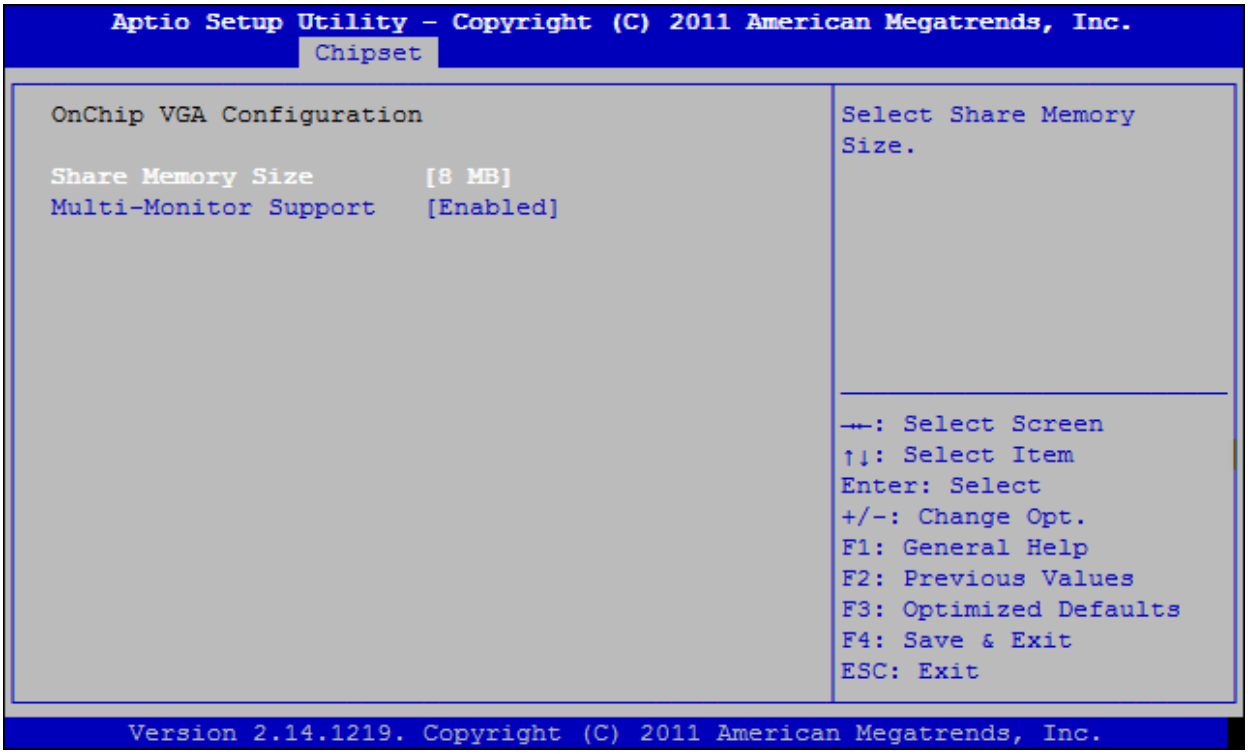


Feature	Options	Description
Memory Frequency and Timing		Config Memory Frequency and Timing settings
OnChip VGA Configuration		Config On Chip VGA Settings.
MMIO Size	**AUTO** 1GB 2GB	Set reserver memory size for MMIO
Initate Graphic Adapt	**IGD** PCI/IGD PCI/PEG PEG/IGD PEG/PCI	Select which graphics controller to use as the primary boot device.

Memory Frequency and Timing

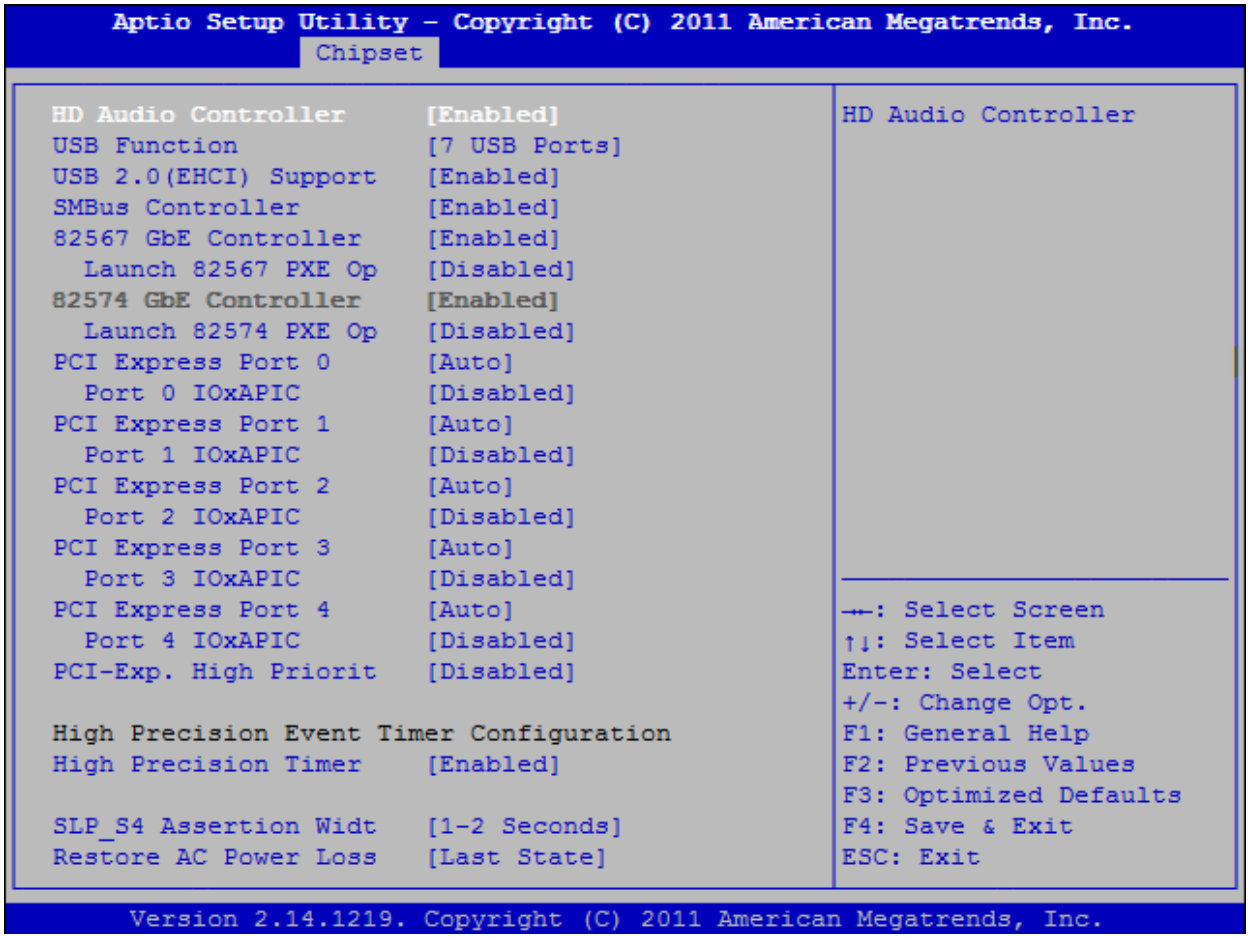


OnChip VGA Configuration



Feature	Options	Description
Share Memory Size	Disabled 1 MB **8 MB**	Select Share Memory Size
Multi-Monitor Support	Disabled **Enabled**	Enable the Multi-Monitor mode.

South Bridge



Feature	Options	Description
HD Audio Controller	**Enabled** Disabled	HD Audio Controller
USB Function	Disabled 2 USB Ports 4 USB Ports 6 USB Ports **7 USB Ports**	Enable or disable USB Function
USB 2.0 (EHCI) Support	**Enabled** Disabled	Enable or disabled USB 2.0 (EHCI) Support.
SMBus Controller	**Enabled** Disabled	Enable or disable onchip SMBus Controller
82567 GbE Controller	**Enabled** Disabled	Enable or disable onchip 82567 GbE Controller.
Launch 82567 PXE Op	**Disabled** Enabled	Enable or disable Boot Option for Intel 82567 Network Device.
Launch 82574 PXE Op	**Disabled** Enabled	Enable or Disable Boot Option for Intel 82574 Networ Device.

PCI Express Port 0	**Auto** Enabled Disabled	Enable or disable PCI Express Root Port 0.
Port 0 IOxAPIC	**Disabled** Enabled	Enable or disable PCI Express Port 0 IO APIC
PCI Express Port 1	**Auto** Enabled Disabled	Enable or disable PCI Express Root Port 1.
Port 1 IOxAPIC	**Disabled** Enabled	Enable or disable PCI Express Root Port 1 IO APIC
PCI Express Port 2	**Auto** Enabled Disabled	Enable or disable PCI Express Root Port 2.
Port 2 IOxAPIC	**Disabled** Enabled	Enable or disable PCI Express Root Port 2 IO APIC.
PCI Express Port 3	**Auto** Enable Disable	Enable or disable PCI Express Root Port 3.
Port 3 IOxAPIC	**Disabled** Enabled	Enable or disable PCI Express Root Port 3 IO APIC
PCI Express Port 4	**Auto** Enabled Disabled	Enable or disable PCI Express Root Port 4
Port 4 IOxAPIC	**Disabled** Enabled	Enable or disable PCI Express Root Port 4 IO APIC.
PCI-Exp. High Priority Port	**Disabled** Port 0 Port 1 Port 2 Port 3 Port 4 Port 5	Select a PCI Express High Priority Port.
High Precision Timer	Disabled **Enabled**	Enable or disable the High Precision Event Timer.
SLP_S4 Assertion Width	1-2 Seconds 2-3 Seconds 3-4 Seconds 4-5 Seconds	Select a minimum assertion width of the SLP_S4# signal
Restore AC Power Loss	Power Off Power On **Last State**	Select AC power state when power is re-applied after a power failure.

6.3.4 Boot Menu

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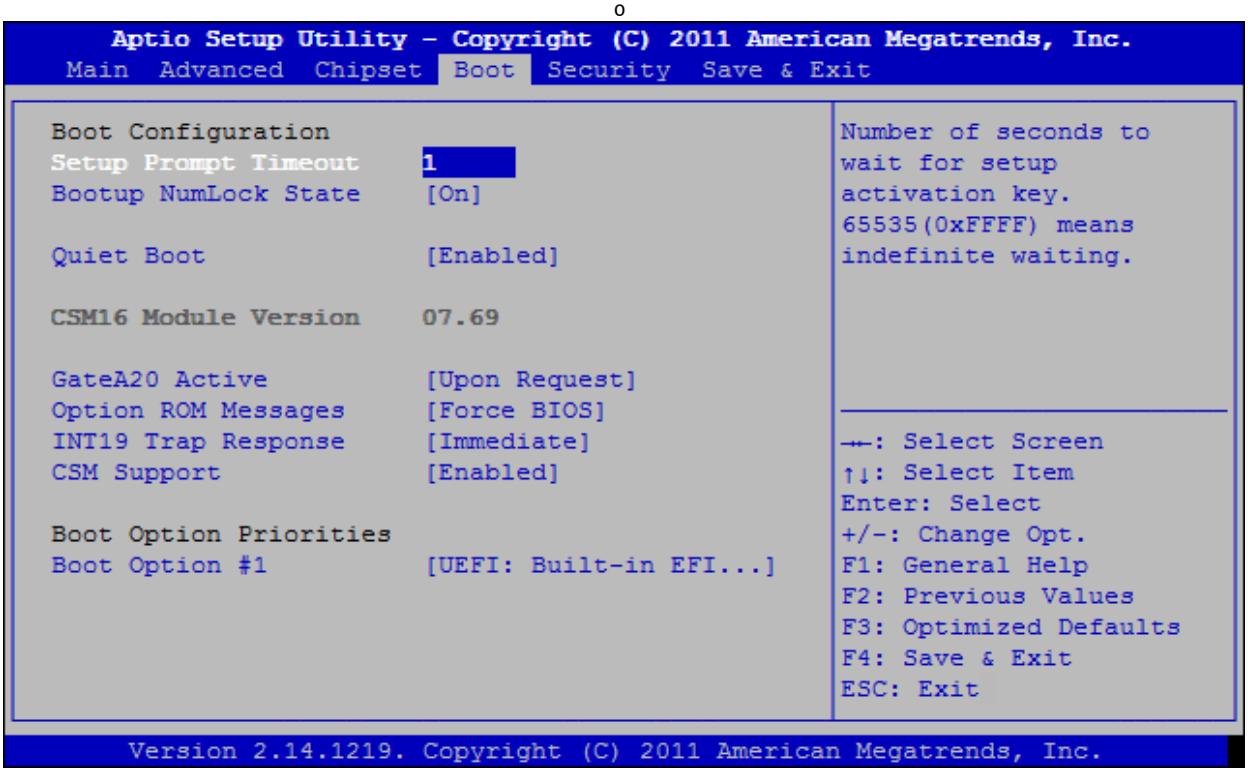

Feature	Options	Description
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** OFF	Select the keyboard NumLock state.
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Gate A20 Active	**Upon Request** Always	UPON REQUEST – GA20 can be disabled using BIOS services. ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Oprion ROM Messages	**Force BIOS** Keep Current	Set display mode for Option ROM
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE – execute the trap right away; POSTPONED - execute the trap during legacy boot.
CSM Support	Disabled **Enabled** Auto	Enable/Disable CSM Support. If Auto is selected, based on OS, CSM will be enabled/disabled automatically.
Boot Option #1	**UEFI: Built-in EFI Shell** Disabled	Sets the system boot order

6.3.5 Security Menu

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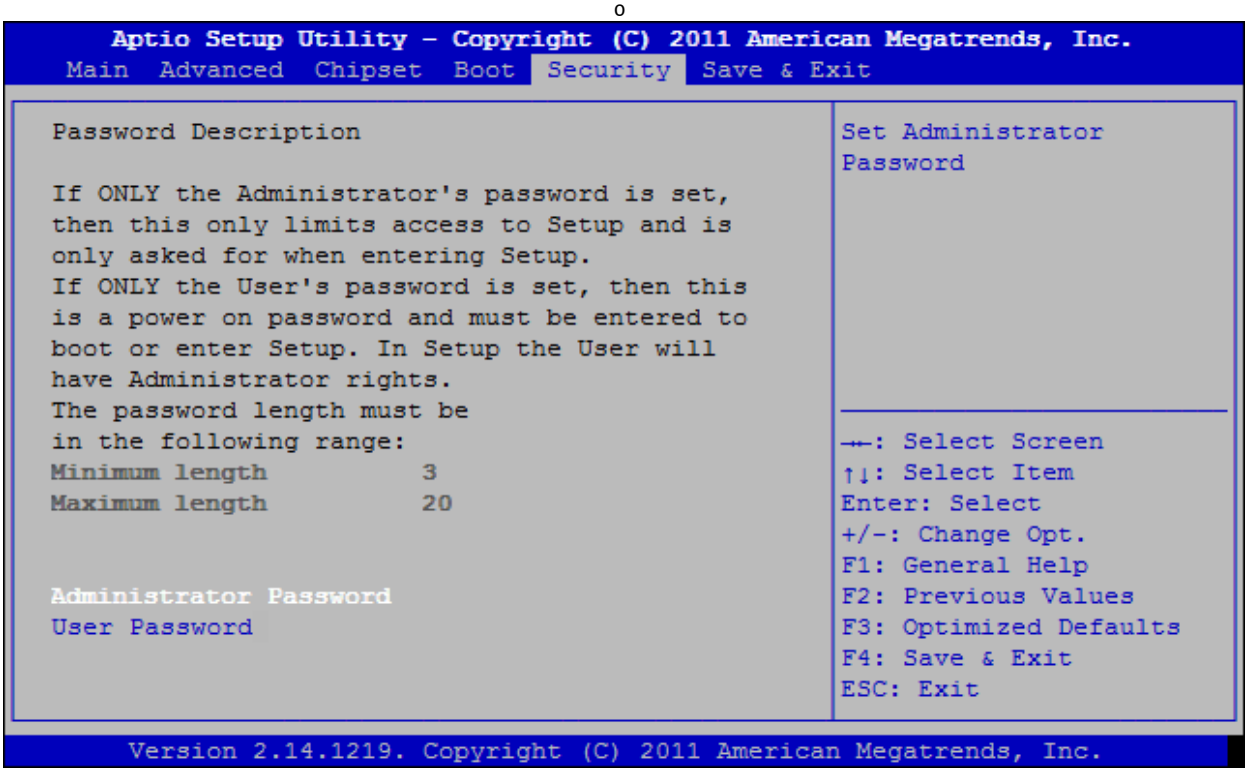
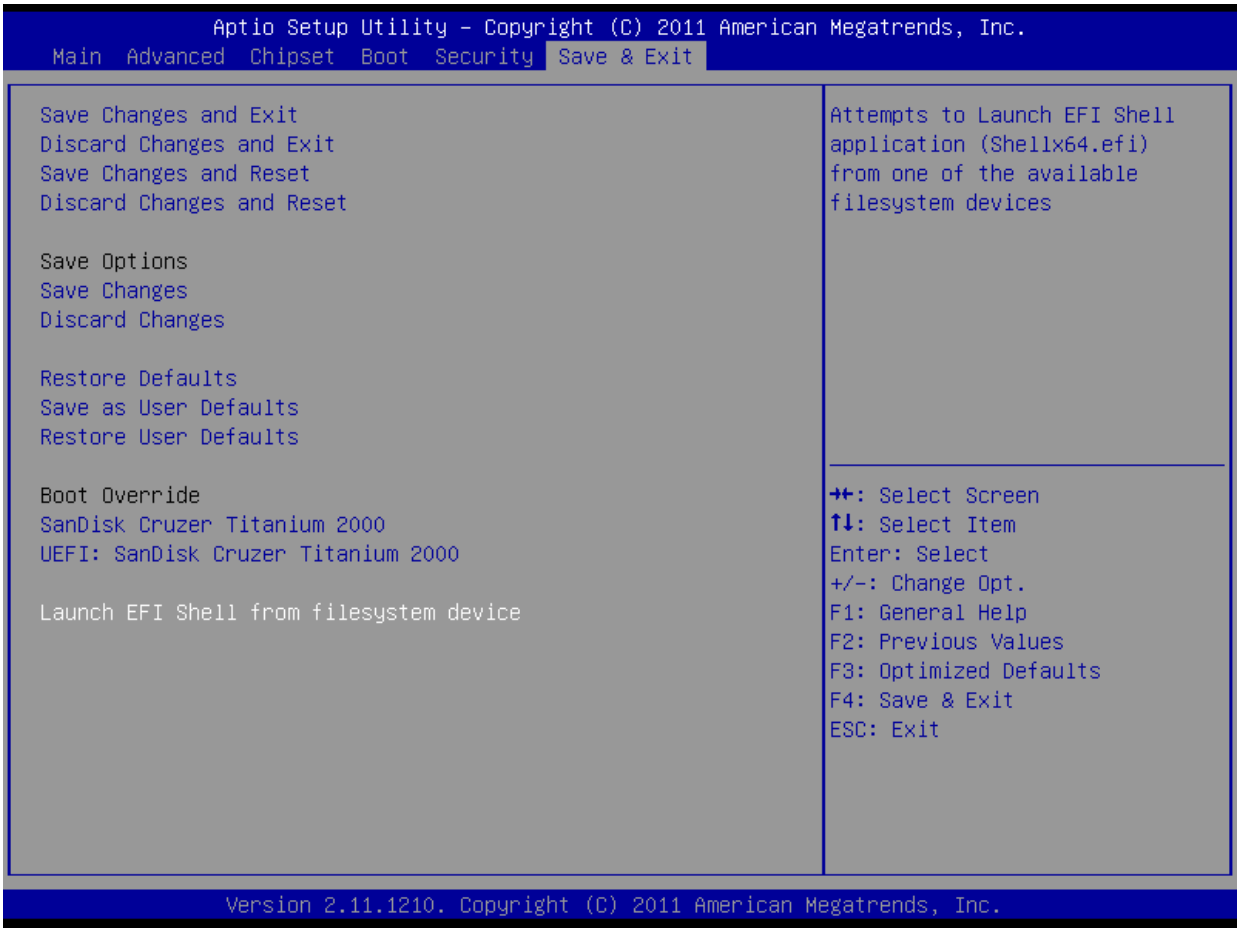


Feature	Options	Description
Administrator		Set Administrator Password
User Password		Set User Password

6.3.6 Exit Menu



Feature	Description
Save Changes and Reset	Exit utility and save your changes to CMOS.
Discard Changes and Exit	Exit utility without saving setup data to CMOS.
Save Changes	Save setup data to CMOS.
Discard Changes	Load previous values from CMOS for all setup items.
Load Setup Defaults	Load default values for all setup items.

6.4 BIOS Update

Before downloading a BIOS, please check the following:

Make a bootable diskette which includes the following files:

- DLDELEP.exe
- afudos.exe
- core BIOS (MSMLPxxx.ROM)
- Rename the MSMLPxxx.ROM file to bios.rom

IMPORTANT: Do not use boot disks created in a Windows operating system. If you do not have an MSDOS 6.22 disk available, you can download a boot disk from www.bootdisk.com.

Notes:

- Disable the EMM386 or other memory managers in the CONFIG.SYS of your boot disk.
- Make sure that the AFUDOS.exe program and the BIOS are in the same path and directory!
- Boot DOS without config.sys and autoexec.bat. (Press **F5** while starting the DOS boot).

Start the DOWNLOADING process:

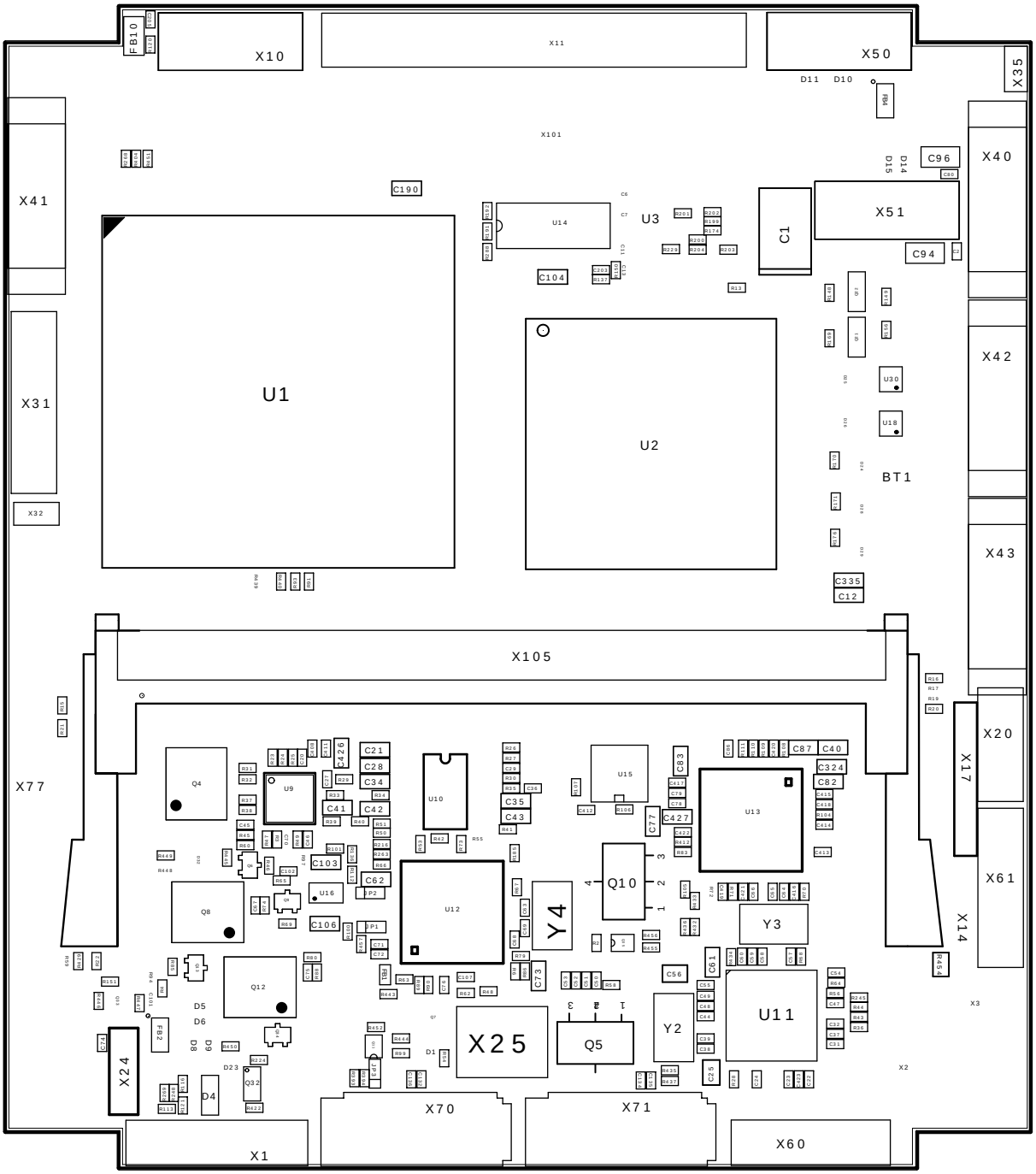
1. Start the system using the bootable diskette.
2. Run DLDELEP.exe to clear the CMOS and the EEPROM.

WARNING: If you do not run DLDELEP.exe, the system will be destroyed during the BIOS upgrade!

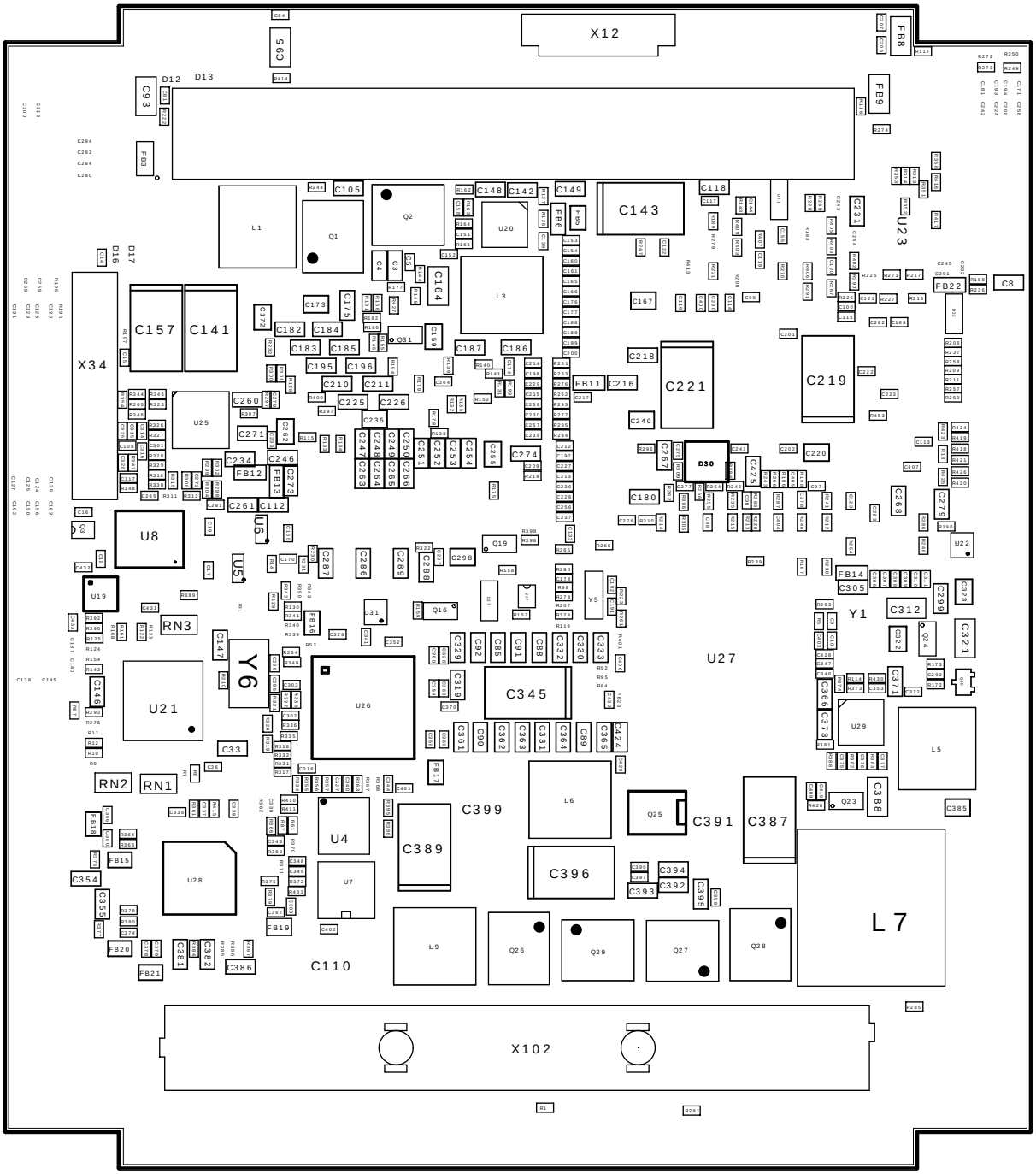
3. Run AFUDOS.EXE BIOS.ROM /X /B /P /N.
4. Reboot the system and press **DEL** to enter the setup mode. Set the default values by pressing **F3**.
5. "Save and exit" the setup by pressing **F4**.
6. Reboot the system.

7 Appendix A: Assembly Views

7.1 Top



7.2 Bottom


X12
C95
FB8
D12
D13
C93
FB9
FB3
C105
Q2
C148
C142
C149
C143
C118
L1
Q1
U20
FB6
FB5
C231
U23
D16
D17
C4
C3
C164
L3
FB22
C8
C157
C141
C172
C173
C175
C182
C184
Q31
C159
C187
C186
C167
X34
C183
C185
C195
C196
C210
C211
C218
C221
C219
FB11
C216
C260
U25
C225
C226
C235
C240
C271
C242
C247
C248
C249
C250
C251
C252
C253
C254
C255
C274
C267
D30
C220
C234
C246
FB12
FB13
C273
C261
C112
C180
C268
C279
U8
U6
Q19
U22
U5
C287
C286
C289
C288
C298
FB14
C305
C299
C323
U19
Y5
Y1
C312
RN3
U31
Q16
C322
C321
C147
Y6
C329
C92
C85
C91
C88
C332
C330
C333
U27
C146
U21
U26
C345
C319
C366
C371
C373
U29
L5
C33
C361
C90
C362
C363
C331
C364
C89
C365
C424
RN2
RN1
FB17
L6
Q25
C391
C387
Q23
C388
C385
C399
U4
C389
C396
C394
C392
C393
C395
FB18
FB15
C354
U28
U7
C355
FB19
L7
L9
Q26
Q29
Q27
Q28
FB20
C381
C382
C386
FB21
C110
X102

8 Appendix: Document Revision History

Document Revision History

Revision	Date	Edited by	Changes
100	12.Oct.2011	WAS	Intial released version
101	29.Nov.2011	WAS	BRM: table in Section 4.3.1 corrected. AVM: 4GB DDR3 correction. BRW: clarification of Watchdog timeout settings.
102	01.Mar.2012	WAS/MEG	NK 10957: Eval Kit has PCI-104 assembled. MEG: X24 connector description. WAS: Assembly diagrams enhanced.
103	16.May.2012	WAF/VIV	Adoption to version V1.1. WAF: Modules added. Renumbering of connectors. Backlight connector X12, analog output changed to PWM. COM3 / 4 swapped on PCB. Fan connector X24: voltage changed to 5V. Remarks for system boards. Jumper adopted to V1.1. Power information FPC connector X11and Backlight connector X12 changed. VIV: New chapter 4.1 KeAPI , chaper 4.4.1 I/O Control Access changed
104	04.Sep.2013	UMA	Changed to new Kontron Corporate Design, updated drawings
105	12.Nov.2013	UMA	Added BIOS description
106	10.Dez.2013	UMA	Removed SSD option

Corporate Offices

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