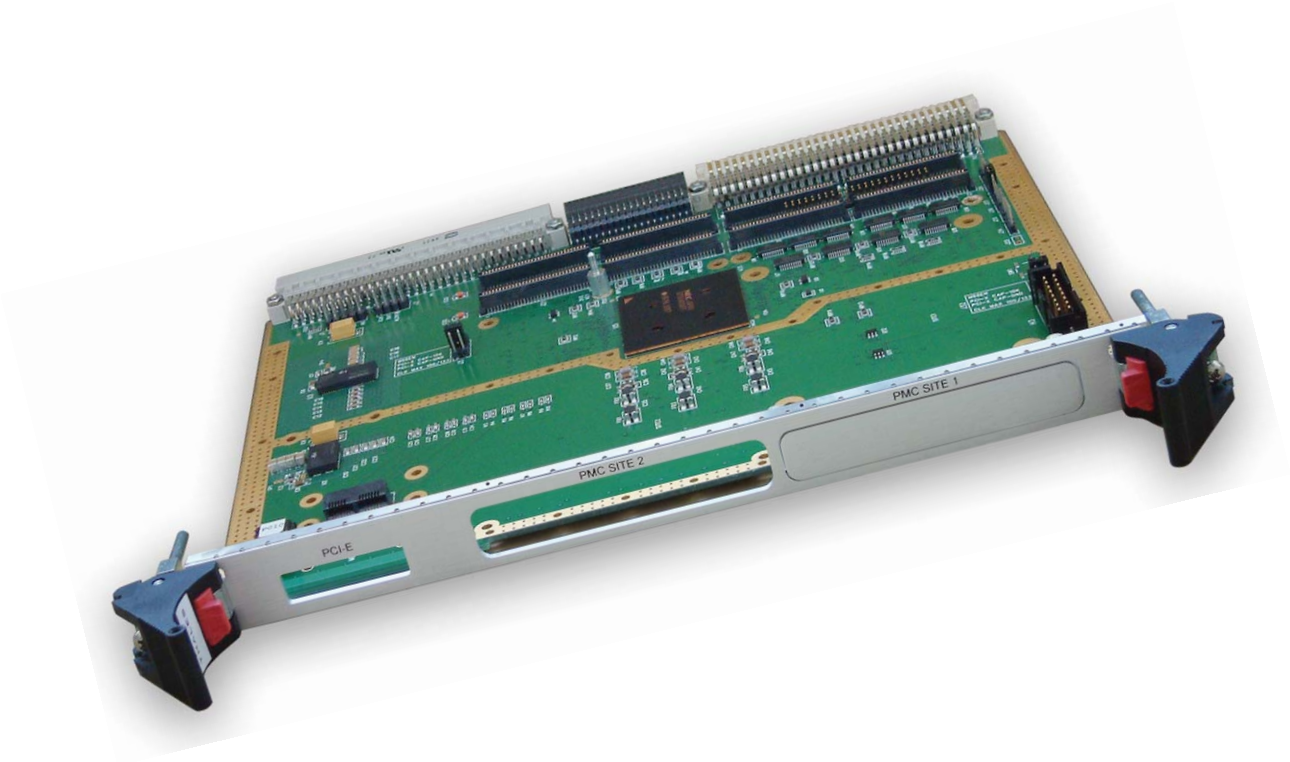

V2PMC2 Dual Slots PCI-X/PMC VME Carrier User's Guide

CA.DT.A11-2e — October 2008

Revision History

Publication Title:	V2PMC2 User's Guide	
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Rev.	**Brief Description of Changes**	**Date of Issue**
2e	Fix a problem in 5.1.1 P0 Connector Pin Assignment	10-2008

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention.

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, 'k' 'M' and 'G' mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$ $*2^{20}$ *and* $*2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

Personal Injury

Be careful while handling the board, because of the cutting edges of the CPU heatsink.

Do not touch the CPU heatsink or the ruggedizer while removing the board from a rack because it can get very hot.

Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

Chapter 1 - Overview

The V2PMC2 is a major leap forward in Modular 6U VME COTS architecture. It allows both to significantly expand the number of PMC modules attached to a processor card by using a high bandwidth scalable PCI-Express link, and the data throughput available to these PMC modules.

The V2PMC2 PCI-X/PMC carrier card is a 6U VME that holds up to two single-width or one double-width PCI-X/PMC modules.

The V2PMC2 works in association with a PCI-Express host which is connected to it through a x4 PCI-Express serial link.

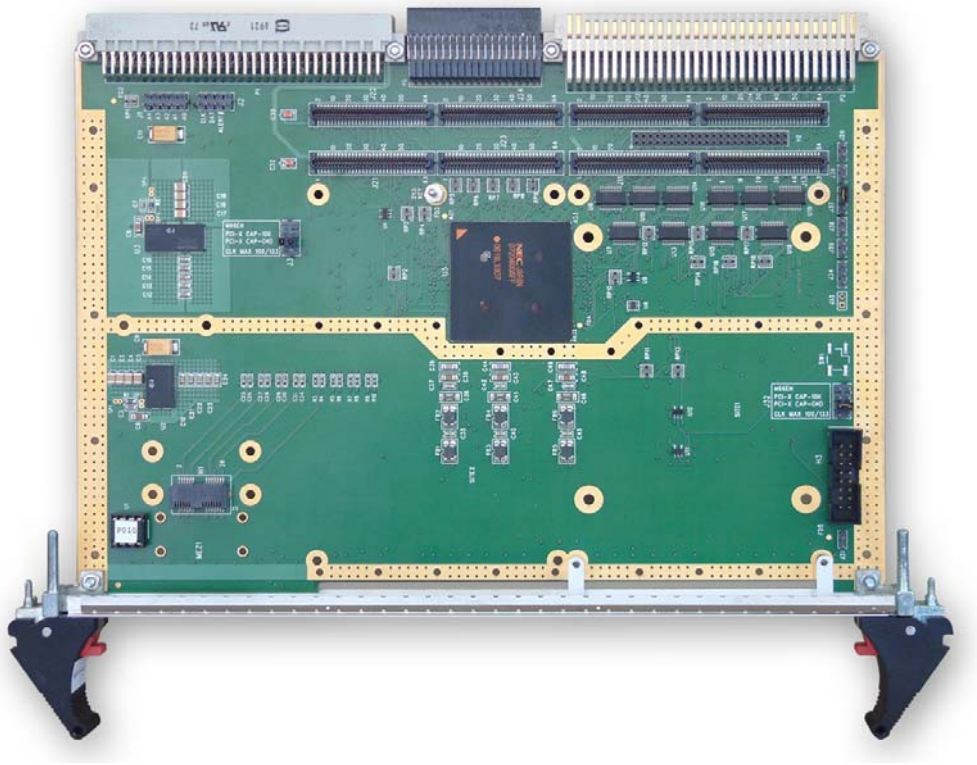


Figure 1: V2PMC2 Overview

The following table shows the number of PMC slots available with the motherboard (PENTXM2 and PENTXM4) and with or without the V2PMC2 carrier board:

Configuration	PMC Slots Available	VME Slots Used
PENTXM2 and PENTXM4 configuration without a V2PMC2	2	1
PENTXM2 and PENTXM4 configuration with a V2PMC2	4	2

Order Code

V2PMCX-SA-010 . . . . . Dual Slot PCI-X / PMC VME carrier

1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the V2PMC2 board.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.2 Audience

This manual is a guide and reference handbook for engineers and system integrators who wish to use Kontron V2PMC2 carrier board. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding, VME, and communications.

1.3 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 (this chapter) - Brief introduction, this guide's objectives and audience, the structure, some warnings, conventions, and related documentation
- Chapter 2 - Technical Specification
- Chapter 3 - Preparing before Using
- Chapter 4 - Functional Description
- Chapter 5 - Connectors
- Chapter 6 - Installation

1.4 Related Documents

Hardware

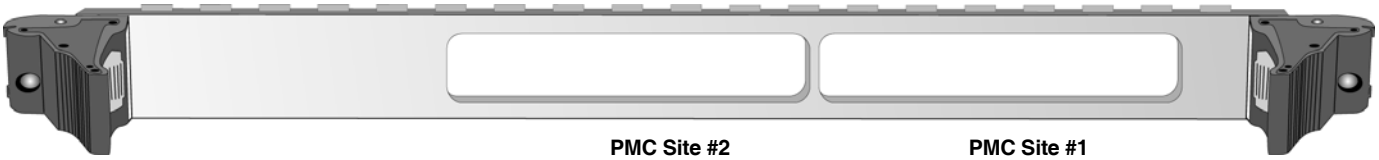
- PENTXM2 and PENTXM4 Hardware Release Notes, ... CA.DT.A09
- PENTXM2 and PENTXM4 User's Guide, ... CA.DT.A07
- PENTXM2 and PENTXM4 Connection Guide, ... CA.DT.A10

- R2U4S - Rack Mount Industrial Chassis - Installation and User's Manual SD.DT.E84
- R8U16S - Rack Mount Industrial Chassis - Installation and User's Manual SD.DT.E85

Standard

- PCI Local Bus Specification Revision 3.0, PCI Special Interest Group.
- IEEE Std 1386-2001 Standard for a Common Mezzanine Card (CMC) Family.
- IEEE Std 1386.1-2001 Physical and Environmental Layers for PCI Mezzanine Cards (PMC).
- VITA 35-2000 PMC-P4 Pin Out Mapping to VME-P0 and VME64x-P2.
- VITA 36-199x PMC I/O Module Draft Standard.
- VITA 39-2003 PCI-X Auxiliary Standard for PMCs and Processor PMCs.
- PICMG 2.18 Serial RapidIO Specification

Chapter 2 - Technical Specifications



PCI Interface

PCI Interface	PMC Site #1 PMC Site #2	PCI–X, 100/66/33 MHz, 64/32 bits PCI–X, 133/100/66/33 MHz, 64/32 bits
PMC Slots	2	
PCI I/O Signaling Voltage	PMC Site #1 PMC Site #2	Universal: 3.3V or 5.0V Standard: 3.3V
I/O Access	PMC Site #1 PMC Site #2	Rear I/O signal routed on VME P2–64ac (VITA.35) Rear I/O signal routed on VME P2–44dz (VITA.35) Pins 45 to 64 are routed to P0 connector.

Miscellaneous

Size	VME double Eurocard – 6U: 233.3 mm x 160 mm
Weight	310 g

Power Requirements

Power Requirements without PMC Modules	+5V: +/– 12V: onboard +3.3V power generation for PMC	1A Typical (not including current drawn from PMC) routed from backplane to PMC

Environmental Specifications

Electromagnetic Compatibility	NF EN 55022 Class B NF EN 50082–2
Conformal Coating	optional
Airflow	1.2 m/s
Temperature Range	VITA 47–Class AC1 Cooling method: convection Operating: 0°C to +55°C Storage: –45°C to +85°C
Vibration Sine (Operating)	5–200 Hz: 2g Peak
Random	VITA 47–Class V1
Shock (Operating)	10g Peak 16 ls Half Sine
Altitude (Operating)	–1,000 to 15,000 ft
Relative Humidity	90 % without condensation

Chapter 3 - Preparing Before Using

This chapter gives guidelines on preventing static electricity discharge, environmental protection, unpacking, inspecting and identifying the V2PMC2.

3.1 Preventing Static Electricity Discharge

During unpacking and installation of the board, it is important to follow proper procedure:

1. To avoid ESD damage don't remove the board from its antistatic packaging without wearing an antistatic wrist strap. Place the strap around your wrist and connect it to an electrical ground. An electrical ground can be a piece of metal that literally runs into the ground (such as an unpainted metal pipe) or a metal part of a grounded electrical appliance. An appliance is grounded if it has a three-prong plug and is plugged into a three-prong grounded outlet.
2. After removing the board from its protective packaging (or chassis), place the board flat on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
3. Store or ship the board into its shipping box, because it is treated to assure an antistatic protection and to be stored in a protected area (EPA).

The antistatic bag is more appropriate for a one-time use and should not be considered for repeated use.

3.2 Unpacking

Don't throw out the shipping box, it should be used to store or ship the board.

The V2PMC2 is shipped in an individual, reusable shipping box closed by an ESD stick-on label.

1. First, when you receive the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent is present when the carton is opened. Keep the contents and packing materials for the agent's inspection and notify Kontron customer service department of the incident. Retain the packing list for reference.
2. Assuming that you wear an antistatic wrist strap, you can open the shipping box by cutting the ESD stick label. If the label has already been cutting, please notify the carrier and Kontron immediately.
3. If your box contains foams, remove the first foam. Kontron board is protected by an antistatic envelope.
4. When unpacking the board, observe antistatic precautions (refer to section 3.1 page 6).
5. Closely inspect the board for any signs of shipment-related damages such as loose components or bent pins. If any evidence of damage is discovered, please notify the carrier and Kontron immediately.
6. Work at an approved antistatic workstation and a grounded bench mat.

This package has been designed for shipping and it is not suitable for long-term storage (upper than two years) nor storage under severe conditions.

3.3 Inspection

Assuming that the V2PMC2 is not obviously damaged, you can now go on to inspect it. It is possible for components (connectors, socketed chips etc.) to work loose or be dislodged in transit or in the process of unpacking, although this is extremely unlikely. A quick visual inspection should reveal any obviously loose components. Any defects detected should be reported to Kontron.

3.4 Board Identification

Kontron V2PMC2 boards are identified by a label fitted to the bottom side of the board.

This is a two-row label containing:

- the board identification (Order Code) on the first row,
- the revision (3 digits) and serial number of the board on the second row.

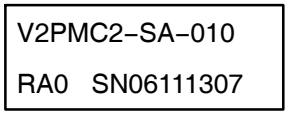


Figure 2: Identification Label

Chapter 4 - Functional Description

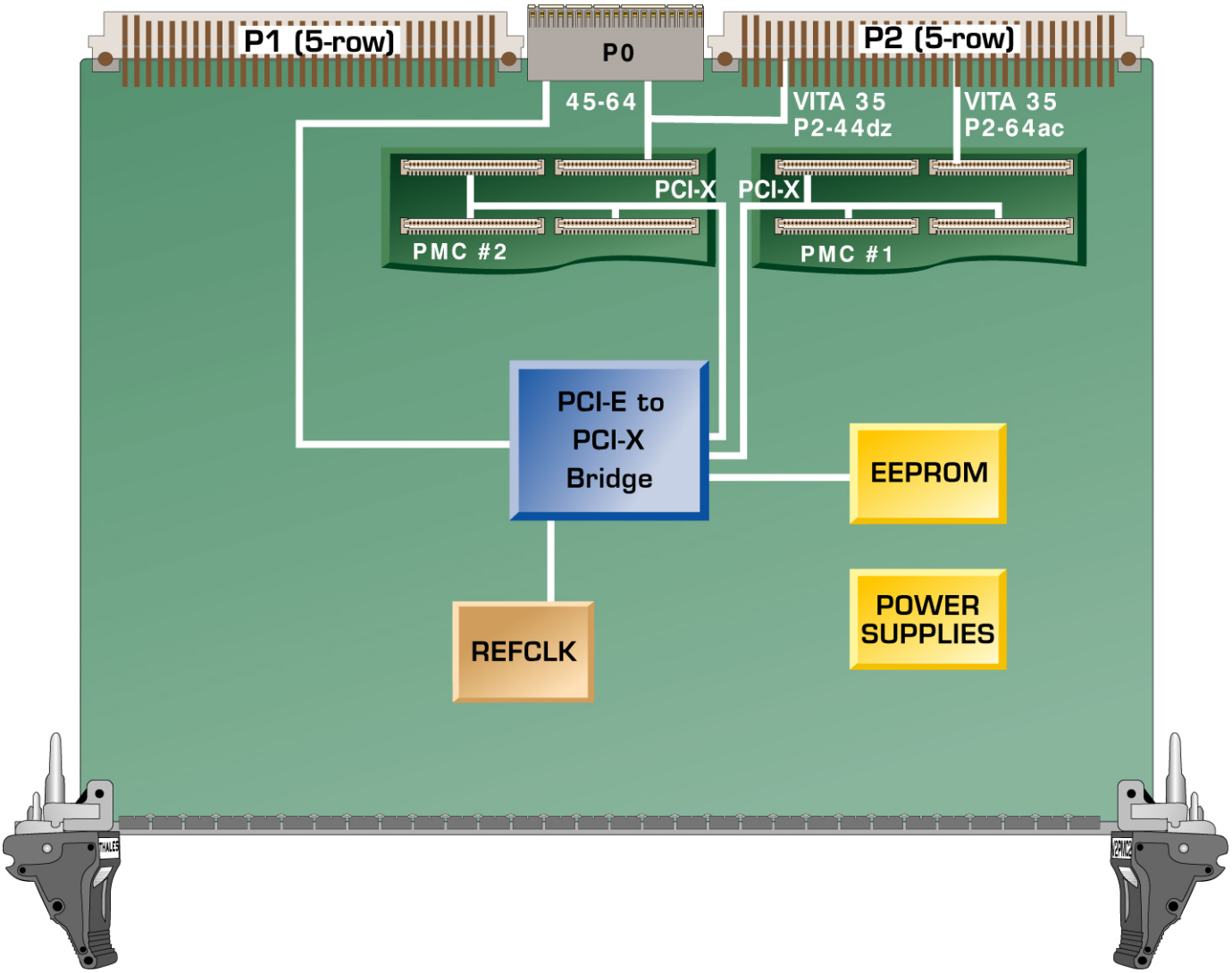


Figure 3: Simplified Block Diagram

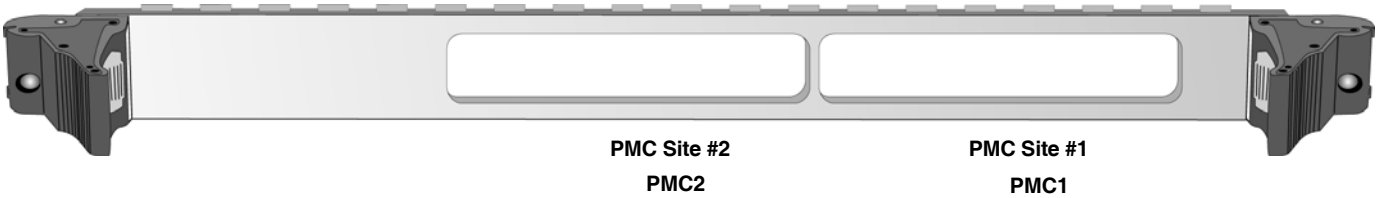


Figure 4: Front Panel

The V2PMC2 features includes:

- PCI Express (x4) from P0 connector
- PCI-Express to PCI-X bridge
- Two PMC sites (PMC Site #1 and PMC Site #2)
- PCI/PCI-X parallel bus to PMC Site #1
  - 64/32 bit data path
  - 100/66/33 MHz
  - 3.3V or 5V signaling levels
- PCI/PCI-X parallel bus to PMC Site #2
  - 64/32 bit data path
  - 133/100/66/33 MHz
  - 3.3V signaling level

There are two separate PCI busses on the board. This allows them to run at different speeds and configurations. Also, this provides greater system throughput.

4.1 PCI-E to PCI-X Bridge

A NEC uPD720400 component provides the bridging between the PCI express serial interconnect and the PMC connectors. The bridge is hardwired for forward transparent mode operation. The uPD720400 provides the PCI clocks and arbitration functions.

The PCI/PCI-X clock frequency and protocol selections are determined by the installed PMC's and may be downscaled by jumpers (refer to Table 2 "PCI/PCI-X Clock Frequency Selection" page 13). The valid auto-selectable combinations are:

- PCI-X at 133, 100 or 66 Mhz
- PCI at 66 or 33 MHz

The bridge expects the host to be external to the carrier board. In this mode the bridge generates a PCI reset (asserts RST#) during power up or when a reset message is received over the serial link. All reset sources other than the reset message will force a reconfiguration of the clock frequency and protocol on the PMC side of the bridge. Note that the host processor connected to the serial link must perform the configuration space cycles for all connected PMC boards and the bridge.

The carrier expects the external PCI Express host processor to perform the configuration cycles. This mode of operation should not require any software drivers in order to function at the minimum level.

4.2 Power

The board routes +/-12V and +5V from the VMEbus directly to the PMC sites.

The board generates its own +3.3V for the PMC sites, onboard logic and bridge as well as it's own onboard power for the bridge.

4.3 Jumpers

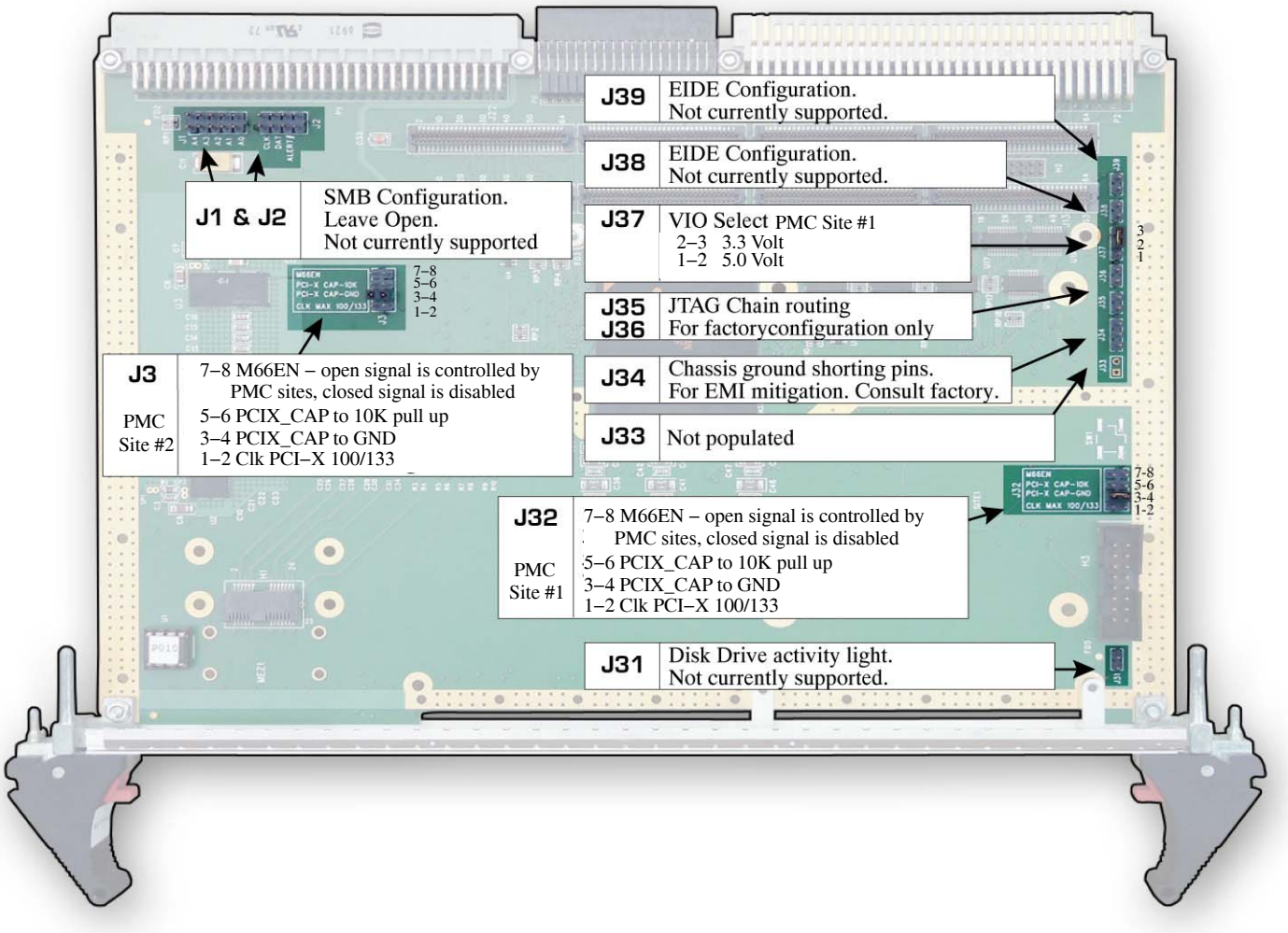


Figure 5: Jumpers Location

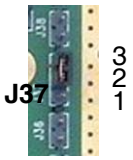
Jumpers provide board configuration control as shown in Table 1.

Identifier	Function	Default Configuration
J1 and J2	SMB Configuration. Leave open. **Not currently supported.**	OFF
H3	JTAG interface, for **factory configuration only.**	OFF
J3 (PMC Site #2) and J32 (PMC Site #1)	**1–2** PCI–X Clock 100/133 **3–4** PCIX_CAP to Gnd **5–6** PCIX_CAP resistor (to 10K pull up) **7–8** M66EN – open signal is controlled by PMC sites, closed signal is disabled	OFF ON OFF OFF
J31	Disk drive activity light. **Not currently supported.**	OFF
J33	Not populated.	
J34	Chassis ground shorting pins. For EMI mitigation. Consult factory.	OFF
J35, J36	JTAG chain routing, for **factory configuration only**.	OFF
J37	V(I/O) Select PMC Site #1 **1–2** 5.0 Volt **2–3** 3.3 Volt	 OFF ON
J38	EIDE configuration. **Not currently supported.**	OFF
J39	EIDE configuration. **Not Currently supported.**	OFF

Table 1: Jumpers Functions

OFF ==> jumper not installed
ON ==> jumper installed

V(I/O) Select PMC Site #1



The J37 jumpers configure the voltage to the V(I/O) to allow boards with specific requirements to be inserted.
J37 configures only the V(I/O) to the PMC Site #1.

- Default configuration is 3.3V signaling level:

J37	**1–2** 5.0 Volt **2–3** 3.3 Volt	OFF ON

- For a 5V signaling level configuration, set up the jumpers as follows:

J37	**1–2** 5.0 Volt **2–3** 3.3 Volt	ON OFF

PCIX_CAP

PCIX_CAP is a 3-level analog signal that is either:

- high(1)
- 3.3K-10K ohms to Ground
- Ground (0)

PCI/PCI-X Clock Fequency

The PCI/PCI-X clock frequency and protocol selections are determined by the installed PMC's and may be downscaled by J32 (for PMC Site #1) and J3 (for PMC Site #2) jumpers as described in Table 2.

PCI–X Clock (2)	PCIX_CAP to Gnd (3)	PCIX_CAP Resistor (3)	M66EN (3)	PCI Device	PCI–X Device
J3/J32 1–2	J3/J32 3–4	J3/J32 5–6	J3/J32 7–8		
Doesn't Care	Closed	Open	Closed	33 MHz	Not Capable
Doesn't Care	Closed	Open	Open	66 MHz	Not Capable
Doesn't Care	Open	Closed	Closed	33 MHz	66 MHz
Doesn't Care	Open	Closed	Open	66 MHz	66 MHz
Open	Open	Open	Closed	33 MHz	100 MHz
Open	Open	Open	Open	66 MHz	100 MHz
Closed	Open	Open	Closed	33 MHz	133 MHz
Closed	Open	Open	Open	66 MHz	133MHz

Table 2: PCI/PCI-X Clock Frequency Selection

Open == OFF ==> jumper not installed
Closed == ON ==> jumper installed

(1) All other combinations of J3/J32 jumpers are illegal.
(2) PCI-X Clock jumper settings effect only PCI-X 133/100 operation. This signal is not used during other modes of operation.
(3) Under normal operation, PCIX_CAP and M66EN jumpers should not be used because the PMC will provide the proper settings for connections.

Chapter 5 - Connectors

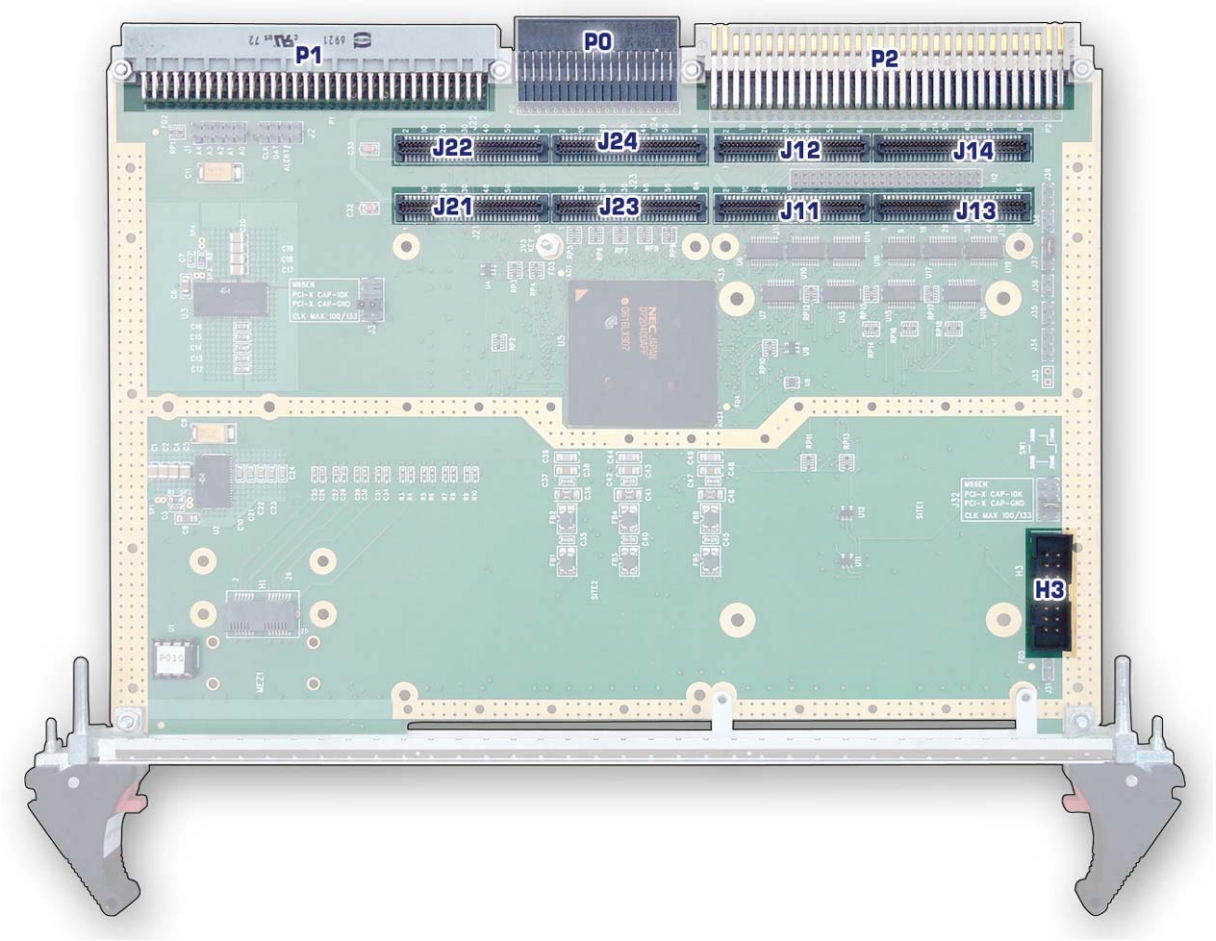


Figure 6: Connectors Location

5.1 P0, P1 and P2 Connectors

P0

P0 is a 19-row version of the 3M HSHM. This connector provides better switching characteristics tha the standard P0 connector used on the VME.

P0 provides I/O signal routing for PMC I/O signals.

P0 provides additional return pins.

P1

P1 is a 3-row connector

P1 provides +12V, -12V, and +5.0V power and return for the board.

P1 connects the VMEbus daisy chains. With the exception of power and ground the remaining VMEbus signals are not used.

P2

P2 is a 5-row connector

P2 provides additional +5V power and return pins.

P2 provides I/O signal routing for PMC I/O signals.

I/O Signal Assignments

The following tables (Table 3 and Table 4) show the P0 and P2 I/O signal assignments.

5.1.1 P0 Connector Pin Assignment

Position	Row A	B	C	D	E	F
1	Reserved		GND	Reserved		GND
2			GND			GND
3			GND			GND
4			GND			GND
5			GND			GND
6			GND			GND
7			GND			GND
8			GND			GND
9			GND			GND
10			GND			GND
11	PMC2 IO 58	PMC2 IO 60	PMC2 IO 46	PMC2 IO 48	PMC2 IO 50	GND
12	PMC2 IO 62	PMC2 IO 64	PMC2 IO 45	PMC2 IO 52	PMC2 IO 54	GND
13	PMC2 IO 61	PMC2 IO 63	PMC2 IO 56	PMC2 IO 51	PMC2 IO 53	GND
14	PMC2 IO 57	PMC2 IO 59	PMC2 IO 55	PMC2 IO 47	PMC2 IO 49	GND
15	PEX RXL0+	PEX RXL0–	GND	PEX TXL0+	PEX TXL0–	GND
16	PEX RXL1+	PEX RXL1–	GND	PEX TXL1+	PEX TXL1–	GND
17	PEX RXL2+	PEX RXL2–	GND	PEX TXL2+	PEX TXL2–	GND
18	PEX RXL3+	PEX RXL3–	GND	PEX TXL3+	PEX TXL3–	GND
19	N.C.	N.C.	Pin 5 H3 SMB_ALERT#	Pin 1 H3 SMB_CLK	Pin 3 H3 SMB_DAT	GND

Table 3: P0 I/O Signal Assignments

5.1.2 P2 Connector Pin Assignment

Position	Row Z	A	B	C	D
1	PMC2 IO 02	PMC1 IO 02	+5V	PMC1 IO 01	PMC2 IO 01
2	GND	PMC1 IO 04	GND	PMC1 IO 03	PMC2 IO 03
3	PMC2 IO 05	PMC1 IO 06	N.C.	PMC1 IO 05	PMC2 IO 04
4	GND	PMC1 IO 08	N.C.	PMC1 IO 07	PMC2 IO 06
5	PMC2 IO 08	PMC1 IO 10	N.C.	PMC1 IO 09	PMC2 IO 07
6	GND	PMC1 IO 12	N.C.	PMC1 IO 11	PMC2 IO 09
7	PMC2 IO 11	PMC1 IO 14	N.C.	PMC1 IO 13	PMC2 IO 10
8	GND	PMC1 IO 16	N.C.	PMC1 IO 15	PMC2 IO 12
9	PMC2 IO 14	PMC1 IO 18	N.C.	PMC1 IO 17	PMC2 IO 13
10	GND	PMC1 IO 20	N.C.	PMC1 IO 19	PMC2 IO 15
11	PMC2 IO 17	PMC1 IO 22	N.C.	PMC1 IO 21	PMC2 IO 16
12	GND	PMC1 IO 24	GND	PMC1 IO 23	PMC2 IO 18
13	PMC2 IO 20	PMC1 IO 26	+5V	PMC1 IO 25	PMC2 IO 19
14	GND	PMC1 IO 28	N.C.	PMC1 IO 27	PMC2 IO 21
15	PMC2 IO 23	PMC1 IO 30	N.C.	PMC1 IO 29	PMC2 IO 22
16	GND	PMC1 IO 32	N.C.	PMC1 IO 31	PMC2 IO 24
17	PMC2 IO 26	PMC1 IO 34	N.C.	PMC1 IO 33	PMC2 IO 25
18	GND	PMC1 IO 36	N.C.	PMC1 IO 35	PMC2 IO 27
19	PMC2 IO 29	PMC1 IO 38	N.C.	PMC1 IO 37	PMC2 IO 28
20	GND	PMC1 IO 40	N.C.	PMC1 IO 39	PMC2 IO 30
21	PMC2 IO 32	PMC1 IO 42	N.C.	PMC1 IO 41	PMC2 IO 31
22	GND	PMC1 IO 44	GND	PMC1 IO 43	PMC2 IO 33
23	PMC2 IO 35	PMC1 IO 46	N.C.	PMC1 IO 45	PMC2 IO 34
24	GND	PMC1 IO 48	N.C.	PMC1 IO 47	PMC2 IO 36
25	PMC2 IO 38	PMC1 IO 50	N.C.	PMC1 IO 49	PMC2 IO 37
26	GND	PMC1 IO 52	N.C.	PMC1 IO 51	PMC2 IO 39
27	PMC2 IO 41	PMC1 IO 54	N.C.	PMC1 IO 53	PMC2 IO 40
28	GND	PMC1 IO 56	N.C.	PMC1 IO 55	PMC2 IO 42
29	PMC2 IO 44	PMC1 IO 58	N.C.	PMC1 IO 57	PMC2 IO 43
30	GND	PMC1 IO 60	N.C.	PMC1 IO 59	N.C.
31	N.C.	PMC1 IO 62	GND	PMC1 IO 61	GND
32	GND	PMC IO 64	+5V	PMC1 IO 63	VPC (+5V)

Table 4: P2 I/O Signal Assignments

5.2 PMC Site 1

PMC Site 1 provides quick switch buffers on the PCI that allow 5V PMC's to be installed into the site. The signaling level remains at 3.3V levels (which is inherently supported by 5V devices), but 5V signals generated by the PMC are converted to 3.3V levels by the buffers. If no PMC card is installed in PMC Site 1 (BMODE1# is high) the quick switch buffers are put into the high impedance state. A shunt may be installed on Jumper J37, to forcibly enable the quick switch buffers for those cards that do not properly encode BMODE#1 (refer to Figure 5 page 11 and Table 1 page 12).

5.3 PMC Site 2

PMC Site 2 is a 3.3V signaling site only. This means that only those PMC's that support 3.3V signaling should be installed on that site. A key prevents 5V PMC's from being installed . The keying pin should never be removed from this site.

If the PMC is PCI-X, the bus speed should be limited to 100 MHz by the jumpers (see Table 1 on page 12 for details).

The PMC I/O signals route to both P2 and P0 as shown in Table 3 "P0 I/O Signal Assignments" page 16 and Table 4 "P2 I/O Signal Assignments" page 17.

5.4 PMC J11 / J21

Pin	Signal	Pin	Signal
1	TCK	2	–12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	N.C.
11	GND	12	N.C.
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V(I/O)	20	AD[31]
21	AD[28]	22	AD[27]
23	AD[25]	24	GND
25	GND	26	C/BE[3]#
27	AD[22]	28	AD[21]
29	AD[19]	30	+5V
31	V(I/O)	32	AD[17]
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	PCIX_CAP	40	LOCK#
41	SDONE	42	SBO#
43	PAR	44	GND
45	V(I/O)	46	AD[15]
47	AD[12]	48	AD[11]
49	AD[09]	50	+5V
51	GND	52	C/BE[0]#
53	AD[06]	54	AD[05]
55	AD[04]	56	GND
57	V(I/O)	58	AD[03]
59	AD[02]	60	AD[01]
61	AD[00]	62	+5V
63	GND	64	REQ64#

#: Signals active when low.

Table 5: J11/J21 Signal Assignments

For more information about PCI signals, refer to section 5.8 page 23.

5.5 PMC J12 / J22

Pin	Signal	Pin	Signal
1	+12V	2	TRST#
3	TMS	4	N.C.
5	TDI	6	GND
7	GND	8	N.C.
9	N.C.	10	N.C.
11	BUSMODE2#	12	+3.3VAUX
13	RST#	14	BUSMODE3#
15	+3.3V	16	BUSMODE4#
17	PME#	18	GND
19	AD[30]	20	AD[29]
21	GND	22	AD[26]
23	AD[24]	24	+3.3V
25	IDSEL	26	AD[23]
27	+3.3V	28	AD[20]
29	AD[18]	30	GND
31	AD[16]	32	C/BE[2]#
33	GND	34	IDSELB
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE[1]#	44	GND
45	AD[14]	46	AD[13]
47	M66EN	48	AD[10]
49	AD[08]	50	+3.3V
51	AD[07]	52	REQB#
53	+3.3V	54	GNTB#
55	N.C.	56	GND
57	N.C.	58	EREADY
59	GND	60	RSTO#
61	ACK64#	62	+3.3V
63	GND	64	MONARCH#

#: Signals active when low.

Table 6: J12/J22 Signal Assignments

For more information about PCI signals, refer to section 5.8 page 23.

5.6 PMC J13 / J23

Pin	Signal	Pin	Signal
1	N.C.	2	GND
3	GND	4	C/BE[7]#
5	C/BE[6]#	6	C/BE[5]#
7	C/BE[4]#	8	GND
9	V(I/O)	10	PAR64
11	AD[63]	12	AD[62]
13	AD[61]	14	GND
15	GND	16	AD[60]
17	AD[59]	18	AD[58]
19	AD[57]	20	GND
21	V(I/O)	22	AD[56]
23	AD[55]	24	AD[54]
25	AD[53]	26	GND
27	GND	28	AD[52]
29	AD[51]	30	AD[50]
31	AD[49]	32	GND
33	GND	34	AD[48]
35	AD[47]	36	AD[46]
37	AD[45]	38	GND
39	V(I/O)	40	AD[44]
41	AD[43]	42	AD[42]
43	AD[41]	44	GND
45	GND	46	AD[40]
47	AD[39]	48	AD[38]
49	AD[37]	50	GND
51	GND	52	AD[36]
53	AD[35]	54	AD[34]
55	AD[33]	56	GND
57	V(I/O)	58	AD[32]
59	N.C.	60	N.C.
61	N.C.	62	GND
63	GND	64	N.C.

#: Signals active when low.

Table 7: J13/J23 Signal Assignments

For more information about PCI signals, refer to section 5.8 page 23.

5.7 PMC J14 / J24

Pin	Signal	Pin	Signal
1	PMCx IO[01]	2	PMCx IO[02]
3	PMCx IO[03]	4	PMCx IO[04]
5	PMCx IO[05]	6	PMCx IO[06]
7	PMCx IO[07]	8	PMCx IO[08]
9	PMCx IO[09]	10	PMCx IO[10]
11	PMCx IO[11]	12	PMCx IO[12]
13	PMCx IO[13]	14	PMCx IO[14]
15	PMCx IO[15]	16	PMCx IO[16]
17	PMCx IO[17]	18	PMCx IO[18]
19	PMCx IO[19]	20	PMCx IO[20]
21	PMCx IO[21]	22	PMCx IO[22]
23	PMCx IO[23]	24	PMCx IO[24]
25	PMCx IO[25]	26	PMCx IO[26]
27	PMCx IO[27]	28	PMCx IO[28]
29	PMCx IO[29]	30	PMCx IO[30]
31	PMCx IO[31]	32	PMCx IO[32]
33	PMCx IO[33]	34	PMCx IO[34]
35	PMCx IO[35]	36	PMCx IO[36]
37	PMCx IO[37]	38	PMCx IO[38]
39	PMCx IO[39]	40	PMCx IO[40]
41	PMCx IO[41]	42	PMCx IO[42]
43	PMCx IO[43]	44	PMCx IO[44]
45	PMCx IO[45]	46	PMCx IO[46]
47	PMCx IO[47]	48	PMCx IO[48]
49	PMCx IO[49]	50	PMCx IO[50]
51	PMCx IO[51]	52	PMCx IO[52]
53	PMCx IO[53]	54	PMCx IO[54]
55	PMCx IO[55]	56	PMCx IO[56]
57	PMCx IO[57]	58	PMCx IO[58]
59	PMCx IO[59]	60	PMCx IO[60]
61	PMCx IO[61]	62	PMCx IO[62]
63	PMCx IO[63]	64	PMCx IO[64]

Table 8: J14/J24 Signal Assignments

PMCx on J14: device I/O signals from PMC Site #1 connector. Used to transmit I/O signals from PMC1.

PMCx on J24: device I/O signals from PMC Site #2 connector. Used to transmit I/O signals from PMC2.

For more information about PCI signals, refer to section 5.8 page 23.

5.8 PCI Signal Description

Mnemonic	Description
AD[0] to AD[31]	**Address/Data bits.** Multiplexed address and data bus.
ACK64#	**Acknowledge 64–bit Transfer.** Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	**Bus Mode 1.** Driven low by a PMC module to indicate that it supports the current bus mode.
BUSMODE2# to BUSMODE4#	**Bus Mode.** Driven by the host to indicate the bus mode. Always set to PCI mode on V2PMC2.
C/BE[0]# to C/BE[3]#	**Bus Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus.
CLK	**Clock.** Except RST#, INTA#, INTB#, INTC# and INTD#, all 32–bit PCI bus signals are synchronous to 33 MHz clock.
DEVSEL#	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	**FRAME.** Driven low by the current master to signal the start and duration of an access.
GNT#	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent.
IDSEL	**Initialization Device Select.** Device chip select during configuration cycles.
INTA# to INTD#	**Interrupt lines.** Level–sensitive, active–low interrupt requests.
IRDY#	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	**LOCK.** Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	**66MHZ_ENABLE.** 66 MHz enabling lines is defined as GND for 33 MHz backpanes.
N.C.	This pin is not connected.
PAR	**Parity.** Parity protection bit for AD[0] to AD[31] and C/BE0# to C/BE3#.
PERR#	**Parity Error.** Driven low by a PCI agent to signal a parity error.
PMCx IO[1] to PMCx IO[64]	**PCI PMC signals.** Used to transmit I/Os signals from PMC connector (J14 or J24) to P2 and P0 connector.
PME	**Power Management Event.** Used by a device to request a change in the device or system power state.
REQ#	**Request.** Driven low by a PCI agent to request ownership of the PCI bus.
	Page 1 of 2

Mnemonic	Description
REQ64#	**Request 64–bit Transfer.** Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	**Reset.** Driven low to reset the PCI bus.
SBO#	**Snoop Backoff.** Indicate a hit to a modified line when asserted.
SDONE	**Snoop Done.** Indicate the status of the snoop for the current access.
SERR#	**System Error.** Driven low by a PCI agent to signal a system error.
STOP#	**STOP.** Driven low by a PCI target to signal a disconnect or target–abort.
TCK	**Test Clock.** Used to clock state information and test data into and out of the device during operation of the TAP (JTAG) controller.
TDI	**Test Data Input.** Used to serially shift test data and test instructions into the device during TAP operation.
TDO	**Test Data Output.** Used to serially shift test data and test instructions out of the device during TAP operation.
TMS	**Test Mode Select.** Used to control the state of the TAP controller in the device.
TRST#	**Test Reset.** Provide an asynchronous initialization of the TAP controller.
TRDY#	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase.
V(I/O)	**PCI I/O Buffer Voltage.** Power supply delivered by the board. Fixed by the backplane.
+3.3V	+3.3 Volts DC power
+3.3VAUX	An optional 3.3 volt auxiliary power source delivers power to the PCI add–in card for generation of power management events when the main power to the card has been turned off by software.
+5V	+5 Volts DC power
+12V	+12 Volts DC power.
–12V	–12 Volts DC power.
	Page 2 of 2

Table 9: PCI Signal Description

Chapter 6 - Installation

6.1 V(I/O) and Voltage Keying Pins

PMC Site #1

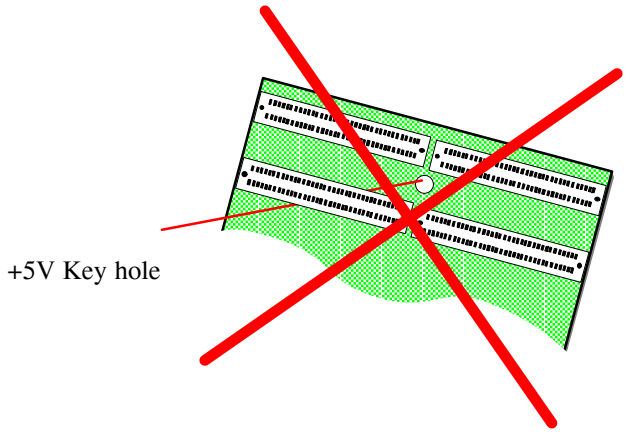
By default, PMC Site #1 is a 3.3V signaling site. PMC Site #1 provides quick switch buffers on the PCI that allow 5V PMC's to be installed into the site. The signaling level remains at 3.3V levels (which is inherently supported by 5V devices), but 5V signals generated by the PMC are converted to 3.3V levels by the buffers. If no PMC card is installed in PMC Site 1 (BUSMODE1# is high) the quick switch buffers are put into the high impedance state.

A shunt may be installed on Jumper J37, to forcibly enable the quick switch buffers for those cards that do not properly encode BUSMODE#1 (refer to Figure 5 page 11 and Table 1 page 12).

PMC Site #2

PMC Site #2 is a 3.3V signaling site only. This means that only those PMC's that support 3.3V signaling should be installed on that site.

A 3.3V voltage selection key is provided on the board, to make sure not to insert a +5V PMC on the PMC Site2. Failture to observe this restriction may result in damage to the PMC or the V2PMC2.



6.2 Installation of a PMC Module

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

The installation of the PMC on the V2PMC2 conforms to the IEEE P1386.1 standard.

To install the PMC module, refer to Figure 7 "PMC Site 1" and Figure 8 "PMC Site 2" and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the V2PMC2 board or the PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the V2PMC2 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the appropriate PMC slot of the V2PMC2.
3. Check that the standoffs are attached to the PMC.
4. Install the PMC, component-side down, aligning the PCI connectors with their mating connectors on the V2PMC2. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the V2PMC2 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.
5. Screw the PMC in place using the 4 mounting points, on the bottom side of the V2PMC2 . You need a Phillips screwdriver for this stage.
6. The PMC attachment is now complete.
7. Insert the V2PMC2 into the chassis making sure it is plugged into the backplane.

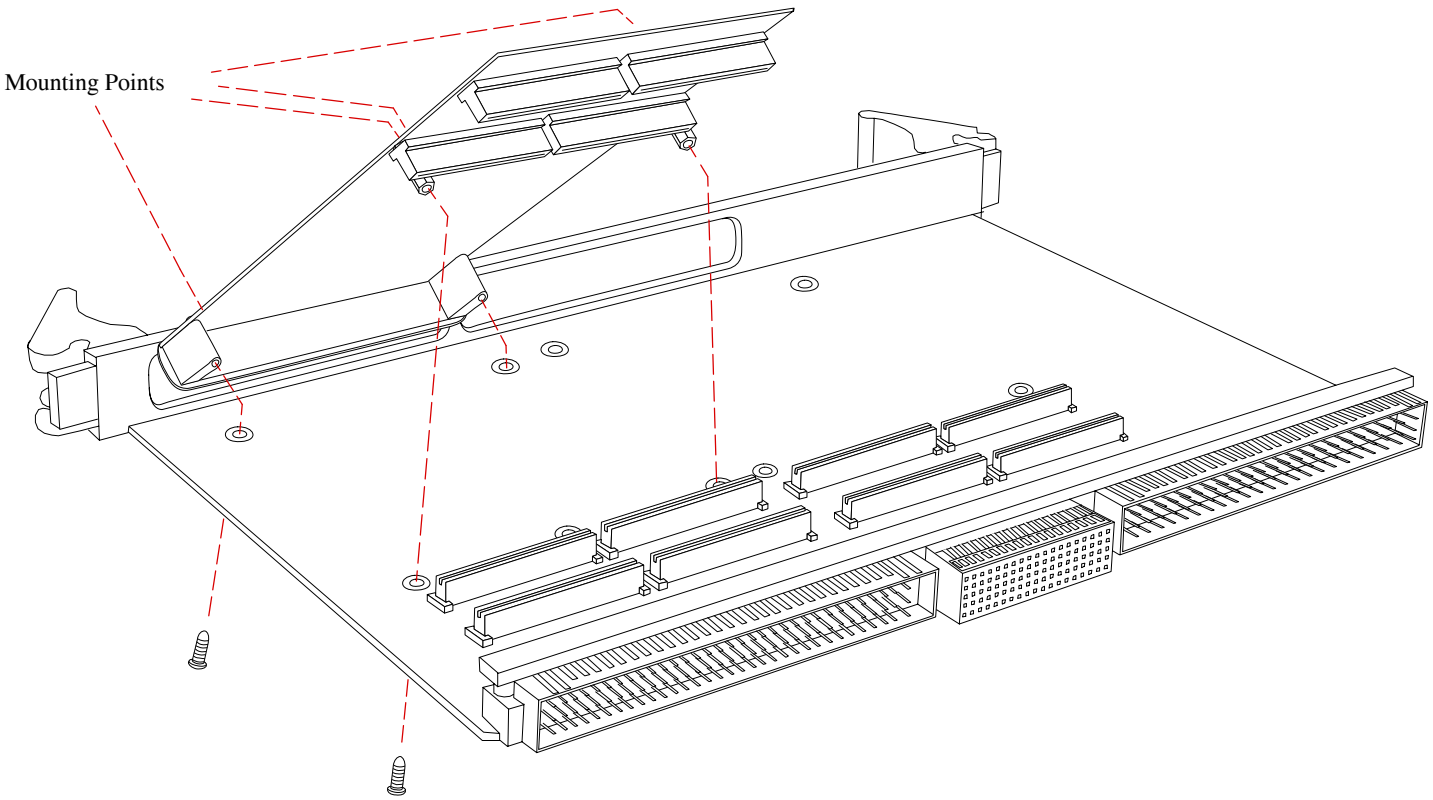


Figure 7: PMC Site 1 Installation

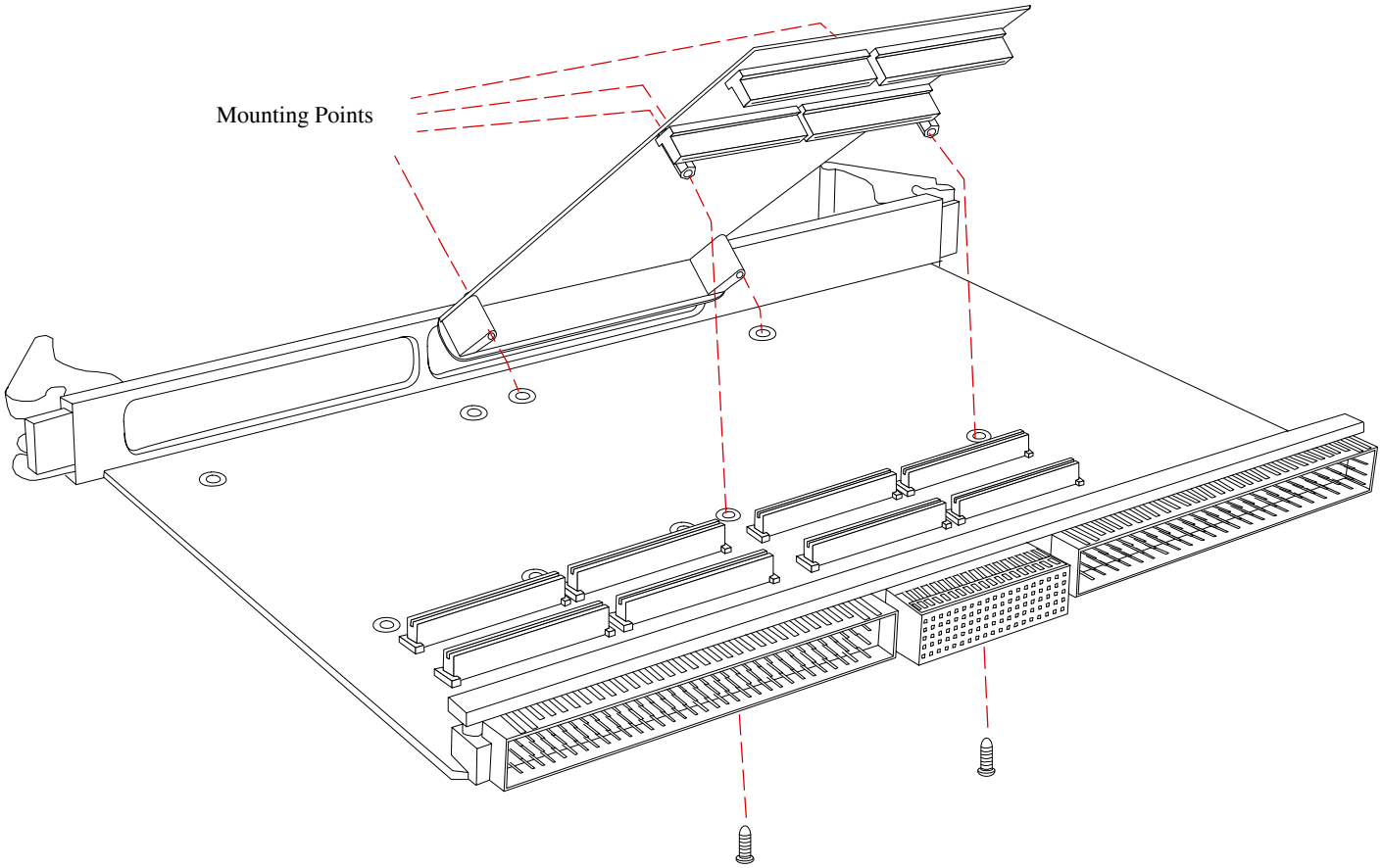


Figure 8: PMC Site 2 Installation

6.3 Installation of the Motherboard and the V2PMC2 into a Rack

The rack used in following examples is a Kontron **R2U4S.**

Refer to the R2U4S - Rack Mount Industrial Chassis - Installation and User's Manual (SD.DT.E84), for a complete description of the rack.

Note in following picture, the location of the P0, P1 and P2 connectors on the rear panel of the rack.

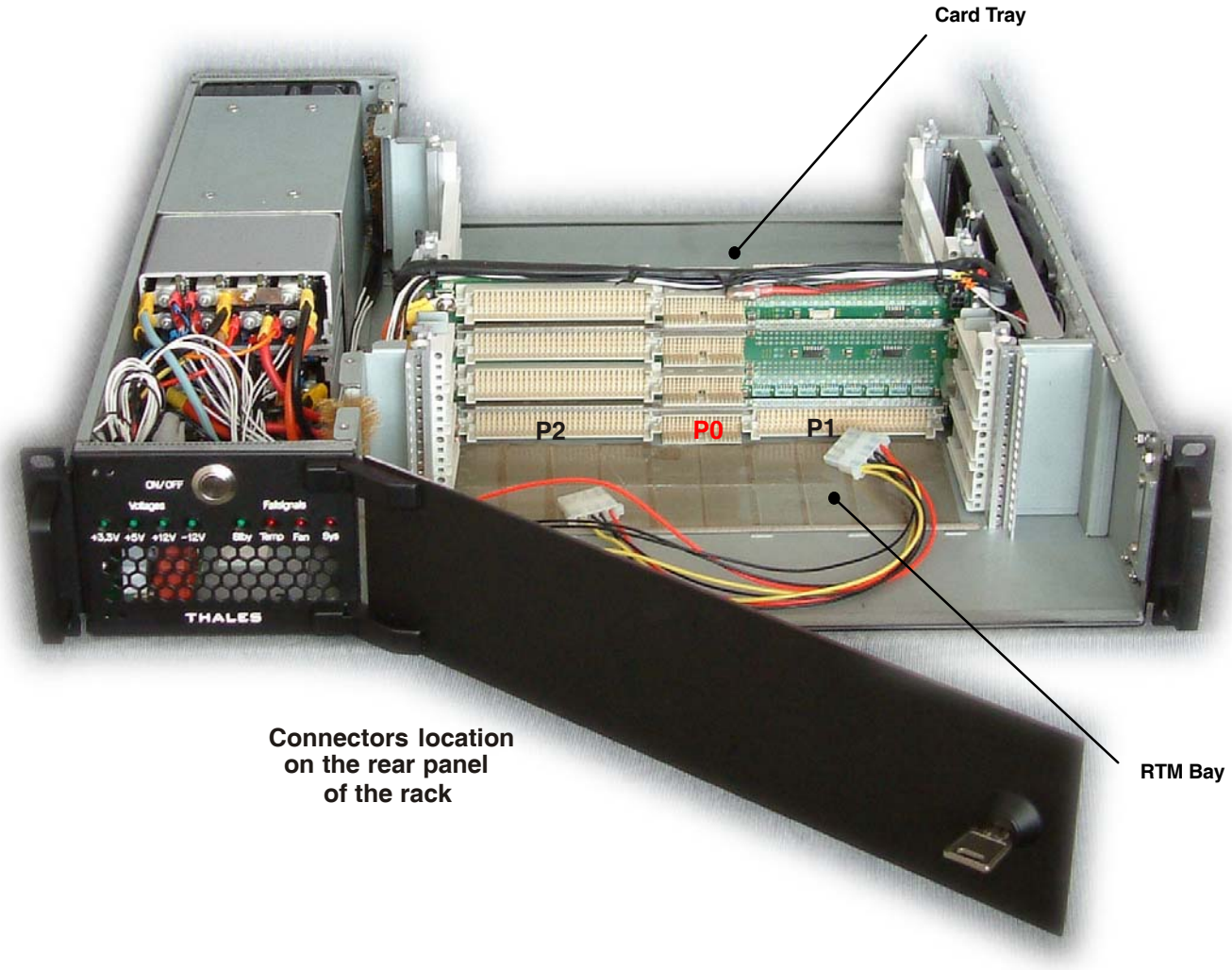


Figure 9: R2U4S Overview

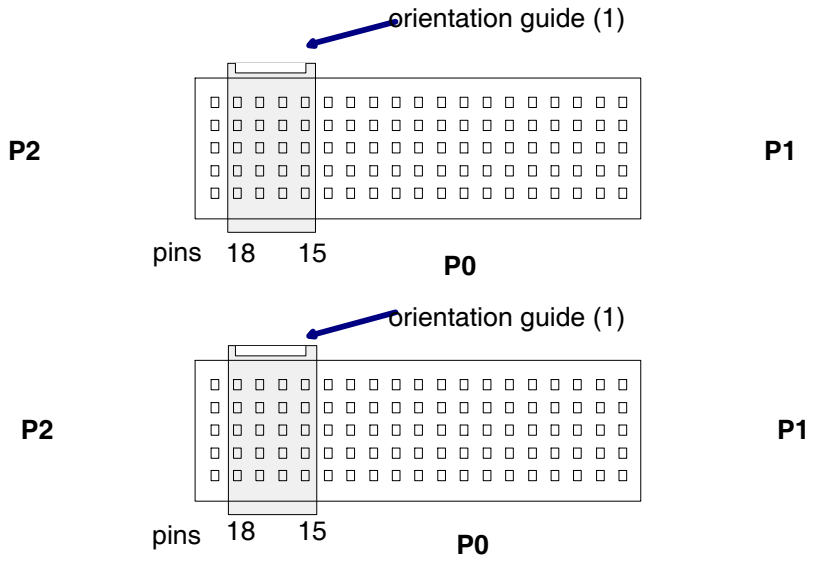
6.3.1 P0 to P0 Connection

1. Insert the motherboard, then the V2PMC2 carrier board into the chassis.

Insert the V2PMC2 in the slot just above the motherboard.

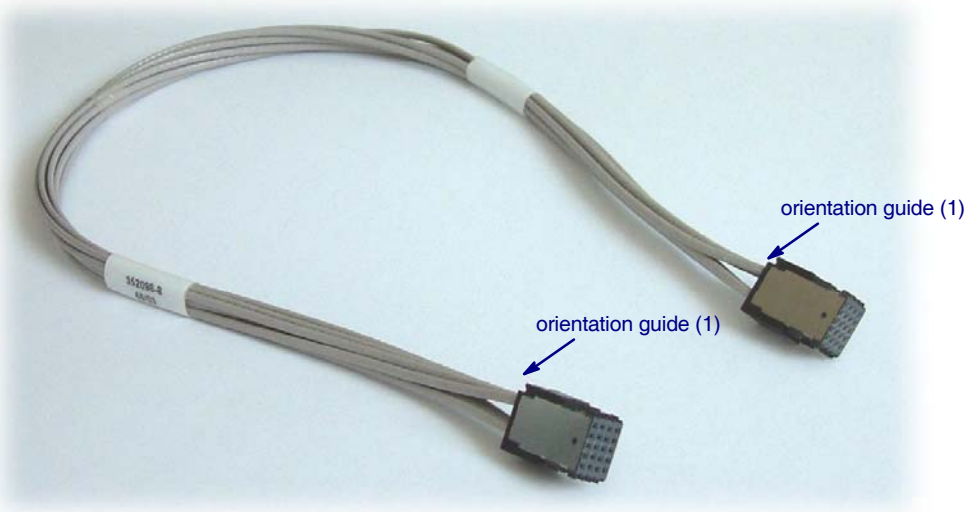
2. Connect the P0 backplane connector of the motherboard to the P0 backplane connector of the V2PMC2 as described hereafter using a rear P0 cable (Kontron Order Code: CABL–ZPACK–X4–022). The cable interconnects two x4 PCI-Express serial I links via two ZPACK female connectors (5x4 pins).

   The ZPACK connectors must be connected respectively to the pins [15-18] of the rear P0 connector of the rack where the motherboard and the V2PMC2 board are installed.



Connectors viewed from the rear panel of the rack

(1) The orientation guide (position of the notch located on one side of each connector) must be set up on the same side of the P0 connector of the motherboard and the V2PMC2 carrier board.



6.3.2 RTM to P0 Connection

Please contact your Kontron representative for detailed information on this topic and the availabily date of such a configuration.

6.3.3 System Backplane Compliance

The backplane of the rack where a V2PMC2 board is inserted, must conform to the VME64X standard: ANSI/VITA 1.1-1997. More precisely, the P0 connectors of the backplane must conform to the level 1 of the IEC 16076-4-101 standard (length of the pins of the [a-e] rows = 8.2 mm).

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